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A curvature-corrected CMOS bandgap reference

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Abstract. This paper presents a CMOS bandgap reference that employs a curvature correction technique for compensating the nonlinear voltage temperature dependence of a diode connected BJT. The proposed circuit cancels the first and the second order terms in the $V_{BE}(T)$ expansion by using the current of an autopolarized Widlar source and a small correction current generated by a MOSFET biased in weak inversion. The voltage reference has been fabricated in a 0.35 μm 3Metal/2Poly CMOS technology and the chip area is approximately 70 μm × 110 μm. The measured temperature coefficient is about 10.5 ppm/K over a temperature range of 10–90°C while the power consumption is less than 1.4 mW.

1 Introduction

Voltage references are widely used in applications such as A/D and D/A converters, acquisition data systems or smart sensors. As the precision of these circuits increases, the requirements for the reference stability with temperature, supply and process variations have also increased.

Since introduced by Widlar (1971), the bandgap reference (BGR) has been extensively used to obtain a constant value of the reference voltage with respect to temperature variations. The basic idea of a first-order compensated BGR is to cancel the negative temperature dependency of the V_{BE} by adding a correction factor proportional to the thermal voltage V_t which has a positive variation with temperature. The temperature coefficient (TCR) that can be obtained with this approach is generally greater than 30 ppm/K, being acceptable only for applications that do not require a very good accuracy (Ferro et. al., 1989; Tham and Nagaraj, 1995; Vermaas et al., 1998; Banba et al., 1999). This TCR limitation is determined by the fact that V_t is a fully linear function of T while V_{BE} is a complex function of T that contains higher order terms (Filanovsky and Chan, 1996) – see also Eq. (1).

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A first way to improve the TCR of a bandgap reference is to correct the nonlinear temperature dependence of the base-emitter voltage by a suitable polarization of the bipolar transistor. In Filanovsky and Chan (1996), a polarization at a PTAT^3 + PTAT^4 collector current reduces the temperature coefficient to 4–8 ppm/K. The curvature-correction technique from Popa (2001), based on the polarization of the bipolar transistor at a PTAT^n current, reports a TCR of 20 ppm/K without trimming and chip temperature stabilization. Also these methods are conceptually simple, generating PTAT^n currents requires complex circuits which consume significant chip area and power.

Another possibility to improve the temperature dependence of a BGR is to add a correction voltage to the basic reference voltage (Salminen and Halonen, 1992), or a correction current to the PTAT current (Gunawan et al., 1993; Lee et al., 1994). The voltage reference presented in Salminen and Halonen (1992) has a relatively large temperature coefficient, about 30 ppm/K for a limited temperature range, due to the MOS parameters mismatching. The current compensation technique (Gunawan et al., 1993; Lee et al., 1994) decreases the temperature coefficient to less than 10 ppm/K but requires a large silicon area and it is not compatible with the CMOS technology.

This paper proposes a TCR improvement technique based on the compensation of the base-emitter nonlinearity with a current with an opposite temperature dependence, which will cancel the first and second-order harmonics in $V_{BE}(T)$. The main problem is to find a suitable implementation of a current generator with superior-order harmonics in its temperature expansion. In Sect. 2 the proposed circuit for implementing this technique is introduced and analyzed. Section 3 presents the experimental results: the measured temperature coefficient is 10.5 ppm/K for a temperature range of 10–90°C. The compatibility with CMOS technology is fulfilled because only MOS and pnp transistors have been used.

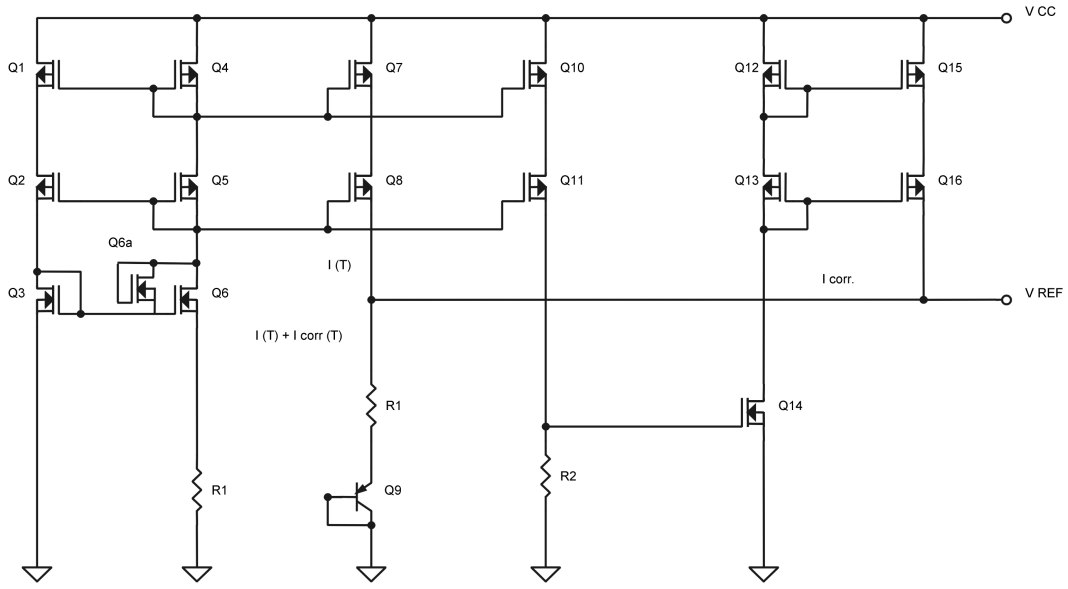

Fig. 1. Weak inversion curvature-corrected bandgap reference.

2 Circuit design

The temperature characteristic of the base-emitter voltage of a BJT can be expressed like Filanovsky and Chan (1996):

$$V_{BE}(T) = E_G(T) + \frac{T}{T_0}[V_{BE}(T_0) - E_G(T_0)] + \\ + \frac{KT}{q} \ln\left[\frac{I_C(T)}{I_C(T_0)}\right] - \eta \frac{KT}{q} \ln\frac{T}{T_0} \quad (1)$$

where T_0 is the reference temperature, E_G is the silicon bandgap voltage, $I_C(T)$ is the collector current of the bipolar transistor (considering a general temperature dependency) and η is a constant specific for each technology having typical values around 4. According to Lee et al. (1994), the temperature dependence of the silicon bandgap voltage can be very accurately modeled (with an error smaller than 0.2 mV) by the following empirical equation:

$$E_G(T) = a - bT - cT^2 \quad (2)$$

$$\text{with} \quad \begin{aligned} a &= 1.1785\,V \\ b &= 9.025 \times 10^{-5} V/K \quad \text{for} \quad 150\,K \le T \le 300\,K \\ c &= 3.05 \times 10^{-7} V/K^2 \\ a &= 1.20595\,V \\ \text{and} \quad b &= 2.7325 \times 10^{-4} V/K \quad \text{for} \quad 300\,K < T \le 400\,K. \\ c &= 0 \end{aligned}$$

In order to improve the TCR we propose a CMOS implementation of a correction technique that exploits the exponential characteristic of a MOS transistor working in weak inversion – see Fig. 1.

The bipolar transistor Q9 and the resistor R1 form the core of the circuit: the reference voltage is the sum of V_{BE} and the voltage drop across R1. The autopolarized Widlar current source Q1-Q6 produces a PTAT current that is further mirrored through Q7-Q8 for biasing the BJT. Q6a is a start-up transistor that drives the circuit out of the degenerated bias point when the supply is turned on. Q10, Q11 and R2 generate the gate voltage of Q14 and should be dimensioned such that Q14 is biased in weak inversion ($V_{GS} < V_{TN}$). The current of Q14 is multiplied by Q12-Q16 and further injected in R1 to cancel the second order harmonics in $V_{BE}(T)$. The main PTAT current has the following expression (Razavi, 2001):

$$I(T) = \frac{2}{KN(W/L)_3 R1^2} \frac{(W/L)_7}{(W/L)_4} \left(1 - \sqrt{\frac{(W/L)_3}{(W/L)_6}}\right)^2 \quad (3)$$

Because the bipolar transistor is biased at a collector current $I(T)$ (we can neglect I_{corr}), the base-emitter voltage will have the following general expansion around the reference temperature T_0:

$$V_{BE}(T) = V_{BE}(T_0) + \sum_{k=1}^{\infty} a_k (T - T_0)^k \quad (4)$$

where a_k are constant coefficients of the expansion, with the following expressions $a_1 = [V_{BE}(T_0) - E_G(T_0)]/T_0 - b - 2cT_0 - (\eta - 1)K/q$, $a_2 = (\eta - 1)K/2qT_0 - c$, etc. The first term in Eq. (4) is a constant term. The next two terms (the linear and quadratic terms) will be cancelled by adding convenient correction factors to the base-emitter voltage. The influence of the superior-order terms (a_3, a_4, ...) will be further neglected.

The basic idea for improving the temperature behavior of the bandgap reference is to add a very small correction current, I_{corr} to the PTAT current $I(T)$, in order to compensate the first two-order terms from the base-emitter voltage expansion. Because this correction current has to be small and

Table 1. Measurement results

T (°C)	14	22	30	38	46	54	62	70	78	86	94
Vref (V)	1.1833	1.183	1.1834	1.1835	1.1834	1.1835	1.1831	1.183	1.1825	1.1828	1.1835

must contain at least second-order terms in its temperature expression, the proposed circuit for obtaining this current is based on a MOS transistor (Q14) working in weak inversion. Thus, the correction current is given by:

$$I_{\text{corr}}(T) = A \exp\left[\frac{I(T)R2 - V_{TN}}{nV_t}\right] \tag{5}$$

where $A = (W/L)_{14} I_{D0} \frac{(W/L)_{15}}{(W/L)_{12}}$ and $I(T) \gg I_{corr}(T)$. In this case, the reference voltage is:

$$V_{REF}(T) = V_{BE}(T) + [I(T) + I_{\text{corr}}(T)]R1 =$$
$$= V_{BE}(T) + V_{R1}(T) \tag{6}$$

Using the Taylor's series, the correction voltage given by the voltage drop across $R1$ can be expressed like:

$$V_{R1}(T) = V_{R1}(T_0) + \sum_{k=1}^{\infty} b_k (T - T_0)^k \tag{7}$$

where b_k are constant coefficients of the expansion, with the following expressions $b_1 = K_w + A \frac{V_{14}}{nV_{t0}} \frac{1}{T_0} \exp\left(\frac{V_{14}}{nV_{t0}}\right)$, $b_2 = -A \frac{V_{14}}{nV_{t0}} \frac{1}{T_0^2} \left(2 + \frac{V_{14}}{nV_{t0}}\right) \exp\left(\frac{V_{14}}{nV_{t0}}\right)$, etc. and $V_{14} = I(T_0)R2 - V_{TN}$. Finally, the output voltage is:

$$V_{REF}(T) = V_{REF}(T_0) + \sum_{k=1}^{\infty} a_k (T - T_0)^k +$$
$$+ \sum_{k=1}^{\infty} b_k (T - T_0)^k \tag{8}$$

In order to cancel the linear and the quadratic term from Eq. (8), the design conditions are:

$$a_1 + b_1 = 0 \quad \text{(to cancel the linear term)}$$
$$a_2 + b_2 = 0 \quad \text{(to cancel the quadratic term)} \tag{9}$$

The remaining nonlinearities of the BGR will be now given only by the superior-order terms (greater than two) from the reference voltage expansion. Other sources of errors could be transistors mismatches, the neglect of the correction current I_{corr} when Eq. (4) was deduced, or the finite value of the current gain of the pnp transistor.

3 Experimental results

The circuit was dimensioned using the previous design relations and Spectre® simulations. The following values have been employed for the transistors widths: W1–5 = 2 μm, W7–8,10–11 = 8 μm, W14–16 = 1 μm, W6,12–13 = 4 μm. All MOS devices have the minimum length $L = 0.3\,\mu$m.

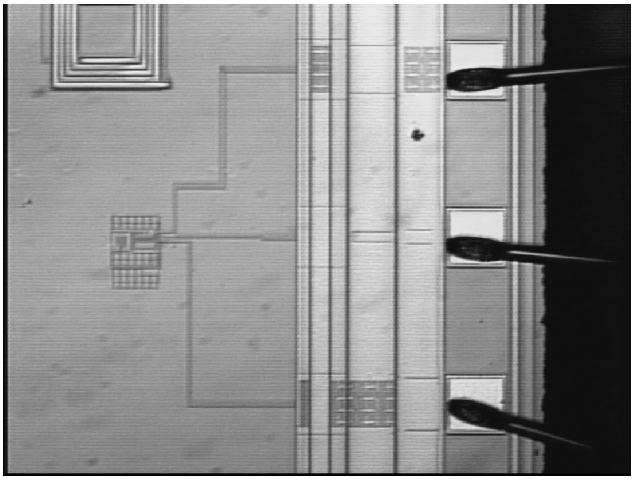

Fig. 2. Chip micrograph.

The values used for resistances are: R1 = 1.9 kΩ and R2 = 2.5 kΩ. The reference consumes approximately 0.4 mA from a supply voltage of 3.3 V.

The circuit was laid out and fabricated using the 0.35 μm CMOS AMS technology, available through the Europractice program – see the chip micrograph in Fig. 2. Special care was taken for avoiding mismatching between paired MOS devices and resistors. The silicon occupied area was about 70 μm × 110 μm, much smaller than that reported in other curvature-corrected voltage references with comparable performances (290 μm × 150 μm in Tham and Nagaraj (1995), 380 μm × 190 μm in Lee et al. (1994) and 600 μm × 220 μm in Gupta and Black (1996)).

Measurements and simulation results of the curvature-compensated voltage reference are presented in Table 1 and Fig. 3. The achieved temperature coefficient is about 10.5 ppm/K (without thermal stabilization of the chip) for a temperature range of 10–90°C.

4 Conclusions

A curvature-correction technique based on the compensation of the base-emitter voltage nonlinearity, using as correction the drain current of a MOS transistor working in weak inversion, was presented. The cancellation of the first and second-order term from the polynomial expansion of the base-emitter voltage allows the reduction of the temperature coefficient of the bandgap reference to about 10 ppm/K, for an extended temperature range. In addition, this circuit offers the possibility to cancel other superior-order terms which af-

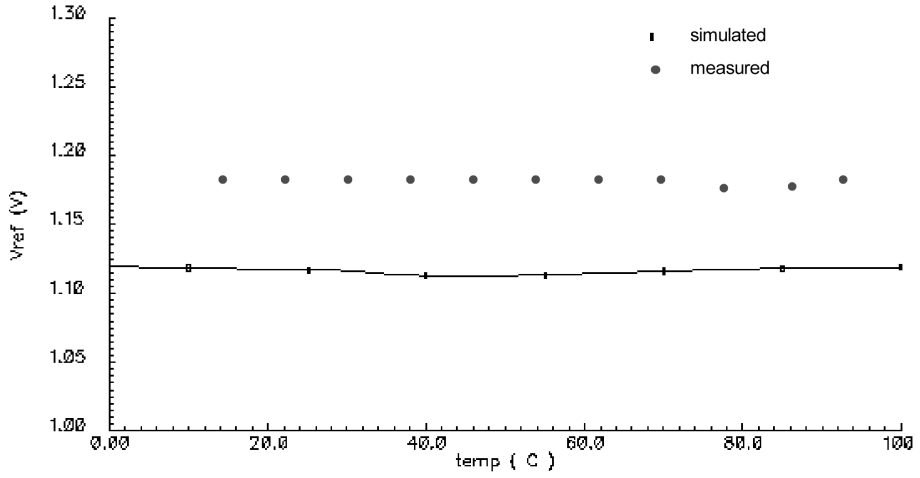

Fig. 3. Measurement and simulation results.

fect the TCR: the design condition for canceling the kth – order harmonic is $a_k + b_k = 0$.

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