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Resonance circuits for adiabatic circuits

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Abstract. One of the possible techniques to reduces the power consumption in digital CMOS circuits is to slow down the charge transport. This slowdown can be achieved by introducing an inductor in the charging path. Additionally, the inductor can act as an energy storage element, conserving the energy that is normally dissipated during discharging. Together with the parasitic capacitances from the circuit a LC-resonant circuit is formed.

1 Introduction

In conventional CMOS logic the load capacitor is charged to V_{DD} via the PMOS block (pull up network) and discharged to *GND* via the NMOS block (pull down network). During the charging of the output, the power supply has to deliver a charge $Q = C_L V_{DD}$ at the voltage V_{DD} resulting in a supplied energy of $QV_{DD} = C_L V_{DD}^2$. that dissipats as heat.

To decrease the dissipated energy, the charge transport can be slowed down. Using a ramp-like charging voltage, the output capacitance is charged at a constant current. This current source delivers the charge $C_L V_{DD}$ over a period of time T. The dissipation through the resistance of the charging path R is then (Chandrakasan and Brodersen, 1995):

$$E_{diss} = P \cdot T = I^2 RT = \left(\frac{C_L V_{DD}}{T}\right)^2 RT = \left(\frac{RC_L}{T}\right) C_L V_{DD}^2 \ . \quad (1)$$

This shows that it is possible to charge and discharge a capacitance through a resistance while dissipating less energy than $C_L V_{DD}^2$. By introducing an energy storage element, the energy that is normally dissipated as capacitances are discharged can be conserved for later use. This can be observed in LC resonant circuits, where the energy oscillates between the capacitance and the inductance.

To determine the efficiency of a resonant circuit, the amount charge per charging/discharging cycle of an ideal abrupt charge/discharge circuit can be compared to the average charge required by the oscillator.

$$E_{oscillator,percycle} = \frac{i_{avg,osc}}{f_{osc}} \quad (2)$$

$$E_{abrupt,percycle} = C_{load} \cdot V_{dd} \quad (3)$$

In the equations C_{load} is the sum of all capacitances in the resonance circuit and f_{osc} the frequency of the oscillator. From this equations we can determine the efficiency of an oscillator

$$\eta = \frac{E_{oscillator,percycle}}{E_{abrupt,percycle}} = \frac{\frac{i_{avg,osc}}{f_{osc}}}{C_{Load} \cdot V_{dd}} \quad (4)$$

This means, that at a resonant circuit with an efficiency of 70% dissipates only 30% of the power of an abrupt charging circuit.

2 Multi-stage charging

A very simple approach to implement a charging/decharging circuit is to use multi-stage charging (Saas et al., 2001). Multi-stage charging is not a LC oscillator due to its missing inductor however it is presented here as comparision to the other resonant oscillators. The basic concept is to charge/discharge the capacitance stepwise in n steps each with the voltage $V_{step} = \frac{V_{supply}}{n}$.

Multi-stage charging also reuses the charge stored in the load capacity. Under the assumption that the pull-up transistors charge the load to the full supply voltage, the power dissipation for discharging is the same as for charging. It is not necessary to use power supplies for the intermediate voltages because the average current is zero in the ideal case.

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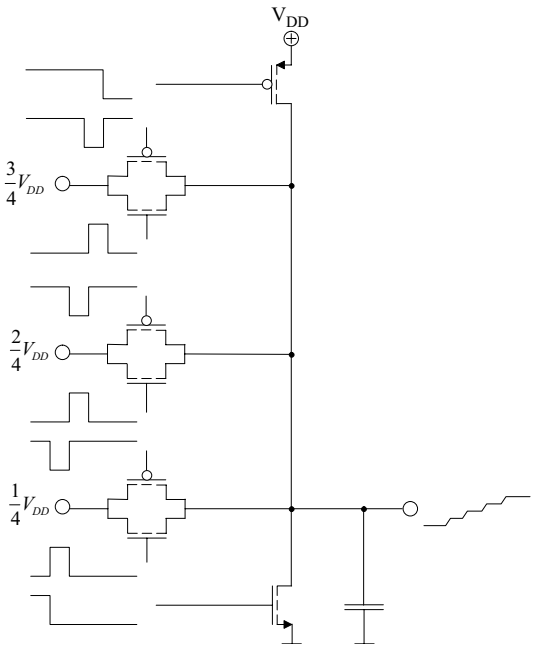

Fig. 1. Principle of multi-stage charging.

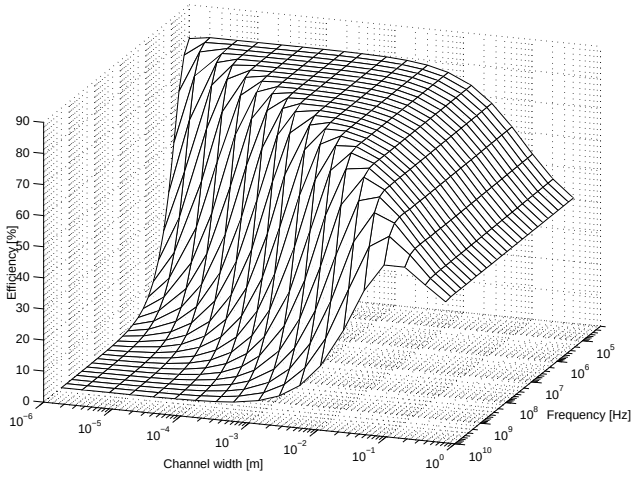

Fig. 2. Efficiency for 5-stage (4 intermediate voltages) charging/discharging.

Instead, large buffering capacitors are sufficient. These capacitors must be charged to the desired voltage just at startup and afterwards it is only necessary to compensate losses.

The efficiency of the multi-stage charging is assessed through a simulation that is depicted in Fig. 2. This simulation was done for a five step circuit, this means four intermediate voltages are used. The current consumption is calculated for a load capacity of 1500 pF, the current consumed by the control logic is estimated to be equal to the current needed for driving the pass transistor gates. This means, that the current is twice the current consumed by driving the pass transistor gates. The channel length of the transistors is 0.35 μm and the circuit is supplied with 3.3 V. The top area

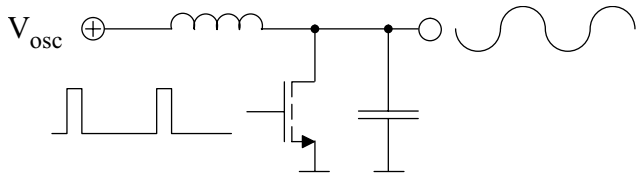

Fig. 3. Schematic of the one transistor oscillator.

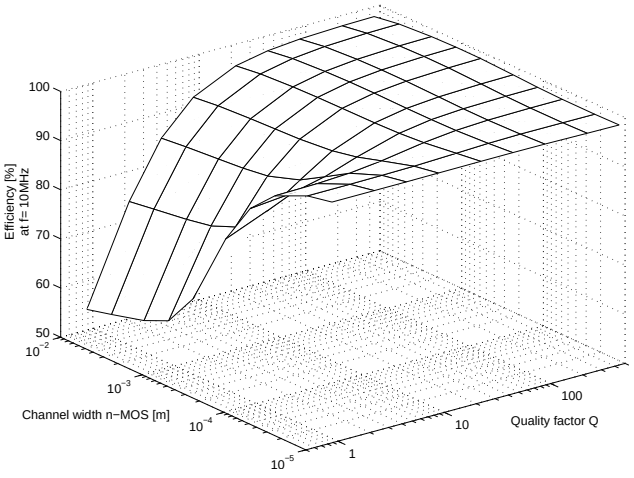

Fig. 4. Efficiency for one transistor oscillator.

of the graph shows the range for usefull operation. Increasing the channel width leads to bad efficieny because of the rising current consumption for the control logic. The other limitation is the charging time, increasing the operating frequency reduces the time period for charging/discharging the load capacity. If the time interval is getting to small the load capacity can not be completely charged or discharged. Consequently case multi-stage charging is not applicable in this case.

3 Continuously oscillating circuits

3.1 One transitor resonant circuit

The simplest attempt to design a resonant circuit is the 1-transistor circuit depicted in Fig. 3 (Voss, 2001). The gate of the transistor is driven by a control signal that must be derived from an other oscillator, i.e. a crystal oscillator. Besides the control of the frequency the gate driver logic has also to control the duty cycle of the transistor. The efficiency diagram of this oscillator is depicted in Fig. 4. This diagram results from a simulation with a transistor channel length of $w_n = 0.35\,\mu$m, a resonant capacity of $C_{res} = 1500$ pF, an inductance with $L_{res} = 170$ nH and a supply voltage of $V_{osc} = 1.65$ V. The oscillation frequency is about 10 MHz. The gate of the MOSFET is driven with a pulse width $pw = 10$ ns (equiv. to a duty cycle of $\approx$ 10%) and a periode of $per = 100$ ns (resonance frequency). The power consumption of the driver logic for the transistor gate was also taken

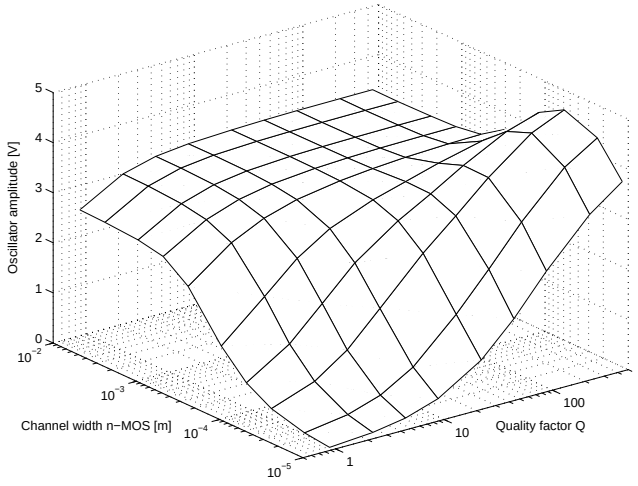

Fig. 5. One transistor oscillator: Variation of the quality factor of the inductor.

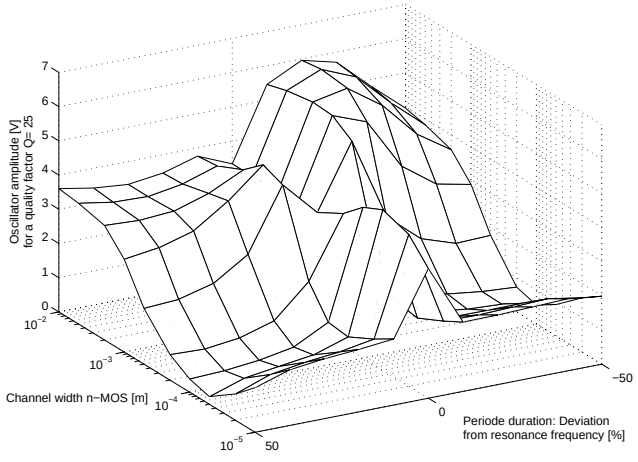

Fig. 6. One transistor oscillator: Amplitude as function of variation of the control frequency.

into account. It's value was estimated as twice the power needed for driving only the gate of the MOSFET.

In Fig. 3.1 the amplitude of the oscillator as a function of the channel width of the MOSFET and the quality factor of the inductor is shown. It can be seen that only for very high quality factors of the inductor and small channel width of the MOSFET the amplitude of the oscillation differs from the nominal value (3.3 V, twice the oscillator voltage).

In Fig. 3.1 the periode duration of the gate drive signal is varied from the period duration at resonance frequency (frequency mismatch) and the resulting oscillator amplitude is drawn. It can be seen very clearly that the oscillator is only working well within in the range of some percent around the resonance frequency. This limits also changes in the load capacity because these changes are equal to changes in the resonance frequency as it can be derived from the calculation of

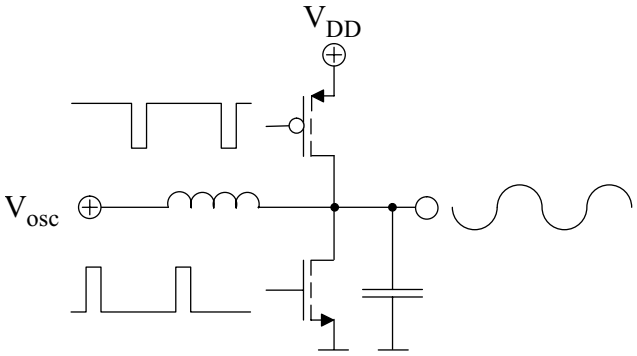

Fig. 7. Two transistor oscillator.

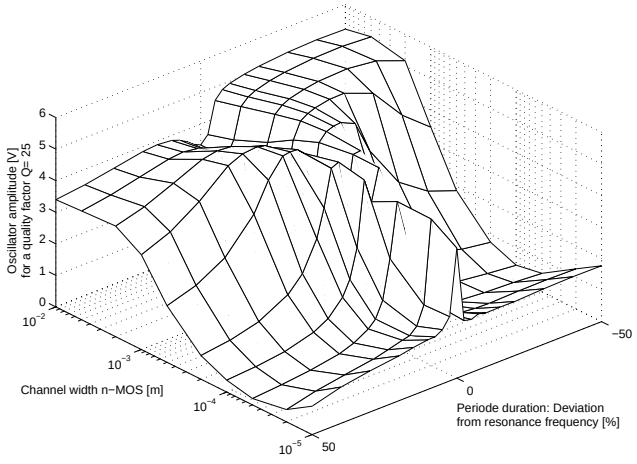

Fig. 8. Two transistor oscillator: Amplitude as function of variation of the control frequency.

the resonance frequency:

$$\frac{f_{resonance,actual}}{f_{resonance,nominal}} = \sqrt{\frac{C_{actual}}{C_{nominal}}} \tag{5}$$

This equation shows, that the deviation in the load capacitance must also be in the range of some percent around the nominal value for a stable operation.

3.2 Two-transistor oscillator

The one transistor oscillator can be expanded to a push-push stage by adding a *p*-MOSFET and the necessary control logic. This stage behaves mostly like the single transistor oscillator previously presented. It can be clearly seen in Fig. 8 that this circuit is also not stable against mismatch between control and resonance frequency or varying the load capacity.

3.3 H-bridge oscillator

If the circuitry needs a sine signal with as well 0° as 180° phase shift, the two-transistor oscillator can be extended to the H-bridge shown in Fig. 9 (Voss, 2001). The main advantages of the H-bridge are the stable phase shift between

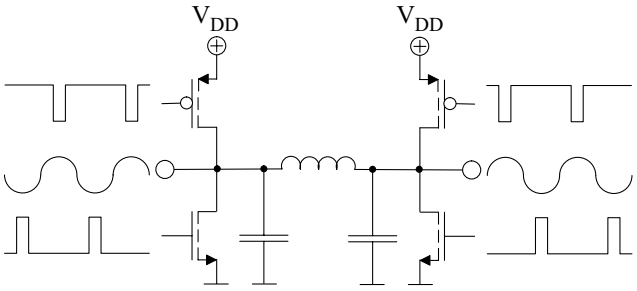

Fig. 9. H-bridge with four transistors.

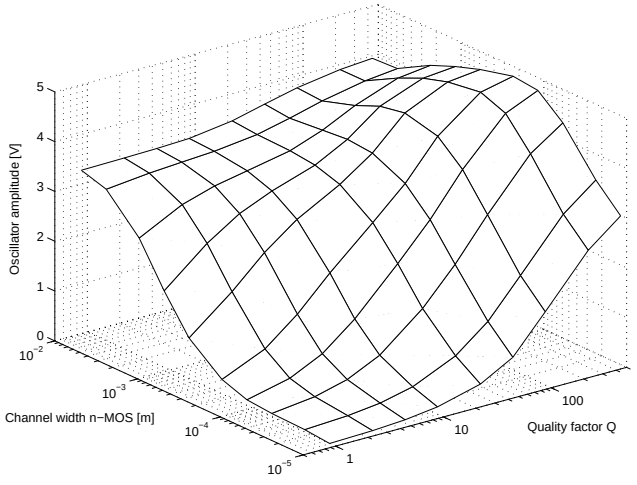

Fig. 10. H-bridge: Amplitude for varying quality factor of the inductor.

the two outputs and the use of only one inductor. The stability against mismatch between control and resonance frequency or variation of the capacitances is even worse compared to both the one-transitor and the two-transistor oscillator (Fig. 8).

4 Controlled resonance circuit

Another approch is the oscillator circuit shown in Fig. 13 (Schlachta et al., 2002; Athas et al., 1996). Contrary to the previous discussed oscillators this resonane cell doesn't oscillate continuously.

We start the discussion of the circuit by assuming that the connected load has to change its state. That triggers the circuit, which behaves like a clocked latch. The actual voltage over the resonance capacitor determines the needed transition and is saved in an RS flip flop in the control logic during the whole transition. The power transistor (depicted as ideal switch) is switched on and starts the resonant process by connecting the inductor to $\frac{V_{supply}}{2}$ This starts a resonant oscillation with an amplitude of also $\frac{V_{supply}}{2}$, achieving a voltage swing between $\frac{V_{supply}}{2} - \frac{V_{supply}}{2} = 0$ and $\frac{V_{supply}}{2} + \frac{V_{supply}}{2} = Vdd$. Therefore it is only necessary to stop the oscillation at the desired voltage level to get the demanded change in the

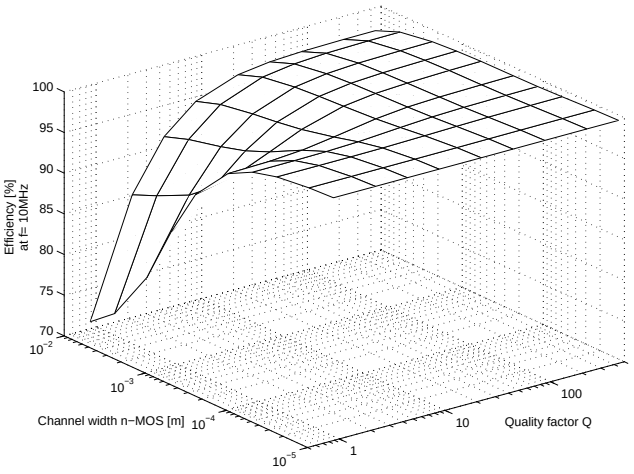

Fig. 11. H-bridge: Efficiency for varying quality factor of the inductor.

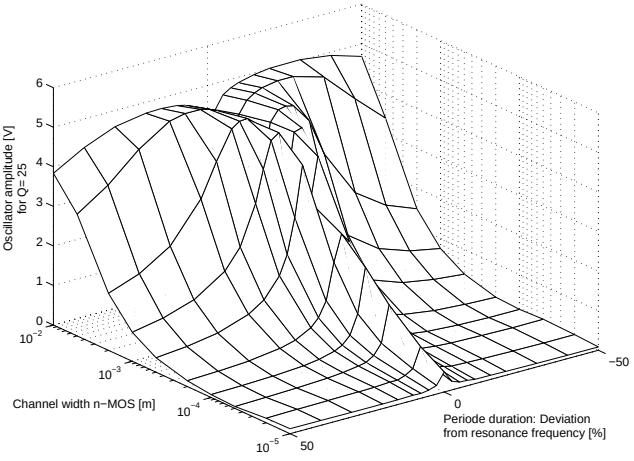

Fig. 12. H-bridge:

voltage of the load. If these levels are the minimum or maximum voltages of the resonant circuit, the inductor contains no energy so that the free wheeling diodes are not needed. A comparator is used to determine the threshold at which the power transistor is switched off. Since there are two thresholds, one for switching from LOW to $HIGH$ and one for switching from $HIGH$ to LOW, two comparators adjusting the switching thresholds are used where the active one is selected depending on the initial value of the resonance capacitor. To ensure constant levels after switching, a tristate buffer is used. This buffer is enabled when the switching cycle is finished and pulls up or down the resonant capacitor, thus compensating the energy and the consequent voltage losses in the resonant ciruit.

Because the resistance of the charging/discharging path influences the energy dissipation in the design (see Eq. 1), the power transistors had to be made very wide. On the other hand, the width of the switching transistors is responsible for the gate capacitance that has to be charged and discharged conventionally each switching cycle, thence dissipating en-

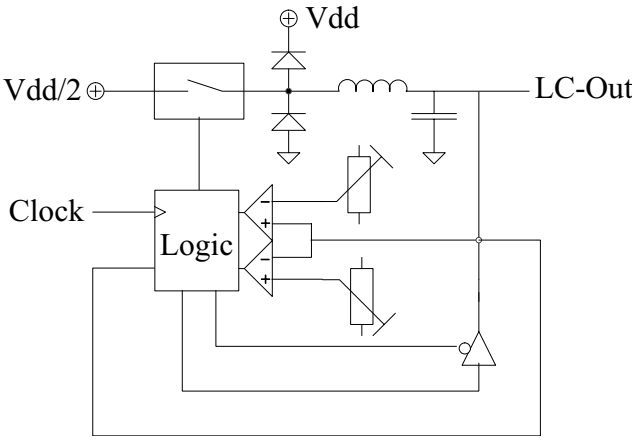

Fig. 13. Controlled oscillator cell.

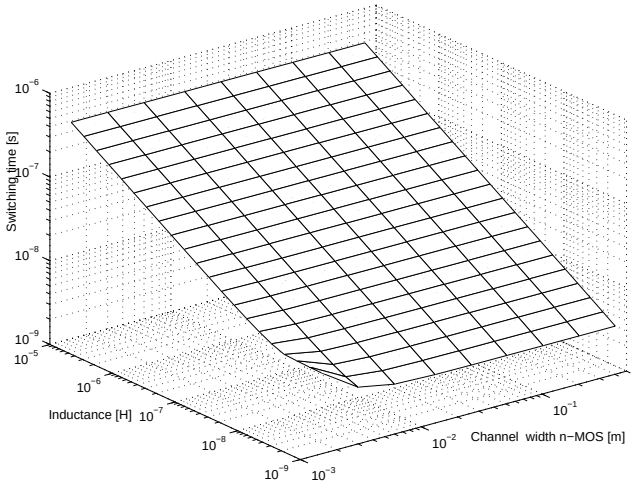

Fig. 14. Controlled oscillator: Switching as function of inductance.

ergy. Thereby, the channel widths of the transistors are a tradeoff between the resistive loss in the resonant circuit especially at full load as well as the switching losses due to the gate capacitance at small load.

Another subject to tradeoff is the value of the resonant capacitor. The resonant capacitor together with the switchable and thereby variable load capacitances forms the resonant capacitance and determines the switching time and thus the slew rate. To achieve a small range of switching time between no load and full load it is necessary and advantageous to use a large additional capacitor (in the range of the maximum load capacitance). The drawback of a large resonant capacitor is that it significantly increases switching losses especially with less load capacitance. As a compromise, the resonant capacitor is sized equal to one third of the maximum load capacitance, achieving a change of $1 : \sqrt{3+1} \approx 1 : 2$ in the switching time between minimum (no load) and full load.

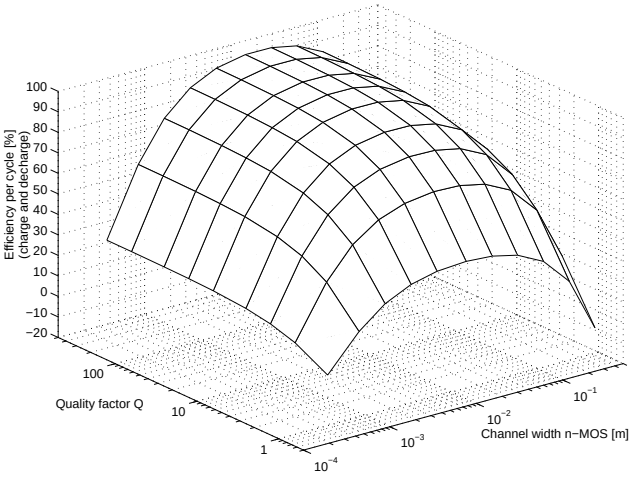

Fig. 15. Controlled oscialltor: efficiency as function of quality factor.

5 Conclusions

Several oscillator designs have been presented. All of these designs have their advantages and drawbacks:

– Multi stage charging is only applicable for limited frequencies; the design without an inductor and the high efficiency makes it a good choice for circuits with lower clock frequencies.

– The one- and two-transistor oscillator and H-bridge have a good efficiency but they all require a nearly constant load capacitance. This limits the application to nets with a constant capacitvie load, e.g. the clock net on a chip.

– The controlled oscillator contains some difficult to implement components like the analog comparators, and the operating speed is limited because of the difficult turn-off detection. On the other hand the ability to drive loads with varying capacity makes it very flexible. Consequently it is a good choice for I/O-buffers and similiar applications.

As a result can be said, that none of the proposed concepts is an optimal choice for all application. Nevertheless, through a careful selection of the oscillator type according to the demands of the load it is possible to find very good solutions for a broad range of applications.

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