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Resonant charging

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Abstract. It has been shown (Athas et al., 1994) that adiabatic switching can significantly reduce the dynamic power dissipation in an integrated circuit. Due to the overhead in the realization of adiabatic logic blocks (Saas et al., 2000) the best results are achieved when it is used only for charging dominant loads in an integrated circuit (Voss and Glessner, 2001). It has been demonstrated (Saas et al., 2001) that a multi stage driver is needed for minimal power dissipation. In this article a complete three stage driver including the generation of oscillating supply is described. To obtain a minimal power dissipation during synchronization the resonant frequency has to be constant. Therefore the waveforms for the logic states of the signal and the realization of a single stage differ from those presented in (Saas et al., 2001). In the H-SPICE simulations losses of the inductor are taken into account. This allows to estimate the power reduction that is achievable in a real system.

1 Introduction

Adiabatic switching (Athas et al., 1994) is a method to reduce the dynamic dissipation of a circuit by charging the capacitances with a time-variant source. The minimal energy dissipation is achieved for a constant charging current.

$$E_{diss} = \frac{RC_L}{T} C_L V_{dd}^2 \tag{1}$$

It has been shown in (Saas et al., 2000) that the realization of general complex logic blocks based on pass transistor logic utilizing adiabatic switching leads to a considerable overhead for maintaining true adiabatic behavior.

Therefore, to avoid this overhead it is worthwhile to consider the energy dissipation associated with dominant load capacitances only, without the inclusion of complex logic. Keeping in mind that usually a large part of the power is dissipated in the I/O-cells of complex chips (Sakurai et al., 1997), a significant reduction of this dissipation can be expected. Since the driver is only a single cell, which can be controlled by standard CMOS logic, it can easily be included into a standard design flow.

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The standard pad driver has to charge the pad as quickly as possible. In particular this time has to be shorter than the clock period T_{clk}. For this reason the $\frac{W}{L}$ of the driving inverters has to be adjusted to keep the channel resistance R_{ch} sufficiently low. The dissipated energy $E_{diss} = \frac{1}{2} C_L V_{dd}^2$ is independent of the channel resistance R_{ch}. Therefore the properties of the transistor do not influence the energy dissipated but only the switching speed of the driver.

To fulfill the speed requirements in most cases an inverter chain is used. The dissipated energy is increased by the additional gate capacitances of the driving inverters in a multiple stage CMOS driver.

The basic idea of an adiabatic driver is very simple. The capacitor is charged through a transmission gate by the phase Φ. The gate is controlled by standard CMOS gates. Both, p and n channel transistors are used to obtain a full voltage swing at the output. Of course the $\frac{W}{L}$ has to be reasonably large as the dissipated energy is dependent on the channel resistance R of the transmission gate (1). Despite the simplicity of the circuit there is a significant saving of energy. The biggest part of the remaining power loss is dissipated in the controlling CMOS gates which charge the large gate capacitances of the transmission gate non-adiabatically. To minimize the losses in the controlling gates, the adiabatic stages can be cascaded. By this, only transistors in the first stage are charged non-adiabatically.

2 The multistage driver

For the present examination a three stage design has been chosen. To find the optimum number of stages is an open problem.

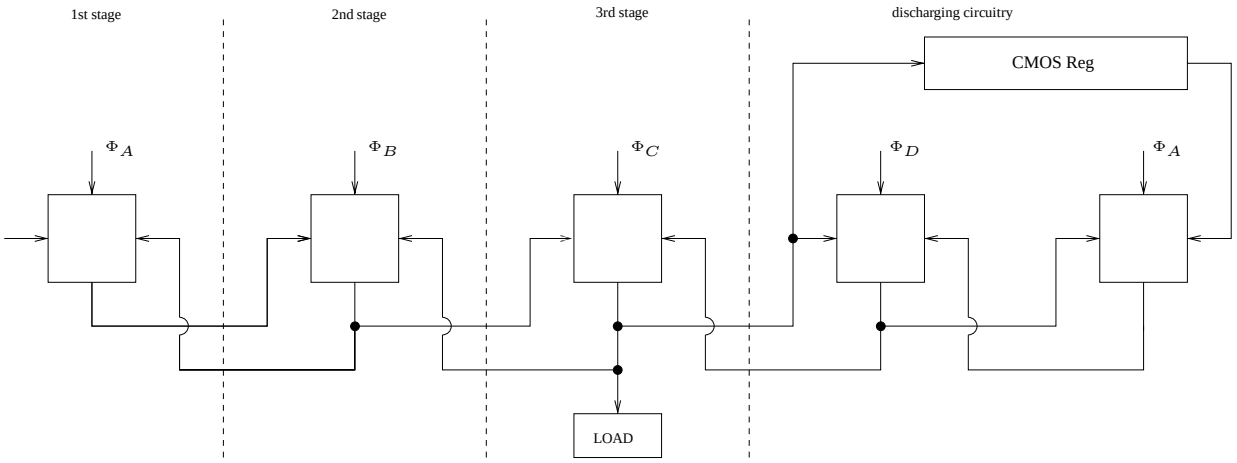

Fig. 1. Schematics for the multi stage driver.

A diagram for a three stage driver is shown in Fig. 1. About half of the energy is dissipated during the discharging process. Therefore, also the discharging has to be done adiabatically. For the discharging process the initial state in the controlling gate has to be present for the whole discharging process (Schlaffer, 2000). So, it is necessary to store this state. Of course, the discharging has to be done with appropriately sized transistors. For discharging the same cascade as for charging is obtained. For the last stage a CMOS register is used to store the state needed for adiabatic discharging. Only the minimal transistors in the register are discharged non-adiabatically, but this energy is negligible.

Four clock phases are used. Each stage is connected to a clock phase which is delayed by a quarter of the clock period to the phase of the predecessor (see Fig. 5). By this the output of the preceding stage is valid during the rising edge. Therefore, the output is well suited as a control signal for the charging of the succeeding stage. On the other hand, the succeeding stage is valid during the falling edge at the preceding stage. Therefore, its output can be used to discharge the output of the preceding stage adiabatically. For the charging of the first stage standard CMOS gates are used. They have to be valid for three quarters of the clock period. The output of a standard CMOS register is used to discharge the last stage. Its state has been set in one of the preceding stages.

Using this timing a three stage driver generates a latency of $\frac{3}{4}T_{clk}$.

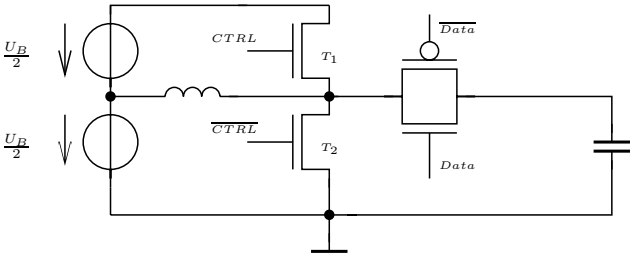

Fig. 2. Oscillator.

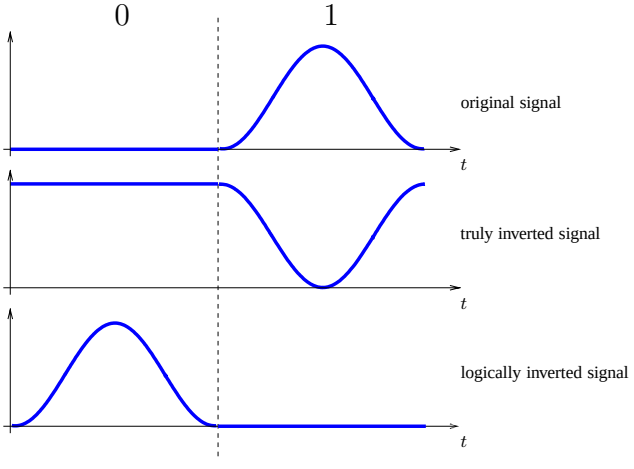

Fig. 3. Waveforms and inverted waveforms.

3 The oscillator

As the generation of ideal ramps is not possible with a high efficiency, they are approximated by a sinus. To generate the sinusoidal power supply, an oscillator is needed. The oscillator (Fig. 2) is a resonant LC oscillator working in class E operation. It is based on (Ziesler et al., 2001) and inherits some advantages when compared to the widely known blip circuit which is often proposed as the source for adiabatic circuits (Athas et al., 2000). It needs only a single inductor for each phase and generates a full sinusoidal voltage oscillation at the capacitor.

The transistors T_1 and T_2 are closed for a short period at the maximum, respectively the minimum, of the output voltage to compensate for losses during one cycle. In addition this keeps the oscillation synchronous to the CMOS clock. Although some work has been published (Ziesler et

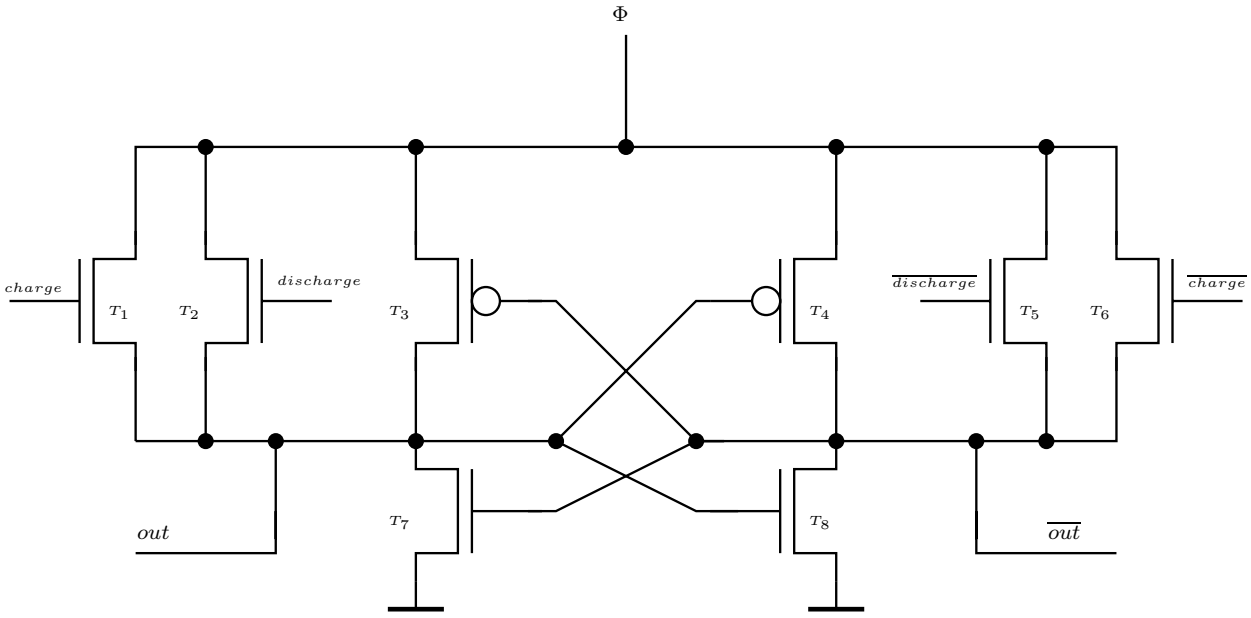

Fig. 4. Circuit of a single stage.

al., 2001), the controlling signals for the T_1 and T_2 are generated manually.

4 Different waveforms for the logic states

The idea of the adiabatic driver is to charge the output with the oscillating power supply in case of a logical 1 and to cut it off in case of a logical 0. A logic 1 will result in one period of the oscillation at the output. It starts and ends in the minimum of the sinus. The DC offset as well as the amplitude of the oscillation is $\frac{V_{dd}}{2}$.

As already mentioned above, dual rail encoding is required. There are two ways to invert the signal, which will be named "truly inverted" and "logically inverted". They are depicted in Fig. 3

If the original waveform is inverted, a signal which is at V_{dd} for a logical 0 and sinusoidal for a logical 1 is obtained. This signal would be the perfect one to control the p-MOS transistor of the transmission gate in the previous and the subsequent stage. The drawback of this solution is, that one can not combine the original and the inverted signal to a DC and a sinusoidal one just by switching between them. This is needed to present a constant load to the oscillator. Since the load capacitance is part of the resonator and therefore has a direct influence on the operating frequency it is mandatory to keep it constant for all logic states of the circuit. To achieve this, there has to be a constant sinusoidal oscillation on a constant number of load capacitances. Therefore, an "logically inverted" output is used. During a logic 1 the output will oscillate and the inverted one will stay at 0 Volt. For the logic 0 it is vice versa. If only a logically inverted signal is created at the output of each stage, there is no signal available which is suitable for controlling the p-channel transistors in the other stages. Therefore, the individual stages of the driver have to be redesigned.

Table 1.

$\frac{1}{2}CU^2$	350.00 $\frac{pJ}{Bit}$
CMOS	351.52 $\frac{pJ}{Bit}$
adiabatic driver at 1 MHz	52.70 $\frac{pJ}{Bit}$

5 A single stage

It is well known, that a p-channel transistor is needed to obtain a full charging up to V_{dd}. If only a n-channel transistor is used, it is only conducting until V_{GS} is larger than V_{th}. Therefore, the source voltage can only reach $V_{dd} - V_{th}$. If one has a look at the waveform of a logical "1", one can see, that the p-channel transistor is only needed during a rather short period. The basic evaluation of the input of a single stage is done by the n-channel transistors. It seems to be a good idea to abandon the signal to control the p-channel transistors and use some internal signal which already reached its final level due to the n-channel transistors instead.

Such a solution is proposed in Fig. 4. It consists of 2 n-channel transistors per output signal (T_1, T_2 and T_5, T_6). One is used to charge the output, and the other one for discharging. The charging signal is "delayed" by $-\frac{T}{4}$ whereas the discharging signal is delayed by $\frac{T}{4}$.

There is only one p-channel transistor per output signal (T_3, T_4). If the output is logical 1 it has to be conducting

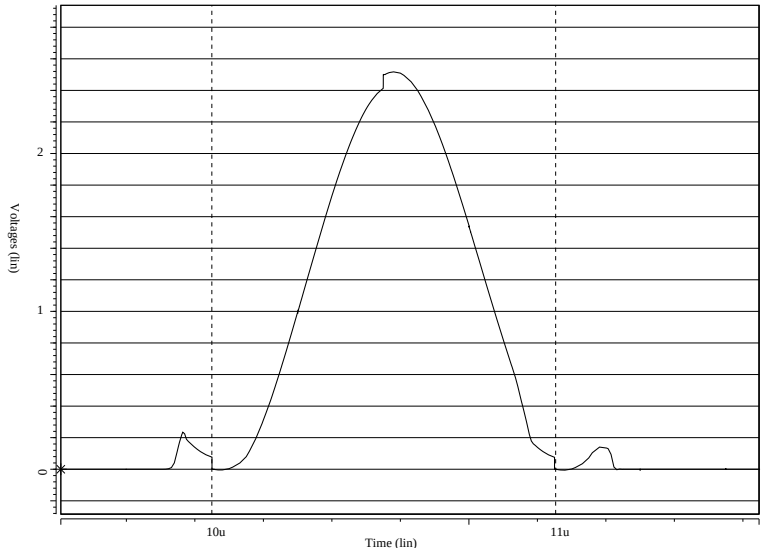

Fig. 5. Simulated output waveform.

during the maximum of Φ. On the other hand, it has to be non-conducting for $U_\Phi > V_{th}$ in the case of a logical 0.

This behavior can be achieved by controlling the p-channel transistor with the inverted output. The n-channel transistors T_7 and T_8 ensure the output signal to be 0 V for a logical "0". They are not present in stage 3, as the load capacitor is large enough to achieven a stable output.

6 Simulation results

The adiabatic multistage driver has been simulated using a 0.25 μm process and H-SPICE. As the inductor is intended to be an external one, a Q value of 100 seems to be realistic.

A driver for 4 off-chip connections has been simulated. Each of the connections represents a load of 28 pF. The adiabatic drivers are implemented to load one output at a time. Thus a group of 4 drivers represents a constant data independant load to the oscillators for all times.

The simulations results show that the circuit is working adiabatically. The driver dissipates much less energy than a conventional CMOS driver at useful operating frequencies. It has to be noted, that these results summarize the whole energy that is dissipated including the generation of the sinusoidal power supply.

7 Summary and outlook

In this paper a multi stage adiabatic driver has been presented. An oscillator has been chosen to generate the sinusoidal power supply. To ensure minimal losses during the synchronization to the CMOS clock the oscillator has to work on a constant load. The single stages of the driver have been designed to fit the requirements for constant load. To avoid the need for truly inverted signals the p-channel transistors which are needed to reach V_{dd} are realized as clamping devices. The simulation results show a pretty large potential for adiabatic drivers. Although a small latency of $\frac{T}{4} * \mathit{Num.\ of\ stages}$ is introduced the energy savings still make this concept interesting for a number of applications. Of course high speed applications are not the aim for adiabatic circuits, but the simulations have shown that reasonable operation is possible up to 100 MHz.

Further research has to be done on the modeling of the load and the other off-chip connections. Most probably the results can be improved by more advanced methods for the transistor sizing.

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