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Resonant 90 degree shifter generator for 4-phase trapezoidal adiabatic logic

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Abstract. Many adiabatic logic families make use of multi phase trapezoidal or sinusoidal power clocks to recover the energy stored in the load capacitances. A key aspect for the evaluation of the performance of adiabatic logic is then the study of a system that includes the power clock generator. A four-phase trapezoidal power clock generator, according to the requirements of the most promising architectures, namely the ECRL and PFAL, has been designed and simulated. The proposed circuit, realized with a double-well 0.25 μm CMOS technology and external inductors, is a resonant generator designed to oscillate at a frequency of 7 MHz, which is within the optimum frequency range for adiabatic circuits realized with this CMOS technology. The generator has been simulated with the equivalent load of fifty 1-bit adders and the operating behavior of a 4-bit adder has been evaluated. The key aspects of a generator for adiabatic logic are its power consumption and the phase relationships between its output signals. The proposed generator has a conversion efficiency higher than 80%, and it is robust with respect to variations of technology parameters. The four power supplies exhibit the correct relationship of phase also in the presence of no equally distributed loads.

1 Introduction

Power consumption is a crucial requirement of present and future circuits and systems since the increasing demand of portable electrical applications makes the tradeoff of computing power versus battery life time more critical. Furthermore, the number of gates per chip area is constantly increasing, while the gate switching energy does not decrease at the same rate, so power consumption rises and heat removal becomes more difficult and expensive. Then, to limit the power consumption, alternative solutions at each level of abstraction are proposed.

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In static CMOS, any circuit can be described as a load capacitor and two switches that connect it alternately to the power supply or to ground, and hence abruptly modify its voltage. If the constant power supply is replaced by a time variable power clock, with a rise time longer than the time constant of the charging path (Athas et al., 1994), the switching operation can be accomplished with ideal vanishing dissipation. Furthermore, when the capacitor is connected to the decreasing power clock, its charge flows back to the power source. Circuits that fulfill the low power requirements recovering the energy through time variable power supplies (power clocks) are called "adiabatic". In literature, choosing different power clocks and methods to control the switching, many multi-phase adiabatic families have been proposed by exemplifying the operating principle with simple circuits and emphasizing the energy saving with respect to standard CMOS. Although these studies illustrate important aspects of the logic circuits, they usually are not comprehensive since the energy dissipated in the DC/AC converter that generates the multi-phase clock is often not taken into account. In some papers the converter is not considered ideal, but the designed solutions have not very high efficiency (Moon and Jeong, 1998) or the generated signals differ from the optimal waveform for the adiabatic circuits (Maksimovic and Oklobdzija, 1995; Moon and Jeong, 1996, 1998).

We believe that a key aspect in the evaluation of the potential of adiabatic logic families is the performance of a complete system, including the power clock generator and the interface with conventional CMOS logic. In this paper, a high efficiency power supply generator is presented, which can be used for logic circuits implemented using three adiabatic families, namely ECRL (Moon and Jeong, 1996, 1998), PFAL (Vetuli et al., 1996; Blotti et al., 2000), and 2N-2N2P (Kramer et al., 1995; Liu and Lau, 1998). These families require, as power supplies, four trapezoidal waveforms equally spaced in phase.

The paper is organized as follows: in Sect. 2 some oscillators proposed in literature are overviewed, illustrating advantages and drawbacks of each architecture. In Sect. 3 the

new oscillator and its amplitude and frequency expressions are introduced. In Sect. 4 the simulation results, such as conversion efficiency and sensibility to parameter variations, are reported. In Sect. 5 an alternative solution is evaluated.

2 Overview of adiabatic oscillators

The main requirements for a DC/AC converter for adiabatic circuits are the capability to recover the energy stored in the load capacitances, and a high power-conversion efficiency, defined as the ratio of the load power to the total DC supply power. Oscillators based on LC resonant circuits can meet these requirements, and therefore ensure that the complete adiabatic system provides significant power saving with respect to its standard CMOS counterpart. In the few schemes appeared in the literature, the adiabatic logic is usually represented by its equivalent load, i.e. a resistance R_e and a capacitance C_e. In the 1N single-phase power clock generator (Maksimovic and Oklobdzija, 1995) (see Fig. 1) an inductance L connects the DC power supply to the logic, that has a nMOSFET in parallel. The oscillator generates only one sinusoidal phase φ_0 and needs a square waveform control signal ctr. The output φ_0 has the same frequency as the control signal, and its amplitude is determined by the ctr duty cycle. When the output signal frequency is close to the resonant frequency, the generator has a conversion efficiency around 70%.

In Fig. 2 is reported the 2N2P two-phase power clock generator (Maksimovic and Oklobdzija, 1995; Moon and Jeong, 1996, 1998; Ye and Roy, 2001), which provides two sinusoidal clocks and requires only one inductor. If control signals are external, the frequency is easily enforced and with some additional circuitry two oscillators can be merged into a 4-phase generator. In this case, the conversion efficiency is around 40–50% (Moon and Jeong, 1996).

Because the adiabatic loads driven by the oscillator outputs are different and time variable (Kim et al., 2001), the circuit cannot be completely balanced with external capacitances, therefore a phase error up to 5% may occur in the output waveforms. If outputs are used as internal control signals, i.e. if $c_1 = \varphi_1$ and $c_2 = \varphi_2$, the circuit complexity and occupied area are reduced, but also the conversion efficiency decreases (Liu and Lau, 1998).

3 Shifting oscillator

The oscillator proposed in this paper is realized as a ring of four low-power 90-degree shifters, as shown in Fig. 3. Each shifter is realized with a CMOS inverter and an LC resonant circuit, so that the energy is transferred between reactive elements while the DC power supply only delivers the energy dissipated on the resistance and on the diodes.

Each output of the oscillator drives a stage of the adiabatic circuit, represented in Fig. 3 by its equivalent load, i.e. a resistance R_e and a capacitance C_e. The inductors are external to the chip. The output amplitude regulation between

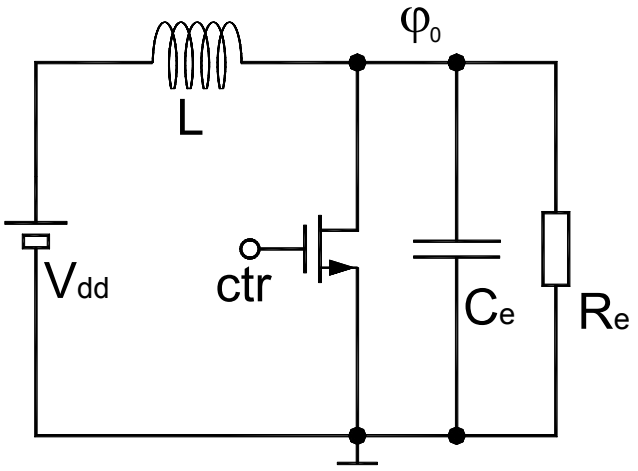

Fig. 1. The 1N generator.

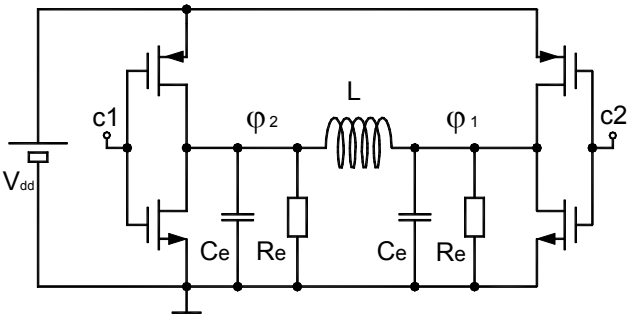

Fig. 2. The 2N2P generator.

0 V and V_{dd} is achieved with Schottky diodes, whose low V_γ ensures moderate energy dissipation when diodes are in conduction. The proper configuration of the reactive elements provides the required phase delay. Therefore, when the circuit oscillates, the four outputs have the same frequency and a quarter-period shift, as required by the considered adiabatic architectures.

To properly dimension the elements of the oscillator, let us consider its analytical transfer function. The ring transfer function is the product of four identical single-stage transfer functions, therefore Barkhausen criterion is met when a single-stage transfer function has a gain equal to 1 and a phase delay equal to $k\pi/2$. In a small signal approximation, the expression of a single-stage transfer function is:

$$\frac{\varphi_1(s)}{\varphi_0(s)} = \frac{-R_e r_{ds}\,(g_{mp} + g_{mn})}{r_{ds} + R_e + (L + r_{ds}\,R_e\,C_e)\,s + R_e\,C_e\,L s^2} \tag{1}$$

where r_{ds} is the small signal output resistance of the MOSFETs, and g_{mp} and g_{mn} are the pMOSFET and nMOSFET transconductances, respectively. By enforcing a phase of $3\pi/2$, we obtain the following expressions for the frequency and for the gain value:

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{r_{ds} + R_e}{R_e\,C_e\,L}} \simeq \frac{1}{2\pi}\sqrt{\frac{1}{C_e\,L}} \tag{2}$$

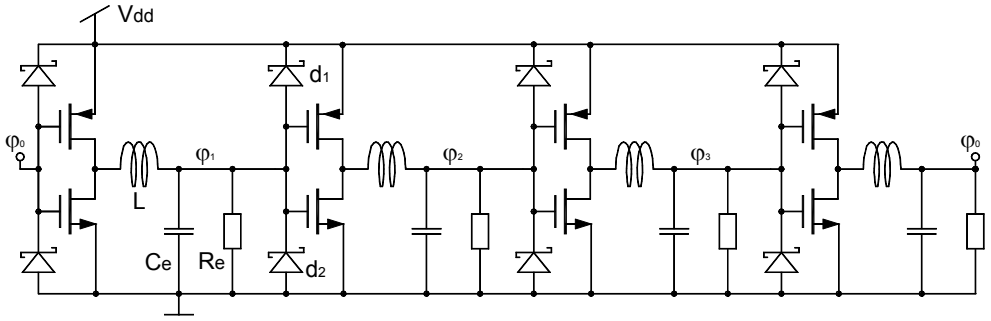

Fig. 3. Schematic of the 4-phase shifter oscillator.

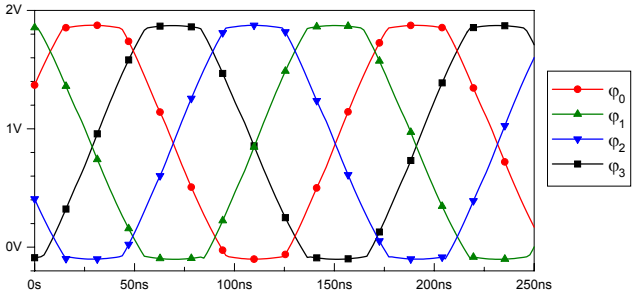

Fig. 4. Waveforms of the 4-phase power clock generator.

$$\left|\frac{\varphi_1}{\varphi_0}\right| = \frac{R_e\, r_{ds}\,(g_{mp} + g_{mn})}{L + r_{ds}\, R_e\, C_e} \sqrt{\frac{R_e\, C_e}{(r_{ds} + R_e)\, L}} \tag{3}$$

In our simulation, a standard double-well 0.25 μm CMOS technology and a DC supply voltage of 1.8 V are considered. R_e and C_e are chosen as the equivalent impedance seen by the power supply of fifty 1-bit adders, so R_e is 2 $M\Omega$ and C_e is 500 fF. Since the considered adiabatic families with this technology process have the optimal frequency range between 1 and 10 MHz (Amirante et al., 2001), the clock frequency is chosen equal to 7 MHz. From Eq. (2), the inductance value is derived to be equal to 1 mH. Since the transfer function is based on a simplified circuit that does not consider the effect of diodes, the gain value must be larger than 1 to ensure oscillation. Nevertheless high gain values lead to square waveforms and to longer period of diode conduction, therefore the optimum gain is found between 1.5 and 3. To reduce dissipation on the channel resistance, the pMOSFET W/L ratio is 10 times larger than of the nMOSFET W/L.

4 Simulation results

The circuit functionality has been simulated with PSpice. The conversion efficiency η, defined as the ratio of the energy dissipated on the load to the total energy delivered by the DC supply, is one of the most important parameters of the generator, since energy dissipation is the main concern of adiabatic architectures. The oscillator, driving the equivalent load of the adiabatic system (R_e, C_e), shows a conversion efficiency of 85%. The time relationship among the power clock phases is another important specification, since between the input signals and the power clock a 90 degree delay must be present . The phase error is defined as the distance in degrees between the real waveform and the theoretical one. In the nominal conditions the proposed oscillator has a maximum phase error of 0.9 degrees.

The threshold voltages of the n- and p-MOSFETs are V_{Tn} = 0.44 V and V_{Tp} = −0.43 V, respectively. Increased efficiency can be obtained with higher threshold voltage devices. For this reason, also the possibility to develop the circuit with high V_T MOSFETs has been considered, and the simulation results with $V_{Tn} = -V_{Tp} =$ 0.9 V are presented.

To evaluate not only the conversion efficiency of the oscillator, but also to evaluate the quality of the generated power clocks, a more complete adiabatic system is simulated. The system is made up of the proposed oscillator, of the synchronizers for the external inputs (Fischer et al., 2002), and of a 4-bit pipelined Ripple Carry Adder realized in ECRL logic. With this load the oscillator presents a conversion efficiency of 82.3% with the high V_T MOSFETs, and of 75.6% with the normal V_T MOSFETs. In both cases the output waveforms are close to be trapezoidal and exhibit the correct relationship of phase (Fig. 4).

The power conversion efficiency has been evaluated when variations of the value of a single reactive parameter occur. Since the inductances are external elements characterized by a tolerance range around the nominal value, our simulations take in account the worst case of technological parameter shift, whereas the capacitive load on each phase is determined by the logic function that the phase itself drives, and its value is usually a function of time, therefore the simulated capacitor conditions must predict the behavior of the circuit in case of the worst operating variations.

The simulation results reported in Table 1 are obtained modifying the value of one reactive element in a single shifter stage (whose modified value is reported in brackets), and leaving unaltered the values of all other reactive parameters.

Using high V_T devices, a 30% variation of one capacitance value causes a reduction of the conversion efficiency of less than 2.3%, while the frequency variation is less than 3%. With a 30% variation of the value of a single inductance, the efficiency is reduced by less then 1%, and the frequency variation amounts to 5%. The phase error of the oscillator

Table 1. Simulation results of the oscillator driving the adiabatic logic gate implemented with high (left) and low (right) V_T MOSFETs

V_T [V]	L [mH]	C [fF]	η [%]	f [MHz]	V_T [V]	L [mH]	C [fF]	η [%]	f [MHz]
0.9	1	500	82.3	7.13	0.4	1	500	75.6	7.14
0.9	1	500 (650)	80.0	6.94	0.4	1	500 (650)	74.0	6.94
0.9	1	500 (350)	81.9	7.35	0.4	1	500 (350)	75.2	7.40
0.9	1 (1.3)	500	81.4	6.93	0.4	1 (1.3)	500	72.9	7.96
0.9	1 (0.7)	500	81.6	7.48	0.4	1 (0.7)	500	74.0	7.54

with the nominal load presents is only 1 degree, while its worst case performance in presence of parameter variations amounts to 5.8 degrees. The oscillator with high V_T devices is therefore not only characterized by higher efficiency value than the solution with low V_T devices, but also by better robustness against parameter variations.

5 Alternative solution without Schottky diodes

Since Schottky diodes are not usually available in a standard CMOS process, alternative solutions have been investigated, in particular, the possibility to replace the diodes with MOSFETs. In this alternative design, the diodes *d1* and *d2* (Fig. 3) are replaced by a pMOSFET and a nMOSFET, respectively, with their gates connected to their sources. The conversion efficiency of this solution simulated with an equivalent load amounts to 76%, instead of the 85% obtained with the Schottky diodes. Moreover, this implementation also exhibits other drawbacks: the clipping of the output waveforms is not accurate, therefore the power-clocks reach voltages lower than 0 V and higher than V_{dd} (-0.7 V; 2.6 V), and the waveforms are almost sinusoidal rather than trapezoidal. To reduce these effects, the diodes are replaced by low V_T MOSFETs (V_T = 0.2 V) whose sources are connected to voltage references ($V_{ref,p}$ = 1.3 V; $V_{ref,n}$ = 0.5 V). In this case, the efficiency amounts to 76%, and the dynamic range of the power supplies is comparable to the results obtained with the implementation using Schottky diodes (-0.3 V; 2.1 V).

6 Conclusions

A high conversion efficiency oscillator capable to generate the 4-phase trapezoidal power-clocks required by many adiabatic logic families has been presented. The generator utilizes Schottky diodes and shows operation at 7 MHz, which is within the optimum frequency range for the considered 0.25 μm CMOS technology. To evaluate the performance of a complete adiabatic system, the oscillator has been simulated driving a pipelined 4-bit adder. The generator produces almost trapezoidal output signals, without the need for any auxiliary control circuit, and it has a conversion efficiency higher than 80%. The robustness to technological and operational parameter variations has been characterized. In case of a 30% variation of a reactive element value, the conversion efficiency decreases only by 2%, while the frequency variation amounts to less than 5%. In addition, the generator exhibits a low energy dissipation even if the load capacitances are not equally distributed on the phases. To avoid the use of Schottky diodes, an alternative solution using low V_T MOSFETs has been discussed, together with its cost in terms of circuit complexity. In this case, the conversion efficiency amounts to 76%. The proposed oscillator, with its high efficiency and its almost ideal trapezoidal waveforms, gives to the adiabatic logic the possibility to compete with static CMOS logic in low power applications.

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