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ESD compact-simulation: investigation of inverter failure

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Abstract. An ESD failure occurring inside the core circuitry known as "inverter failure" will be presented and analysed in this paper. The compact model utilised for this investigation is shortly presented. It will be shown that not only properties of the failed structure are relevant, but also surrounding circuitry. So the gate of an inverter will be connected during the simulations in diverse ways to V_{DD} and V_{SS}. The different possibilities of influence of pre drivers can be appraised in this way. In order to achieve a detailed understanding of the individual failure, it is necessary to include ambient circuitry as well as parasitics like resistors and capacitances.

1 Introduction

Susceptibility to Electro Static Discharge (ESD) increases with the shrinking feature size of VLSI technology. The circuit elements which are connected directly to the pads are particularly endangered and have to be protected. ESD protection structures are present in every modern IC which wouldn't survive without these measures. ESD protection elements are placed in parallel to susceptible structures in order to divert the stress current and to clamp the node voltage to safe values. Nevertheless the protected elements have to be considered particularly as they still represent a possible path for the discharge current. With the growing complexity of IC's associated with an increasing ESD sensitivity the optimization of ESD structures requires a high effort. The behaviour of complex systems under ESD stress is difficult to predict even for ESD engineers and requires a huge level of expert knowledge. Circuit simulation helps to close this gap between huge circuit complexity and understanding of circuit behaviour during discharge. Even apparently simple structures can behave in different ways due to interaction with surrounding circuitry. It is important to find critical structures in circuit architectures even before production of IC's or construction of libraries and to accelerate search of causes of failed elements. In this paper, a well known failure will be investigated which has also been addressed in the literature (Chaine et al., 1997; Krakauer et al., 1994; Puvvada and Duvvury, 1998). Despite correct protection structures circuit elements parallel to protections may be damaged by ESD. It has been observed that the nMOS of an inverter fails for a particular setup of an inverter. Especially nMOS of inverters with pMOS with a large channel width are susceptible. It will be shown that the surrounding circuitry plays an additional role and influences the failure of the inverter. The investigation of the inverter failure will be shown in Sect. 3. The compact model is presented in short terms in Sect. 2. A conclusion is given at the end of the paper.

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2 Compact model

The behaviour of an ESD stressed MOSFET can be ascribed to the turn-on of the parasitic bipolar transistor, caused by avalanche multiplication at the drain diffusion space charge region. A combination of a standard MOS model with a bipolar model extension is already presented in Wolf et al. (1998). The MOS model describing the FET behaviour in the normal operating regime and additional lumped elements describing the FET behaviour during ESD are included in the compact model used to investigate circuitry under ESD stress. Beside two exemplary simulations, Soppa et al. (2002) describes the implementation of this model in a proprietary simulator. Basically, a few elements determine the high current behaviour of the FET which are illustrated in Fig. 1. The bipolar transistor is implemented using the Ebers-Moll model (Ebers and Moll, 1954). This model also includes capacitors, which are mainly necessary for the simulation of the transient behaviour.

The IV-characteristic of a grounded-gate-nMOSFET (ggnMOS) can be divided into four regions shown in Fig. 2. Up to a certain voltage, the reverse current of the drain-bulk junction can be observed (region 1). Due to a high electric field in the space charge region, charge carriers are generated, the

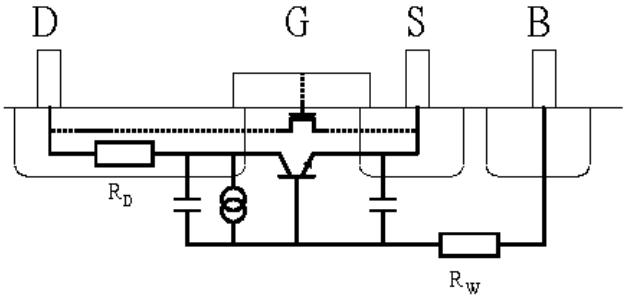

Fig. 1. Profile of nMOSFET with parasitic elements implemented in SQ3.

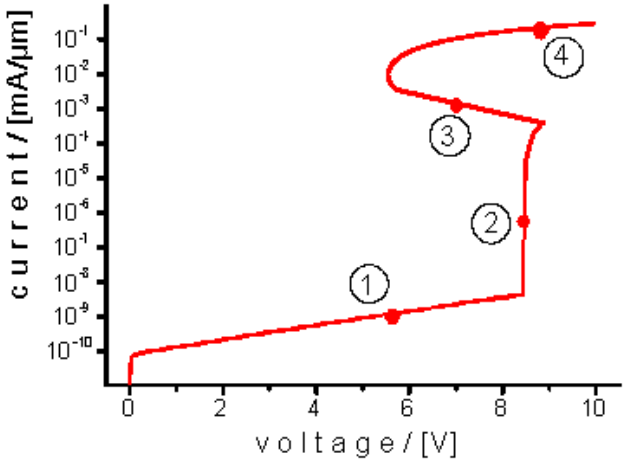

Fig. 2. High-current behaviour of ggnMOS: **1.** reverse current, **2.** avalanche generation, **3.** snapback, **4.** high current regime

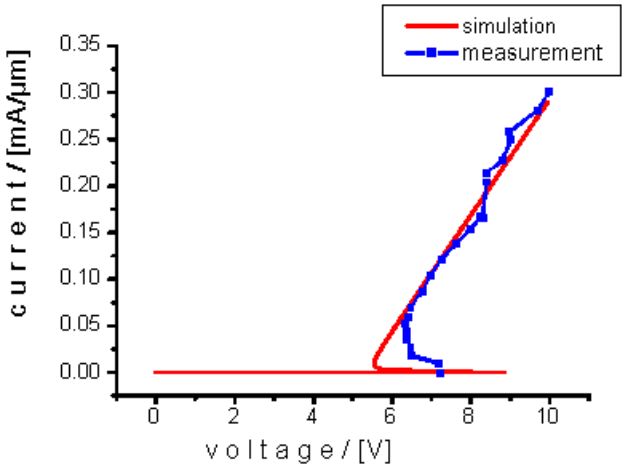

Fig. 3. Simulation and measurement of high current regime.

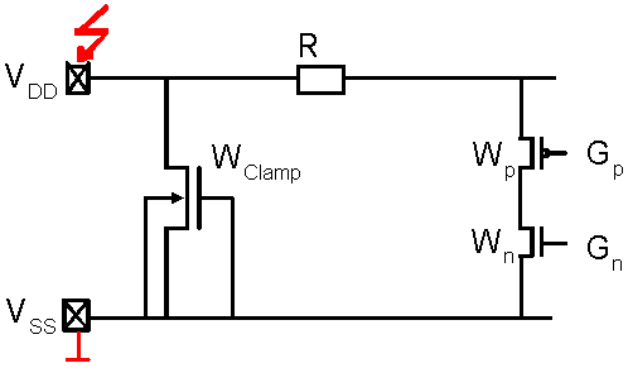

Fig. 4. Schematic of investigated inverter structure.

current (region 2) increases and causes a voltage drop across the well resistor R_W. If this voltage drop is high enough (∼0.7 V) to forward bias the base emitter junction of the bipolar transistor, the voltage snaps back (snapback) to the hold voltage (region 3). When the bipolar transistor is activated, the high current behaviour (region 4) is determined by the diffusion resistor R_D. Simulation of snapback is mainly achieved by implementing the bipolar transistor, the current source I_{ava} and the resistor R_W.

Measurement and simulation of the high current regime are shown in Fig. 3. The measurement of the high current characteristic is done step by step with short pulses (Amerasekera and Duvvury, 2002) for diverse current levels.

3 Inverter failure

Many fails discussed in literature are caused by turn on of parasitic elements like pnpn structures (Amerasekera and Duvvury, 2002). In contrast failures where breakdown of parasitic elements is not observable are also mentioned in literature. Here the local distances of guardrings, diffusions etc. play a secondary role. Design properties like finger width of transistors are important and make it possible to investigate the failure mechanisms by compact simulation. In new technologies it can be observed that nMOS of inverters with large pMOS are susceptible to ESD discharge. This chapter presents some basic examinations of the behaviour of an inverter parallel to an ESD protection element during ESD stress. The basic schematic of the investigated inverter structure is shown in Fig. 4.

The worst case will be investigated in the following simulations. A V_{DD} Pad is stressed positively (2 kV HBM) with a grounded VSS Pad, so that the ESD Protection element (Clamp) is operating in breakdown mode with a higher voltage drop than in its diode mode. In this stress mode the nMOS goes into breakdown and determines the triggering behaviour of the inverter path. The ESD pulse can take two paths from V_{DD} to V_{SS}: through the clamp and through the inverter. The high current characteristics of the inverter nMOS and the Clamp are shown in Fig. 5. The two possible paths have a low resistance in the high current regime, so that the current distribution depends strongly on the triggering behaviour of the paths.

With additional series resistors like a pMOS or bus resistances, the Clamp triggers first and shunts the main current. Different setups will be simulated to examine the behaviour

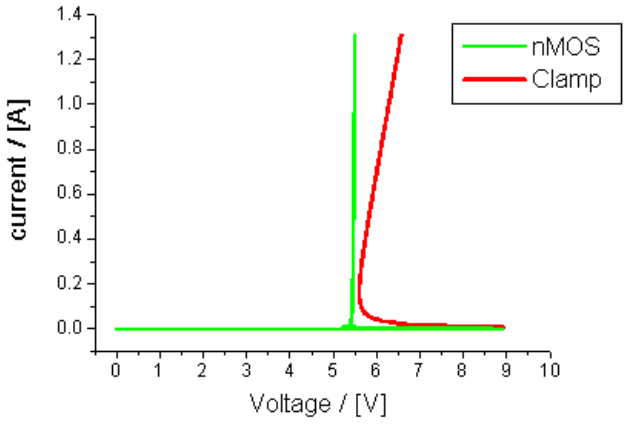

Fig. 5. High current characteristic of nMOS and Clamp.

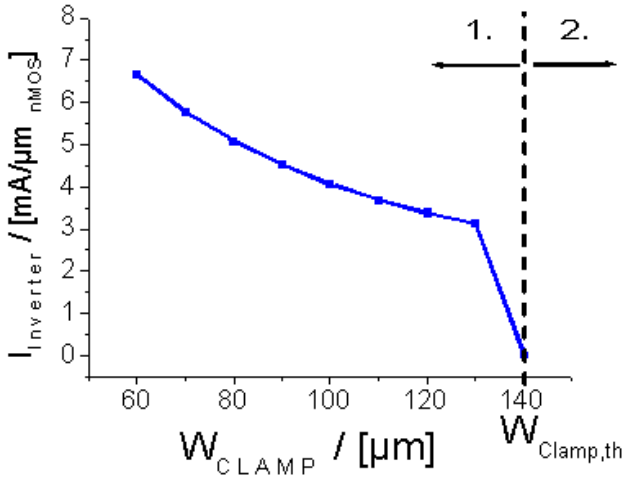

Fig. 6. Dependence of W_{Clamp} on inverter current.

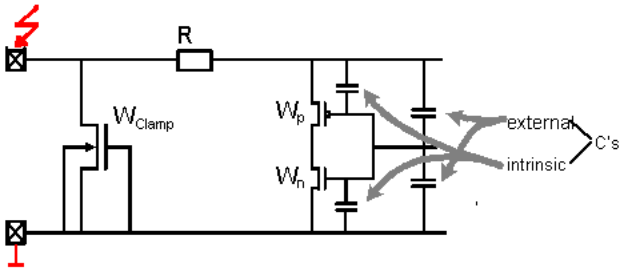

Fig. 7. Setup with intrinsic and external capacitors.

of an inverter during ESD stress. The gate potential of the inverter transistors can be torn to different levels during an ESD pulse. Therefore they are not connected in Fig. 4. For sake of simplicity the pre drivers being also responsible for the gate potential are not included to the following investigations.

In the first investigation the gates are connected to V_{SS}, so that the trigger mechanisms can be explained. The snapback of the inverter is invoked by avalanche multiplication, if the gate is connected to the bulk-node of the nMOS (grounded gate). Additional displacement currents also influence the triggering. The voltage drop at the inverter is essential for triggering of the nMOS. In other words, a good clamping behaviour of a protection device can be inhibited by additional voltage drop in the main current path due to resistors or diodes. If the voltage exceeds the trigger voltage, the nMOS triggers and current can flow through the inverter getting low ohmic. During ESD stress the voltage drop at the inverter and the inverter current are determined by the width of the clamp (W_{Clamp}). Figure 6 shows the influence of W_{Clamp} on the inverter-current $I_{Inverter}$. The threshold width $W_{Clamp,th}$ divides this graph into two regions:

– Region 1: current through inverter

– Region 2: no inverter current

A good clamping behaviour is achieved using a clamp with a high width and a low resistance in the high current regime. The trigger-threshold is not attained and thus no current flows in the inverter. Reduction of W_{Clamp} does not show an influence until W_{Clamp},th is reached. The current is increasing suddenly if W_{Clamp} is falling below $W_{Clamp,th}$. Further reduction of W_{Clamp} increases the current continuously. The width of the pMOS additionally influences the current through the inverter. Despite a good clamping behaviour of the power clamp, current can flow through an inverter if the resistance of the pMOS is low enough. Equivalent results are obtained if the pMOS is replaced with a resistor. In this case, variation of the resistor is equal to variation of the pMOS width. Transient effects play a role as well as the reduction of the series resistance in the inverter path.

Normally the potential of the gate during an ESD event is between V_{SS} and V_{DD}. In the following investigation the gate potential is determined by lumped capacitances. An investigation of the impact of the gate potential on the current through the inverter will be done in this chapter. As the gate voltage increases by capacitive coupling, the nMOS is in on-state before reaching the breakdown voltage. The gate potential will be determined by the capacitors connected from the gate to V_{DD} or V_{SS}. This setup corresponds to a circuit where the transistors connected to the gate are turned off. It should be recognized that potentials are not constant values, but adjusted during ESD pulse due to capacitors and resistors. Two setups are simulated in this investigation. In one case the gate potential is determined by the intrinsic diffusion-well capacitance of the pMOS, in the other case the gate potential is fixed by capacitors outside the transistor. These two setups differentiate whether external capacitors or intrinsic capacitors dominate the gate potential. The schematic with intrinsic and external capacitors is depicted in Fig. 7.

In addition to the ESD protection element, the width of the pMOS and the gate potential plays an important role, which is investigated in this chapter. The high current regime resistance of the inverter path with triggered nMOS is defined

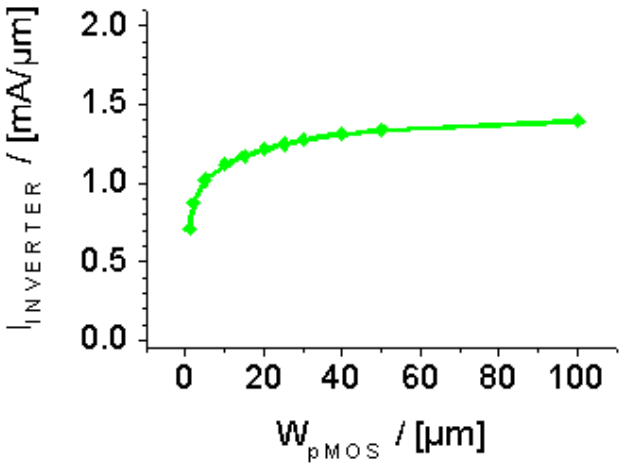

Fig. 8. Inverter current with intrinsic capacitors controlling the gate voltage.

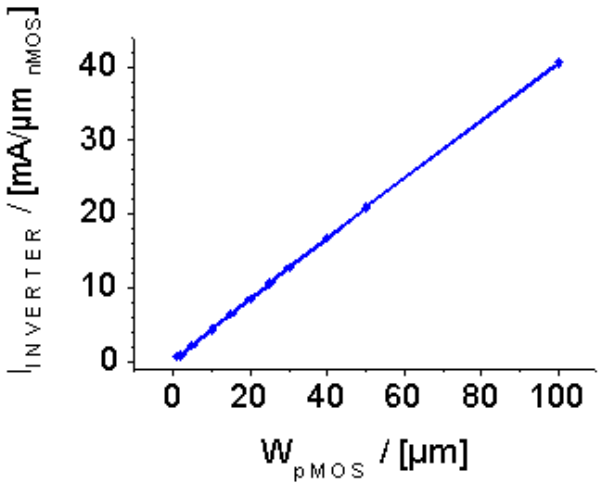

Fig. 9. Inverter current with external capacitors controlling the gate voltage.

by the width of the pMOS and by the gate potential of the pMOS. A high gate potential or a low pMOS width restrain the discharge current through the inverter during ESD stress. Figure 8 shows the influence of pMOS width on the current through the inverter. In these simulations the intrinsic capacitors determine the gate potential. The current doesn't show the expected linear increase with the width.

Two effects influence this behaviour. Increasing the width of the pMOS, the current should increase linearly. The deviation of the curve shown in Fig. 8 from the expected characteristic is caused by the increase of the gate-source capacitance with the width of the pMOS. Due to this capacitance the gate potential approaches the V_{DD} potential and the pMOS is driven into its blocking-state. In this case the gate voltage limits the current through the inverter. With large external capacitors at the gate of the inverter the gate voltage doesn't depend on the pMOS width anymore. The expected linear curve can be observed in Fig. 9.

This investigation demonstrates that the MOS parameters (pMOS width, gate voltages, attached capacitances) had a significant impact on the current through the inverter and with that on the failure of the susceptible nMOS. Assuming a failure current of approximately 2 mA/μm, the nMOS would survive in the first case but would fail for a certain pMOS width using the second setup.

4 Conclusion

In addition to the width of powerclamp and pMOS the gate potential controlled by capacitors has a significant influence on the current through the inverter. It depends on the capacitors, which can be external or intrinsic, if the current through the inverter surmounts the failure current, and thus if the inverter fails. This is one possible answer to the question why only a few of many equal inverter structures are susceptible to ESD events. ESD performance doesn't only depend on the design of the inverter, but also on the behaviour of the surrounding circuitry during ESD. In real circuitry, diverse factors can affect the current and thus the failure of the inverter. So adjacent circuitry as well as parasitics like capacitors and resistors have to be included to the investigation of ESD failures by circuit simulation.

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