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# Broadband suppression of phase-noise with cascaded phase-locked-loops for the generation of frequency ramps

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**Abstract.** The generation of analogue frequency ramps with non-fractional phase-locked-loops (PLL) is a cost effective way of linearising varactor controlled oscillators (VCO). In case that the VCO shows a high phase-noise level, a single non-fractional PLL is not able to suppress the phase-noise of the VCO sufficiently. The reason for this is the limited loop-bandwidth of the PLL. In the field of precise measurements a high phase-noise level is mostly not tolerable.

Examples of VCO-types with an extremely high phase noise level are integrated millimetre wave oscillators based on GaAs-HEMT technology. Both, a low quality factor of the resonator and a high flicker-noise corner frequency of the transistors are the main reason for the poor phase-noise behaviour. On the other hand this oscillator type allows a cost effective implementation of a millimetre-wave VCO. Therefore, a cascaded two-loop structure is presented that is able to linearise a VCO and additionally to reduce its phase-noise significantly.

## 1 Introduction

There are different concepts for the generation of linear frequency ramps. Automatic frequency control (AFC) schemes are fully analogue ways of linearising a non-linear VCO but with a low precision. In the field of digitally assisted concepts the PLL linearisation is an effective method to linearise and stabilise a VCO. Especially fractional-N phase-locked-loops are excellent means to generate highly linear frequency ramps. Basically a fractional PLL is well suited to achieve both, a very good ramp linearity and a phase-noise reduction of the VCO. Unfortunately this requires a very high reference frequency and a complex high-speed digital circuit that would result in a costly design.

To overcome these limitations a two-loop system is shown in the following that offers a good linearity level together with a broadband phase-noise reduction of the VCO. The concept is based on the partitioning of the linearisation part and the phase-noise reduction part of the system each in one of the two phase-locked-loops. The concept is evaluated with numerical simulations as well as with measurements on a prototype system. The millimetre-wave VCO used in the prototype system is an integrated GaAs-HEMT based oscillator with a phase-noise level of $-70$ dBc/Hz at 1 MHz carrier offset. This free running phase-noise behaviour is not sufficient for measurement systems like high precision radar systems.

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## 2 Concept of the cascaded double PLL system

The functional principle is illustrated in the simplified block-diagram in Fig. 1.

The ramp PLL on the left side generates an auxiliary frequency ramp signal. As the VCO in the auxiliary PLL is running at frequencies $f_h$ between 640 MHz and 960 MHz, the phase-noise behaviour of the auxiliary ramp signal is quite good. This is due to the fact that the $VCO_1$ is based on silicon bipolar transistors with a low 1/f-corner frequency and that a high Q resonator is used.

The linearity is achieved with a non-fractional ramp PLL relying on a fast programmable frequency divider. The division ratio $\div N$ of the frequency divider is increased or decreased in integer unity steps at equidistant time intervals. The division ratio of the frequency divider is determined by the micro-controler $\mu P$. As the programming of the frequency divider needs a precise timing, a synchronizing circuit is implemented to provide the divider with a new division value just in time. If the strict timing conditions are violated, the ramp linearity will be clearly deteriorated. The divider is programmed synchronously with the reference frequency so that the following Eqs. (1) and (2) can be derived.

$$Z = \sqrt{B_r \cdot T_r} \tag{1}$$

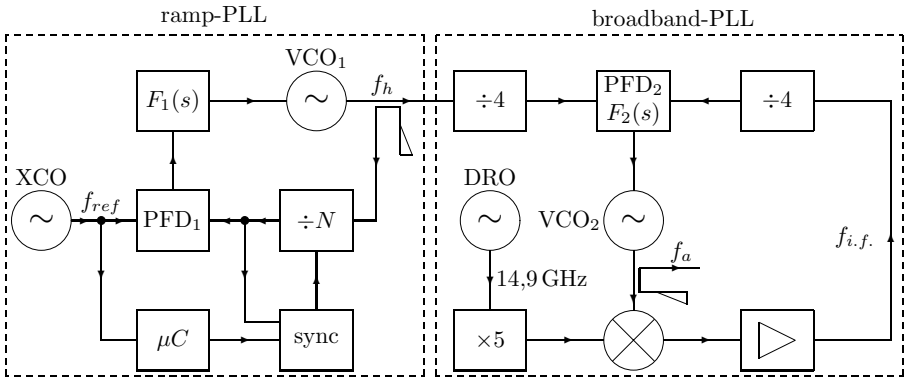


**Fig. 1.** Simplified block diagram of the two-loop PLL.

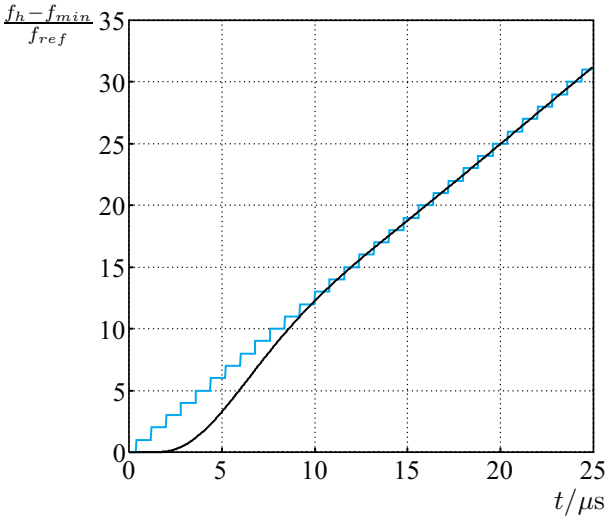


**Fig. 2.** Simulation of the PLL settling at the ramp start in comparison to the stepped static frequency stairs.

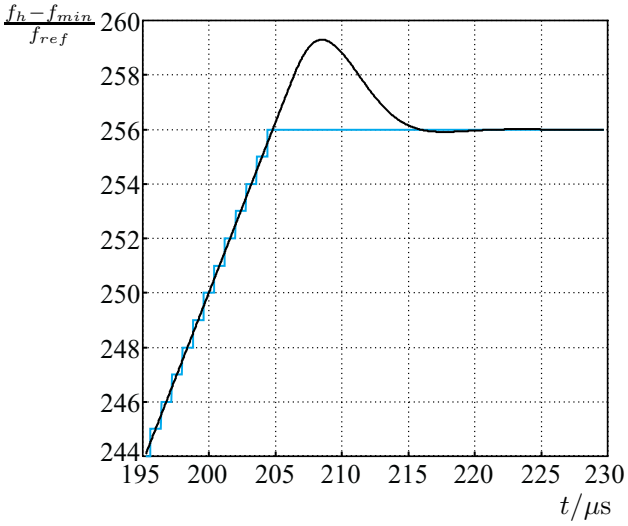


**Fig. 3.** Simulation of the PLL settling at the ramp end in comparison to the stepped static frequency stairs.

$$f_{ref} = \sqrt{\frac{B_r}{T_r}}. \tag{2}$$

The reference frequency $f_{ref}$ and the number of division factor steps $Z = N_{max} - N_{min}$ on the frequency ramp are directly depending on the VCO sweep bandwidth $B = f_{max} - f_{min}$ and the sweep time $T_r$ of the ramp. Normally the ramp time $T_r$ and the ramp bandwidth $B_r$ are determined by the application. In this system the ramp parameters are:

$$B_r = 320\,\text{MHz} \tag{3}$$
$$T_r = 204.8\,\mu\text{s} \tag{4}$$
$$Z = 256 \tag{5}$$
$$f_{ref} = 1.25\,\text{MHz}. \tag{6}$$

The ramp time is chosen to be quite small to achieve very short measurement times which is important for example in a radar system with a fast moving target.

The output signal of the frequency divider is compared with the reference signal $f_{ref}$ from the crystal oscillator by means of a phase frequency discriminator (PFD). The loop filter $F_1(s)$ suppresses the unwanted reference frequency which is equal to the step frequency of the division ratio increment resulting in a smooth analogue frequency ramp.

A simulation of the ramp characteristic versus time gives a good impression of the behaviour of such an analogue frequency ramp. The result of such a simulation is shown in Figs. 2 and 3 for the ramp start and for the end of the ramp, respectively.

Beside the ramp shape the stepped quasi static frequency stair is shown in the diagrams. The smoothing effect of the loop filter forms the analogue frequency ramp from the original frequency stairs. The settling behaviour is similar to that of a normal statically stepped phase-locked-loop. The only difference is due to the settling to a ramp instead of settling to a constant frequency. In case of a linear PLL mode this

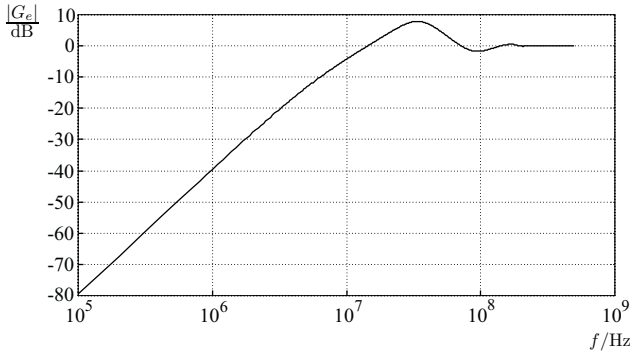


**Fig. 4.** Simulated closed loop error transfer function of the broadband PLL.

settling to the ramp can be dealt with in a similar way as in a static PLL. This means that a phase-locking condition also exists for an analogue frequency ramp-PLL.

At the output of the first $VCO_1$ a smooth frequency ramp with a good phase-noise behaviour is provided as the input signal to the broadband PLL. This broadband PLL relies on an extremely high reference frequency in excess of 150 MHz which enables a high loop-filter bandwidth. To check the loop bandwidth the simulation depicted in Fig. 4 shows the error transfer function in the closed loop versus the carrier offset frequency.

This error transfer function gives the chance to estimate how the phase-noise of the VCO is suppressed by the broadband PLL. The diagram shows a large loop bandwidth of more than 15 MHz. This loop bandwidth allows to stabilise even very noisy oscillators in the two-loop system.

In the broadband PLL a dielectric resonator stabilised oscillator (DRO) generates a fixed-frequency local oscillator signal at 14.9 GHz for a harmonic mixer. This harmonic mixer is essential because the main $VCO_2$ runs at approximately 76 GHz which is much to high to apply its output-signal directly to a digital frequency divider. With the help of this local oscillator signal the $VCO_2$ frequency is down-converted to intermediate frequencies $f_{i.f.}$ in the range of 640 MHz ... 960 MHz, which are equal to the frequencies generated by the auxiliary PLL.

## 3 Measurements

To prove the simulated results concerning the phase-noise suppression and to show the good linearity of the generated frequency ramps a prototype system has been built. Figure 5 shows the block diagram of the prototype system, which, in comparison to Fig. 1, has been extended by a modified FMCW-module to measure the ramp linearity and to estimate the benefit of this concept when being implemented in a FMCW-radar system.

Additionally a spectrum analyser (spec) has been added to measure the phase-noise of the oscillator in a fixed frequency mode. Photos of the two PLL circuits are depicted in Fig. 6 to illustrate the complexity of the system.

The left circuit shows the auxiliary ramp PLL from the top side. The microcontroller ($\mu$C) generates the division factor sequence while the other digital components synchronise the data stream from the $\mu$C and the programmable divider. The programmable divider is located on the bottom side of the circuit and is therefore not visible in this picture. Besides these parts the crystal oscillator is located on the top of the left picture providing a stable reference signal for the phase frequency detector ($PFD_1$) in the ramp PLL.

The broadband PLL stabilising the main $VCO_2$ is shown in the right picture. This PLL contains many discrete components that are necessary because the active loop filter is in need of a very high bandwidth while having a low noise figure at the same time. The core element of this PLL is the $PFD_2$ in ECL-technology located at the left part of the picture. As the voltage swing at the output of this ECL-PFD is only 0.8 V, the following amplifier is a critical component concerning its input noise.

The first measurements taken with this prototype system are related to the phase-noise reduction capability. In Figs. 7 and 8 the result of a measurement with the noisy $VCO_2$ only stabilised with the narrowband auxiliary PLL is compared with a measurement where the $VCO_2$ is stabilised in the cascaded two-loop system. The measurement with the narrowband PLL is performed substituting $VCO_1$ in the auxiliary PLL by the dashed circuit block $VCO_2'$ including the millimetre-wave $VCO_2$, the DRO and the harmonic mixer. This can easily be done because the dashed circuit block $VCO_2'$ macroscopically behaves quite similar to a simple low frequent VCO as for example $VCO_1$.

For this measurement the ramp PLL is programmed to generate a fixed frequency. A static frequency is necessary for the spectrum analyser to measure the phase-noise. As can clearly be seen the phase-noise level at an offset frequency of 1 MHz is improved by more than 37 dB. Compared to the theoretically predicted improvement of 40 dB in Fig. 4 this measurement result is quite close to the simulation. This noise reduction would be hard to reach with a fractional PLL as the reference frequency would have to be even higher than the one in the broadband PLL.

In the next measurement the modified FMCW-system is used for dynamic ramp measurements. This modified FMCW-system relies on a 25 m long low dispersion coaxial delay line. As in a normal free space FMCW-radar the ramp signal $U_1$ from the two-loop generator is down-converted to an i.f-signal with a delayed version $U_2$ of the original ramp signal $U_1$. The resulting i.f.-signal $U_{i.f.}$ is digitised with the help of a digital storage oscilloscope (DSO) and transferred to a computer (PC) for further signal processing. As a first result two i.f.-spectra derived from the i.f.-signals by a Fast Fourier Transform (FFT) are shown in Figs. 9 and 10.

The left spectrum results from a measurement with the $VCO_2$ stabilised just with the auxiliary PLL in comparison to the measurement shown in the right spectrum that has been made with the $VCO_2$ stabilised in the complete

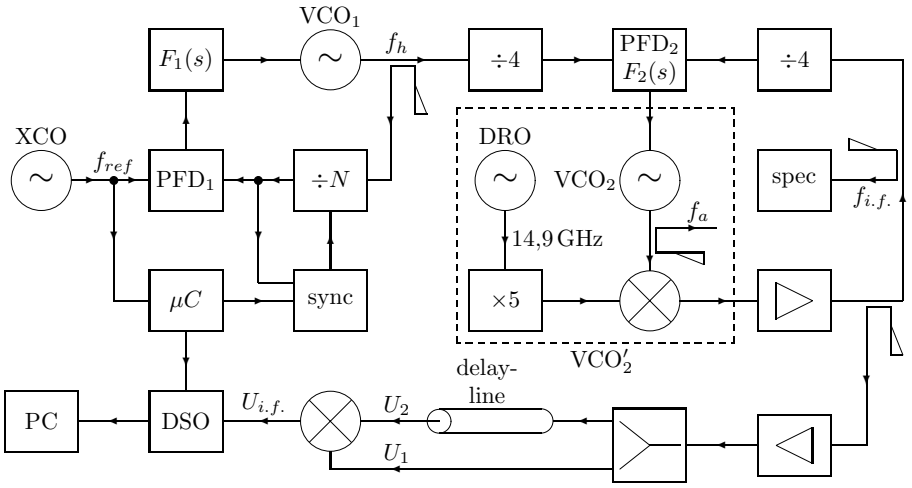


**Fig. 5.** Simplified block diagram of the cascaded PLL system with a modified FMCW-system.

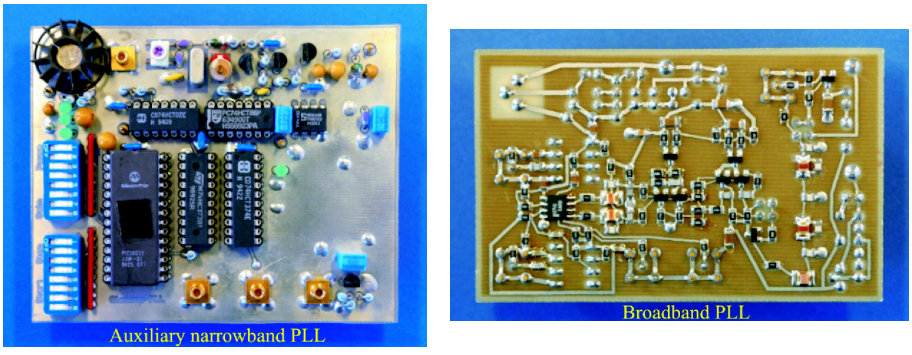


**Fig. 6.** Photos of the two PLL circuits.

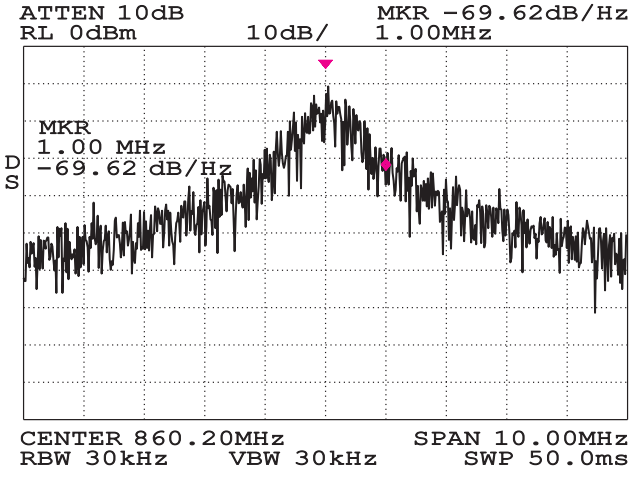


**Fig. 7.** Spectrum of the 76 GHz VCO only stabilised in the auxiliary PLL.

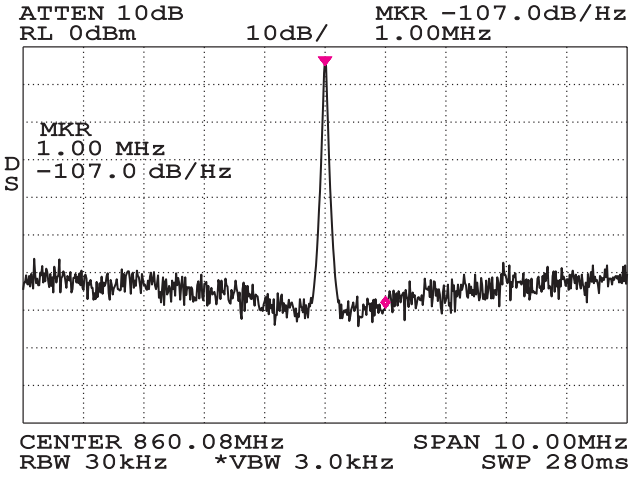


**Fig. 8.** Spectrum of the 76 GHZ VCO stabilised in the broadband PLL.

two-loop system. Again a significant reduction of the noise-level is achieved. While in the left spectrum the target peak can hardly be found, in the right spectrum the noise level is well reduced showing a clear and narrow spectral peak.

The result from these measurements is, that the integrated HEMT-$VCO_2$ stabilised in a single loop ramp PLL is not applicable for the use in a FMCW-radar system. With the help of the cascaded two-loop structure it is possible to stabilise

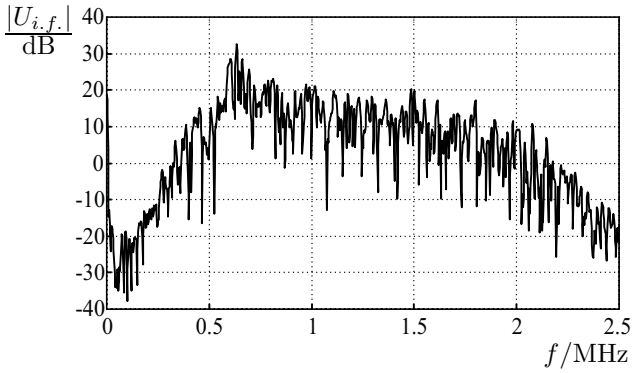


**Fig. 9.** Measured i.f.-spectrum of the modified FMCW-system with the 76 GHz VCO stabilised in the auxiliary PLL only.

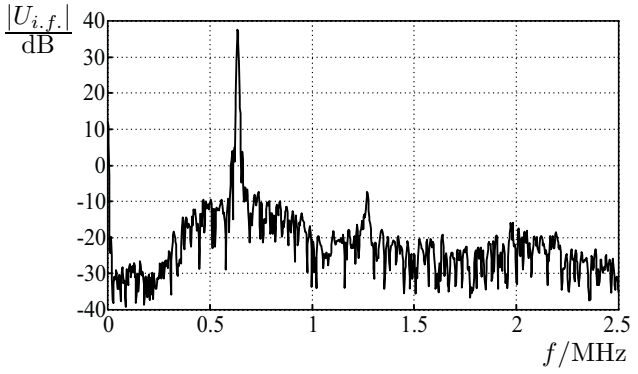


**Fig. 10.** Measured i.f.-spectrum of the modified FMCW-system with the 76 GHz VCO stabilised in the broadband PLL.

the $VCO_2$ well enough to implement it into a FMCW-radar.

Another measurement deals with the frequency deviation of the generated ramp from the ideal ramp. To derive this information the i.f.-spectrum of the modified FMCW-system in the two-loop set up is used to calculate the analytical time signal. The phase of this analytical time signal is used to calculate the frequency deviation $\Delta f$ from the ideal ramp. This frequency deviation is depicted in Fig. 11.

The maximum linearity error is in the order of $\pm 120$ kHz. Related to the ramp bandwidth of 320 MHz this leads to a relative non-linearity in the order of $3.75 \cdot 10{-}4$. This result is quite poor compared to relative linearity errors of less than $10{-}7$ achievable with fractional phase-locked-loops but it is still good enough for an implementation in a FMCW-radar-system. A FMCW-system is quite inert against small linearity errors because of the homodyne structure. The higher linearity error results from the low number of division factor steps of $Z = 256$ in the auxiliary ramp PLL. Running the auxiliary ramp PLL with a longer ramp time $T_r$ would allow for a higher number of steps $Z$ thus resulting in a better ramp-linearity. Also a fractional-N ramp PLL could be used in the auxiliary PLL thus resulting in an excellent ramp linearity but at the expense of a higher system complexity and higher cost.

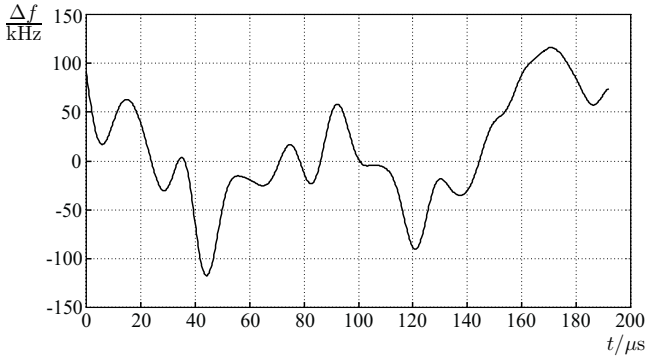


**Fig. 11.** Measured frequency deviation of the PLL stabilised 76 GHz VCO from the ideal ramp.

## 4 Conclusion

A cascaded two PLL non-fractional ramp generator is described that aims at linearising and stabilising extremely noisy oscillators like integrated HEMT-VCOs. The concept is based on the partitioning of the ramp generation and the phase-noise reduction to two different phase-locked-loops respectively. On the basis of numerical simulations and measurements on a prototype system the functional principle has been checked. The two-loop system is able to improve the phase-noise of the free running VCO significantly. A measurement with a modified FMCW-system shows the applicability of the concept for sensitive radar systems.

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