Fractional-N PLL based FMCW sweep generator
for an 80 GHz radar system with 24.5 GHz bandwidth

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Abstract. A phase-locked loop (PLL) based frequency synthesizer capable of generating highly linear broadband frequency sweeps as signal source of a high resolution 80 GHz FMCW radar system is presented. The system achieves a wide output range of 24.5 GHz starting from 68 GHz up to 92.5 GHz. High frequencies allow the use of small antennas for small antenna beam angles. The wide bandwidth results in a radar system with a very high range resolution of below 1.5 cm. Furthermore, the presented synthesizer provides a very low phase noise performance of −80 dBc/Hz at 80 GHz carrier frequency and 10 kHz offset, which enables high precision distance measurements with low range errors. This is achieved by using two nested phase-looked loops with high order loop filters. The use of a fractional PLL divider and a high phase frequency discriminator (PFD) frequency assures an excellent ramp linearity.

1   Introduction

Frequency-modulated continuous-wave (FMCW) radar systems are widely used in a large field of applications. The most important industrial markets are e.g. automotive radars and high precision range measurement radars. This applications presume special requirements for the radar sensor.

Automotive radars need a high spatial resolution to divert the antenna beam to separate cars on different lanes in distances of about 150 m. Because of design specifications, the antennas have to be very small, and these requirements can only be fulfilled by using high frequencies in the region of 80 GHz or even higher.

Special range measurement radars for challenging applications with many disturbing objects also need a high beam directivity and a small antenna at the same time to be focused to the target. For these reasons it is also favorable to use high frequency ranges in this field of application.

In order to separate interfering reflections of disturbing objects from the desired signal of the radar target, a high range resolution is necessary. The radar range resolution ΔR defines the ability to distinguish two targets close to each other. It can be calculated as:

$$\Delta R = \frac{c_0 \cdot B_{\mathrm{w}}}{2(f_{\max} - f_{\min})} = \frac{c_0 \cdot B_{\mathrm{w}}}{2 \cdot \Delta f} \ , \tag{1}$$

where c_0 is the speed of light, B_{w} a factor to describe the influence of the window function used in signal processing, and Δf the bandwidth of the frequency ramp. With the commonly used Hanning window to suppress sidelobes and using the −6 dB width to define two separable targets $B_{\mathrm{w}} = 2$.

Table 1 shows the range resolution for several bandwidths. Standard industrial range measurement radar sensors typically have a bandwidth smaller than 2 GHz due to the complexity of broadband radar systems. State of the art research FMCW radar system like the COBRA94 (Fraunhofer FHR, Germany) allow a bandwidth up to 8 GHz (Essen et al., 2005, 2008). The current record in bandwidth of 10 GHz is set by Nicolson et al. (2008). The presented frequency synthesizer is capable of generating FMCW sweeps with more than 24.5 GHz bandwidth, so the range resolution is improved by more than a factor of 2. This allows a better separation of two near targets, where one of them is the wanted signal like shown in Fig. 1. Here, the advantage of ultra high resolution and high bandwidth FMCW radar systems is clearly visible. With 4 GHz bandwidth, it is impossible to separate the

Table 1. Range resolution for different ramp bandwidths using a Hanning window function in signal processing. Typically, the accuracy of single target distance measurements is decades better.

Bandwidth	2 GHz	5 GHz	10 GHz	25 GHz
Resolution	150 mm	60 mm	30 mm	12 mm

two targets. By using 24.5 GHz bandwidth, the signal of the wanted target can easily be separated from the disturbing target.

2 Concept of the FMCW-Synthesizer

2.1 Overview

The simplified block diagram of the realized FMCW radar signal synthesizer is shown in Fig. 2. A SiGe monolithic microwave integrated circuit (MMIC) with a broadband millimeterwave voltage controlled oscillator (VCO) produces the output signal in a frequency range from 68 GHz to 92.5 GHz (VCO80G, Fig. 2) (Pohl et al., 2009; Pohl, 2010). The MMIC also includes a mixer, a second VCO at 24 GHz (VCO24G, Fig. 2) and two fixed frequency dividers (Pohl et al., 2011).

For stabilization of the VCOs two PLLs with commercially available off-the-shelf frequency synthesizer chips (HMC701LP6CE from Hittite Microwave) are used. The frequency of the output signal of the auxiliary VCO (VCO24G) is divided by 8 to get a low frequency signal, which is well suited for use with commercial frequency synthesizers. An external active loop filter is used to close the loop. A 100 MHz ultra low phase noise temperature controlled crystal oscillator (TCXO) provides the reference signal in order to allow low divider factors in the PLL. For best phase noise performance, an integer divider PLL synthesizer is used. The output frequency is fixed to 24 GHz.

The mmWave VCO (VCO80G) is stabilized in a different way. First, the output signal is divided by a factor of 4 to obtain a signal in a frequency range from 17 GHz to 23.125 GHz, then this signal is downconverted with the fixed 24 GHz output of the auxiliary PLL. Due to image frequencies this results in an output frequency in the range from 0.875 GHz to 7 GHz, which is well suited for commercial PLL synthesizer ICs. The loop is closed with an external loopfilter again. For highly configurable ramp generation the fractional mode of the commercial frequency synthesizer chip with a high reference frequency is used. Frequency ramps are generated by changing the fractional divider inside the synthesizer IC with the build in ramp generator.

The two PLLs are programmed using a microcontroller which can be interfaced with a serial to USB converter to a computer. This assures flexible ramp generation possibilities
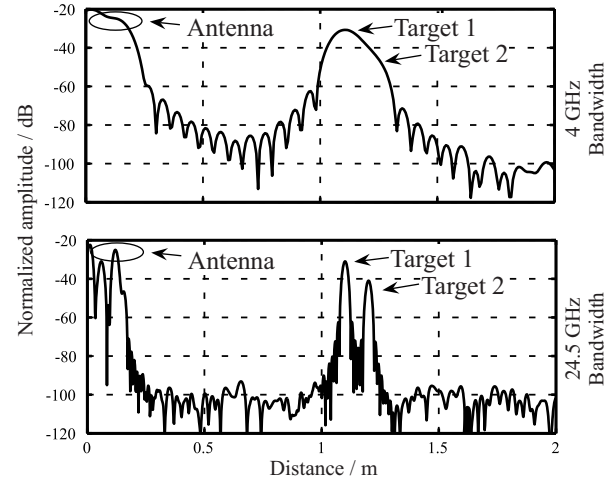

Fig. 1. Simulation of a radar scenario with 4 GHz and 24.5 GHz sweep bandwidth. Target 1 is positioned 1 m behind the antenna, followed by Target 2 another 0.1 m behind it.

in relation to start and stop frequency, bandwidth and slope of the frequency ramp.

2.2 mmWave-Module

The RF-Module contains the high frequency parts of the system. It is based on a Rogers RT/duroid 5880 high frequency substrate mounted on a brass block for a good mechanical stability, and heat transfer. The MMIC is glued into a milled hole and connected to the substrate with bond wires as shown in Fig. 3. The inductive influence of the short and well-defined bond wires for the 68 GHz to 92.5 GHz output is compensated using an Monte-Carlo technique optimized on-chip matching network (Pohl et al., 2012). To reduce influences of the ground plane, to lower the supply voltage swing, and to assure robust signals, all high frequency transmission lines are connected using differential outputs (Rein and Moller, 1996). Bond wires on the left and right side connect the supply and the tuning voltage for the two VCOs.

Figure 4 shows the complete mmW-Module. A rat race coupler is used to transform the differential 80 GHz signal to a single ended signal. A pad for a wafer prober (110H-GSG-150 from PicoProbe) was designed to connect the 80 GHz output with external measurement equipment. The divide-by-4 outputs of the 80 GHz signal can also be connected to measurement equipment by using SMA-connectors to allow noise characterization with commercially available spectrum analyzers.

2.3 PLL-Module

A photo of the PLL-Module is shown in Fig. 5. It consists of a low noise power supply to prevent degradation of the good noise performance. In addition, both PLLs are placed
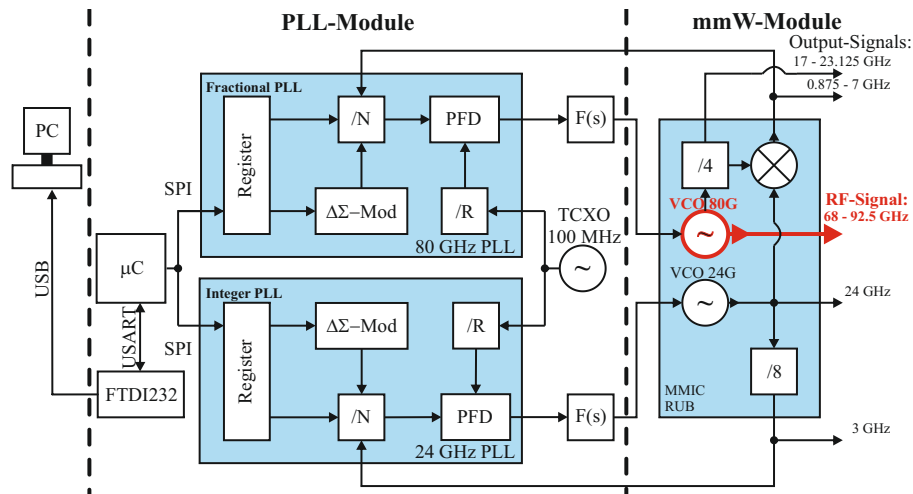
Fig. 2. Block diagram of the frequency synthesizer used to generate the wide bandwidth 68 GHz to 92.5 GHz output signal.
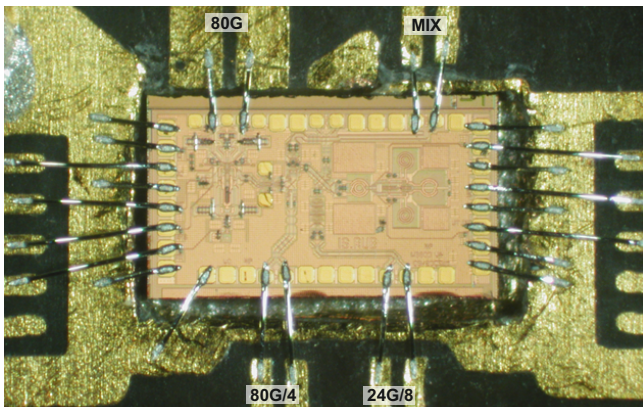

Fig. 3. Section of the MMIC with the two VCOs, the mixer and the two fixed dividers mounted on a Rogers RT/duroid 5880 high frequency laminate.
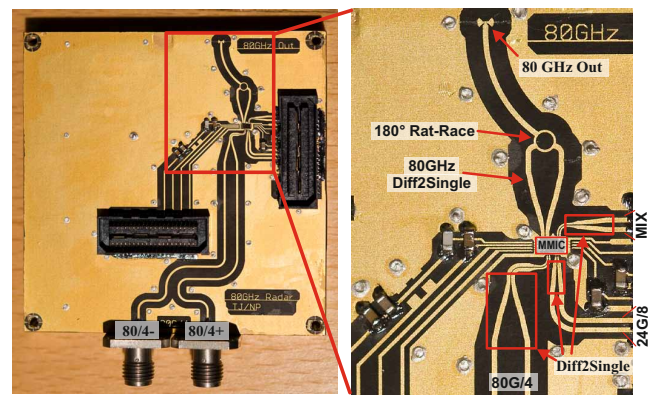

Fig. 4. Photo of the complete mmW-Module with the MMIC and two Samtec QSE high frequency connectors to connect the PLL-Module.

on this module. Each of them includes a PLL synthesizer IC and an optimized high order (PLL24: 4th order, PLL80: 5th order) active loop filter. The PLL ICs are programmed via a serial peripheral interface (SPI) using a microcontroller (ATXMEGA128 from Atmel) on the back side of the module. Connection to a computer can be achieved with the build in Mini-USB-Connector on the lower right side. On the upper left side the SMA-connector for a TCXO reference is visible.

Figure 6 shows the detailed schematic of the loop filter. A low noise operational amplifier (OpAmp) is used to prevent system noise degradation caused by the high tuning sensitivity of the VCO. The inverting Op Amp circuit is biased at half of the charge pump (CP) supply with R_{b1} and R_{b2} to achieve the best operating point. A first part of the filter is placed in front of the OpAmp to pre-smooth the hard current pulses of the charge pump. The loop bandwidth was chosen

to achieve a minimal integrated phase noise. For the auxiliary VCO (VCO24G, 50 MHz PFD-frequency) a bandwidth of 530 kHz with a phase margin of 50° and for the mmWave VCO (VCO80G, 20 MHz PFD-frequency) a bandwidth of 270 kHz with a phase margin of 55° has been obtained.

3 Measurements

3.1 Phase noise

In order to test and to characterize the synthesizer, phase noise measurements have been performed in different temperature ranges.

Figure 7 shows the measured phase noise at a center frequency of 80 GHz and at a temperature of 20 °C. Further measurements show that the degradation over temperature
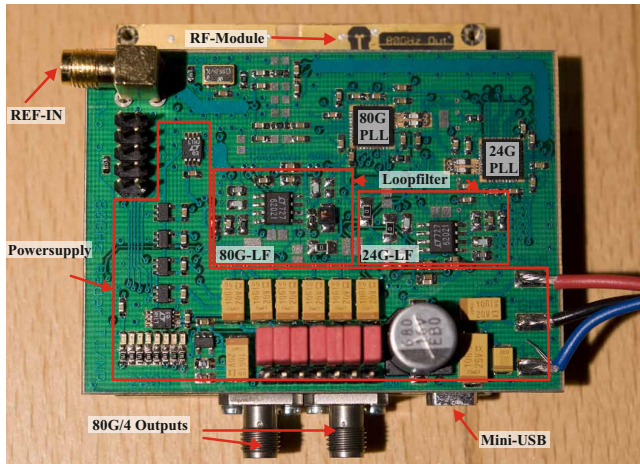
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Fig. 5. Photo of the PLL-Module with low noise power supply, the commercial Hittite HMC701LP6CE PLL synthesizer ICs and the active high order loop filter for both phase-locked loops.
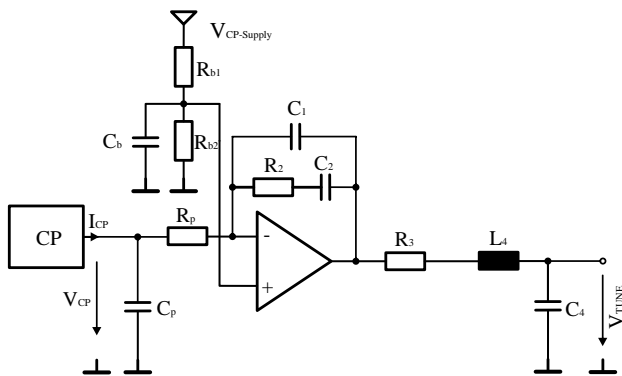

Fig. 6. Schematic of the 5th order active loop filter for optimal phase noise characteristics.

($-45\,°C$ to $90\,°C$) is below $3\,dB$. Measurements have been done with a spectrum analyzer (8565E from Agilent) using the divide-by-4 outputs and adding $12\,dB$ to compensate an influence of the fixed divider.

The inband phase noise of about $-80\,dBc/Hz$ is determined by the PLL noise floor. It almost perfectly fits the predicted phase noise values. The difference at offset frequencies lower than $2\,kHz$ is due to measurement inaccuracy because of the carrier drift. At offset frequencies greater than the loop bandwidth, the phase noise approaches the free running VCO's phase noise.

3.2 Ramp generation

Almost the complete VCO bandwidth can be used in FMCW ramping mode. Figure 8 shows the tuning voltage in continuous sawtooth ramping mode. A FMCW bandwidth of
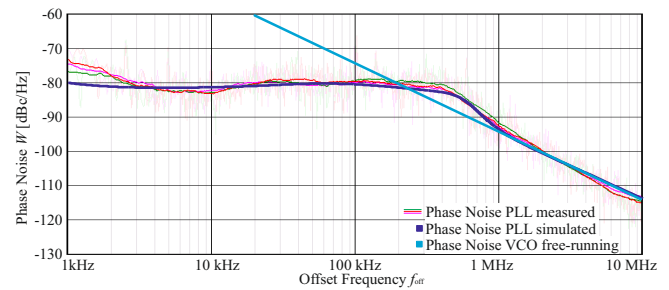

Fig. 7. Measured phase noise of the mmW-VCO output signal at $80\,GHz$ and $20\,°C$ against previously simulated and free-running VCO phase noise.
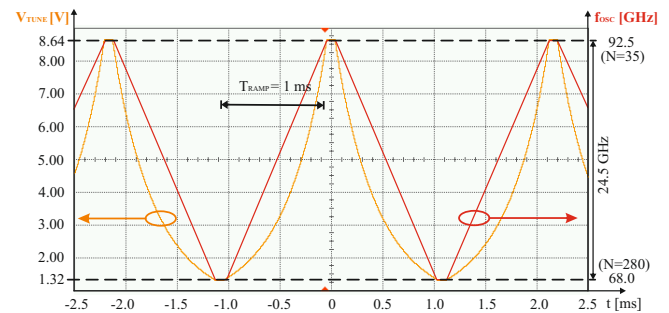

Fig. 8. Measured tuning voltage in continuous FMCW sawtooth ramping mode with a ramp time of $1\,ms$.

$24.5\,GHz$ with an output frequency from $68\,GHz$ to $92.5\,GHz$ is achieved with fractional frequency divider factors between $N = 35$ and $N = 280$. In Fig. 8, an example with $1\,ms$ ramp-time is shown. The ramp duration can be programmed in wide ranges.

Figure 9 shows the measured spectrum of the divide-by-4 output while in ramping mode. Here, the wide bandwidth of $24.5\,GHz$ $((23.125–17\,GHz) = 6.125\,GHz = 24.5\,GHz/4$ at the divide-by-4 output) is clearly visible. The output power of the mmW output is $10\,dBm$ to $12\,dBm$ and much smoother than the output power of the unbuffered divide-by-4 output (Pohl et al., 2009).

3.3 Radar performance

For demonstrating the FMCW synthesizer performance, a mixer and an IF-stage including analog digital conversion and signal processing were added to complete the FMCW radar (Pohl et al., 2012).

Figure 10 shows a first measurement of a radar scenario with $24.5\,GHz$ FMCW bandwidth and a ramp duration of $4\,ms$. A W-band waveguide transition is used to connect the antenna to the FMCW system. The complete signal processing is done by using MathWorks MATLAB after digitization of the IF-signal with an $1\,MSPS$ ADC and transferring the data to the computer over USB. Reflections caused by the
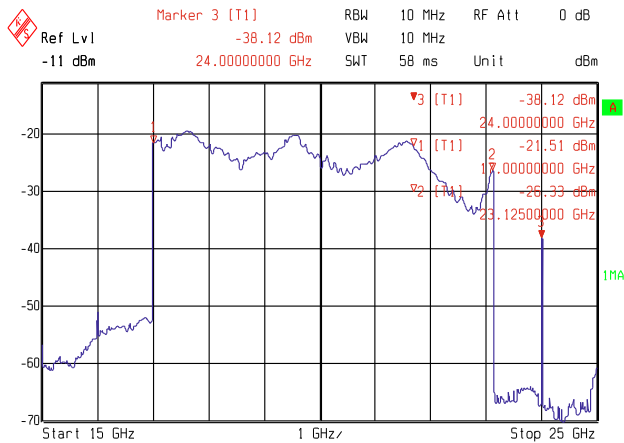
Fig. 9. Spectrum of the divide-by-4 measurement output in max-hold mode while ramping from 68 GHz to 92.5 GHz. The output power of the 80 GHz mmW generator is much smoother and shows a very small variation of ≈2 dB (10 dBm to 12 dBm).
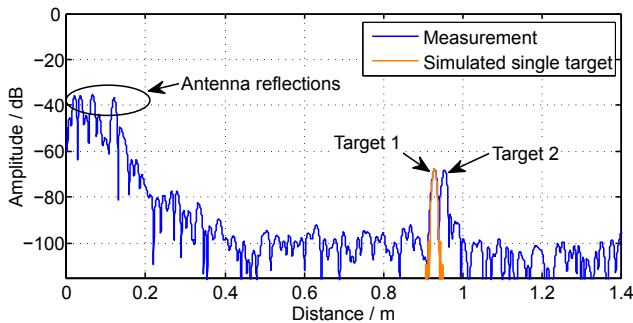

Fig. 10. IF spectrum of the measured radar scenario with two 3 mm diameter steel rods as targets.

antenna are visible at small distances. The targets 1 and 2 are steel rods with 3 mm diameter in about 2.58 cm distance from each other. These targets have a small radar cross section (RCS), but can easily be detected and separated by the sensitive high resolution FMCW radar.

4 Conclusions

A configurable PLL based frequency synthesizer for generation of highly linear broadband frequency ramps was presented, and its usability was confirmed by different measurements. Furthermore, the suitability for use as a FMCW signal source was approved by first measurements in a complete FMCW radar system with an outstanding maximum bandwidth of 24.5 GHz. The use of commercially available semiconductor components in combination with the SiGe MMIC allows a cost-effective realization of ultra high resolution FMCW radar systems, which is suitable for mass produc-

tion. This allows new fields of application for future FMCW radar sensors.

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