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Implementation of a digital trim scheme for SAR ADCs

J. Bialek[1], A. Wickmann[2], F. Ohnhaeuser[2], G. Fischer[1], R. Weigel[1], and T. Ussmueller[1]

[1]University of Erlangen-Nuremberg, Departement of Electrical Engineering, Erlangen, Germany
[2]Texas Instruments Deutschland GmbH, Germany

Correspondence to: J. Bialek (jan@bialek-net.de)

Abstract. Successive approximation register (SAR) analog-to-digital Converters (ADC) are based on a capacitive digital-to-analog converter (CDAC) (McCreary and Gray, 1975). The capacitor mismatch in the capacitor array of the CDAC impacts the differential non-linearity (DNL) of the ADC directly. In order to achieve a transfer function without missing codes, trimming of the capacitor array becomes necessary for SAR ADCs with a resolution of more than 12 bit. This article introduces a novel digital approach for trimming. DNL measurements of an 18 bit SAR ADC show that digital trimming allows the same performance as analog trimming. Digital trimming however reduces the power consumption of the ADC, the die size and the required time for the production test.

1 Introduction

SAR ADCs are widely used in electronic circuits because they cover the important application area for mid resolution and mid speed. In general, SAR ADCs are available with resolutions of 10 bit to 18 bit. The advantage of the SAR architecture is the possibility to capture a snapshot value of an analog signal. This behavior cannot be achieved with $\Delta\Sigma$-Converters since they convert the input voltage over a period of time instead of the input voltage of a single point in time. Whereas Pipeline ADCs are not manufactured with high resolutions because of rising demands of amplifier linearity with rising resolution.

Fig. 1 shows the basic principle of a SAR ADC. When the conversion cycle of the ADC is started, the sample and hold element (S&H) stores the input voltage V_{in}. The input voltage is compared to the output voltage of the DAC, which is usually implemented as a CDAC. The control logic adjusts the input word of the DAC according to the comparator decision. This cycle is repeated for each bit of resolution of the ADC, which means that an 18 bit ADC needs 18 conversion cycles to output the result. At the end of the conversion cycle the difference between the input voltage V_{in} and the DAC output voltage V_{DAC} is less than one Least Significant Bit (LSB).

The basic schematic of a 3 bit SAR ADC is shown in Fig. 2. The capacitors are used for sampling the input voltage as well as for the CDAC. The position of the switches in Fig. 2 represents the sampling mode. When switch S_{C} is opened, the trapped charge on the capacitors is proportional to the input voltage V_{in}. During the conversion cycle, the switches S_1 through S_3 are switched between the reference voltage V_{ref} and ground until the voltage V_{A} at node A is equal to the voltage at the non-inverting comparator input, which is in this case ground potential. At the end of the conversion the position of the switches S_1 through S_3 resemble the digital output word corresponding to the input voltage V_{in}. The voltage V_{A} can the be written as

$$V_{\text{A}} = -V_{\text{in}} + \frac{k_1 V_{\text{ref}} C}{2C} + \frac{k_2 V_{\text{ref}} \frac{C}{2}}{2C} + \frac{k_3 V_{\text{ref}} \frac{C}{4}}{2C} \quad (1)$$

where k_1 through k_3 are either 0 or 1 according to the position of the switches S_1 through S_3. Switch S_4 is not used for the conversion of the input voltage, as it is switched to ground potential at the beginning of the conversion. Its only purpose is to raise the total value of the capacitor array to $2C$. Equation! 1 shows the importance of capacitor matching. The voltage V_{A} is not a function of a capacitor value, but is a function of the ratio of the capacitor values and the value of the capacitor array.

The capacitors in the capacitor array are binary weighted. If their ratios are not binary, the conversion result will be wrong. Due to variances in fabrication processes, the capacitor ratios are never perfectly binary weighted. These errors result in deviation of the DNL. Examples of a perfect and erroneous DNL are shown in Fig. 3. The DNL can be measured using a staircase measurement. The input voltage of the ADC is set to a certain value where an output code transition

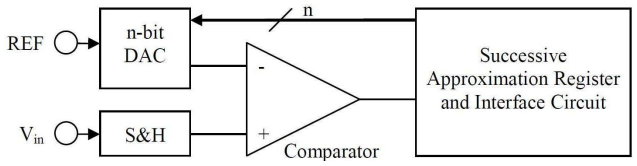

Fig. 1. Basic principle of a SAR ADC

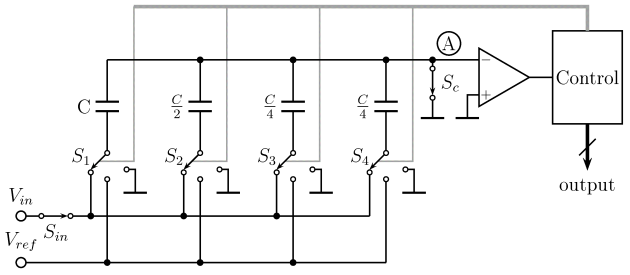

Fig. 2. Schematic of a 3 bit single ended SAR ADC with CDAC

occurs. Now the input voltage will be raised until the next output code transition occurs. The difference between these two input voltage values shall be measured in multiples of the LSB. The perfect DNL has a code transition every LSB, which means that every output code has the length of one LSB. The code length varies in the non-perfect DNL. If a code is completely missing, the DNL of this code equals −1. The integral non-linearity (INL) of a given output code is the sum of all the preceding DNL errors. These errors caused by the mismatch of capacitor ratios can be corrected by trimming. If all DNL errors can be corrected to equal zero, the INL errors are also zero.

2 Analog trimming

Trimming must be done in-package because parasitics between the die and the package influence the performance of the ADC. It is not possible to estimate these parasitics of ADCs with a resolution of 16 bit and more because air inclusions within the package make a large contribution to the parasitics. Therefore, analog in-package trimming was introduced (Ohnhaeuser et al. , 2010). A second capacitor array is added to the circuitry which is used for trimming the first capacitor array. This circuit can be seen in Fig. 4. During the production test of the assembled die, the DNL is measured and the trim capacitors are switched to fit the DNL. This procedure has to be repeated at least once more to get adequate results due to inaccuracies of the trim capacitors. Because the trim capacitors are not used during sampling, this procedure also produces a gain error, which has to be corrected afterwards. The trim capacitor array occupies space on the die and also adds to the production costs because of the increased test time.

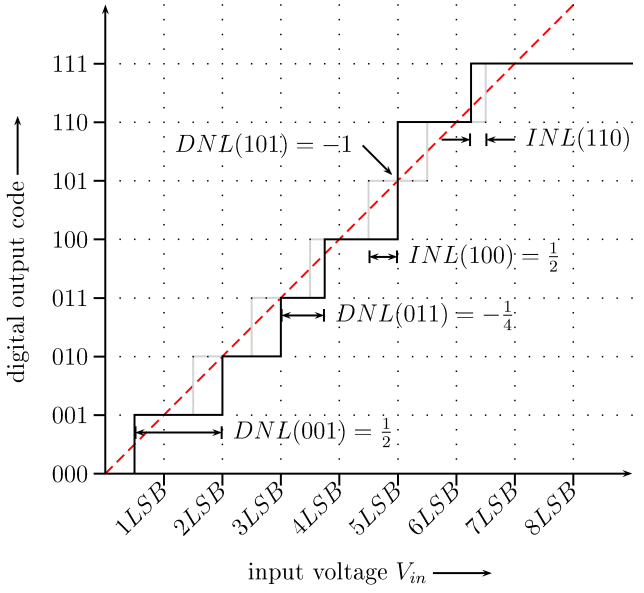

Fig. 3. Ideal (light) and erroneous (dark) output characteristic of an ADC

3 Digital trimming

The capacitors of the CDAC represent the major code transitions. If the error for each capacitor is known, it is possible to implement an arithmetic unit within the ADC that corrects the error (Reinhold et al. , 2011). This makes the trim array obsolete. This method only works, if the output codes are unique, i.e. no codes are missing. Therefore, a dynamic error correction is introduced, which adds a stage of redundancy. Several different forms of error correction units have been described in previous publications (Ogawa et al. , 2008; Bacrania , 1986; Cho et al. , 2009). The schematic of the improved capacitor array can be seen in Fig. 5. The dynamic error correction consists of two capacitors C_{DUP} and C_{DDWN} (Ohnhaeuser and Huemer , 2008; Srinivasan and Godbole , 2002). In this example, the dynamic error correction is placed between the second and the third bit decision. In dependence on the second bit decision the capacitor C_{DUP} is switched to the reference voltage or the capacitor C_{DDWN} is switched to ground potential to increase or decrease the voltage at the comparator input. The rest of the conversion executes as before. After the conversion, the value of the dynamic error correction is added to the SAR output. In order to guarantee converging voltages at the comparator input, the capacitances of C_{DUP} and C_{DDWN} are chosen to be a little smaller than C_2.

At the end of the conversion, the errors of each switched capacitor and the dynamic error correction are added to the output word.

Figure 6 shows an example of a possible implementation. In this case, the complete error is calculated at once which requires a large arithmetic unit. Also it will take some time until the corrected result will be available. Therefore, a finite

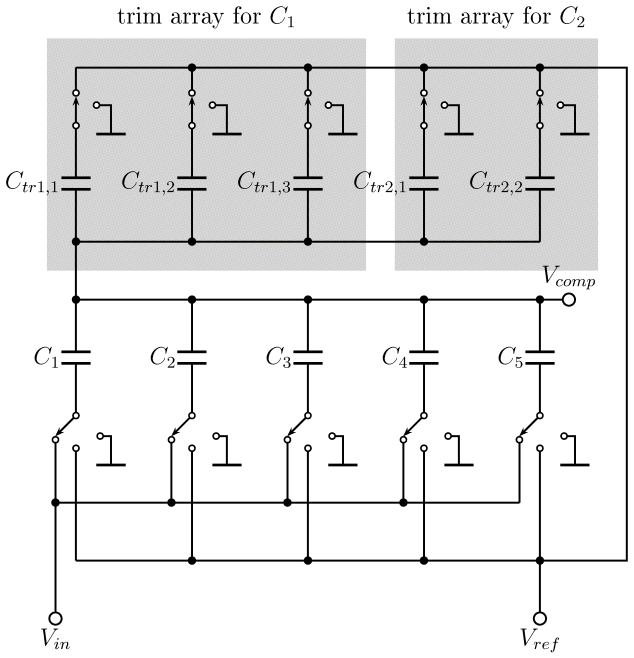

Fig. 4. CDAC with capacitor array for trimming C_1 and C_2

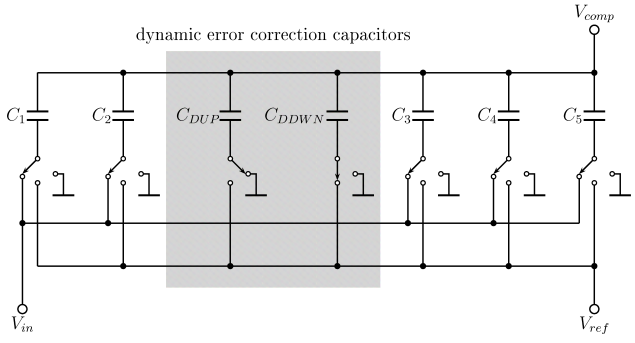

Fig. 5. CDAC with dynamic error correction

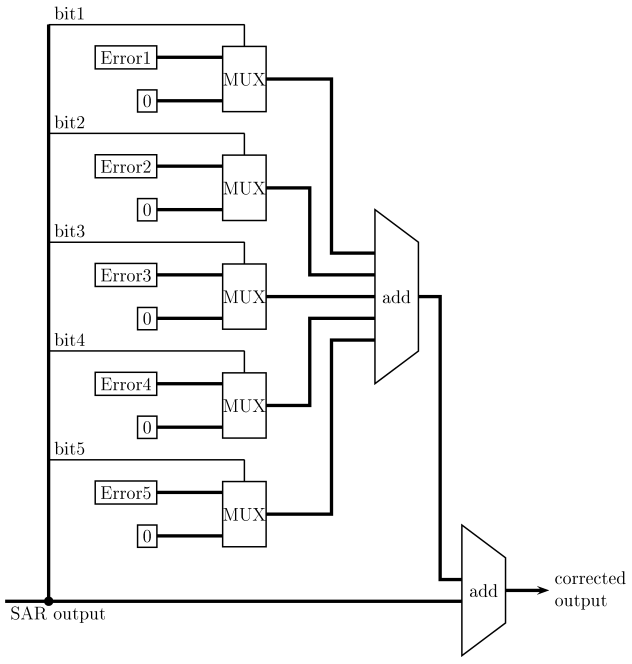

Fig. 6. Principal of digital trimming

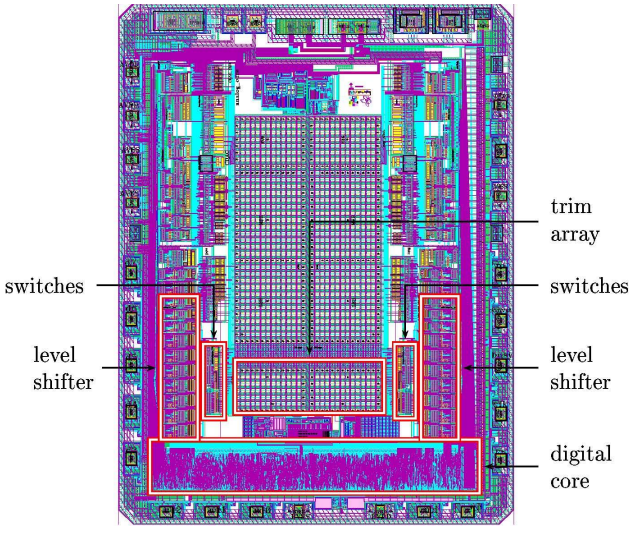

Fig. 7. Layout of 18 bit SAR ADC with trim related circuitry

state machine (FSM) approach to digital trimming will be faster and the arithmetic unit will be smaller (Bialek , 2009). After each bit decision, the error of the current bit decision is added to the present complete error if the bit decision is logic "1". Otherwise the complete error remains unaltered. The same is done for the dynamic error correction stage. Since the lower bits are usually not trimmed the complete error will be readily calculated several clock cycles before the end of the conversion. This has two advantages. First, the final addition of the total error and the SAR output can be done right after the last bit decision. The data can be processed faster than calculating everything at the end. Therefore, the sampling rate does not change. Second, it is possible to introduce additional trim capacitors that have a weight of a half and a quarter LSB into the CDAC. These capacitors will be switched according to the total error before the last conversions according to the fractional sum. This increases the trim resolution to $\frac{1}{8}$ LSB.

4 Measurements

Digital trimming was implemented in an 18 bit SAR ADC. The top level layout of the die is shown in Fig 7. The digital circuitry is located close to the bottom of the layout. Digital trimming occupies approximately one third of the digital core. The die area can be shrinked about 10 % because

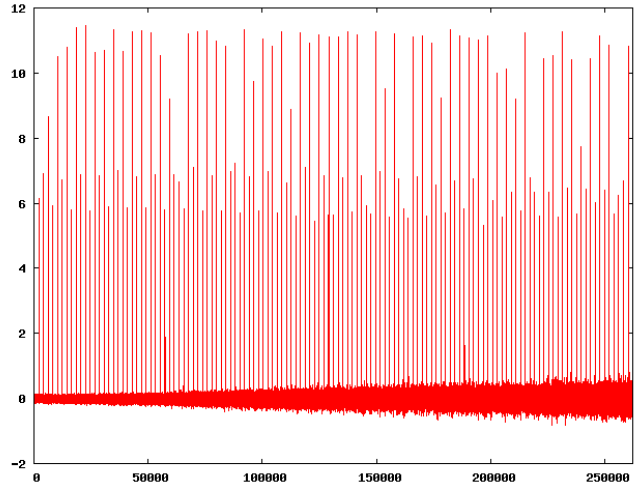

Fig. 8. DNL of an untrimmed 18 bit SAR ADC

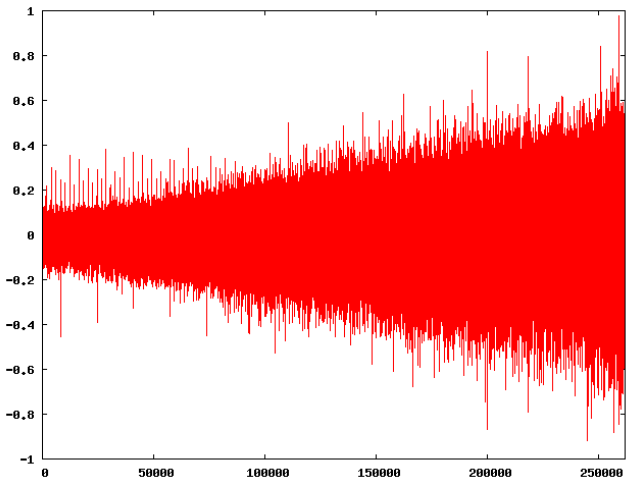

Fig. 9. Digitally trimmed DNL of the same SAR ADC as shown in Fig. 8

trim capacitors, level shifters and switches as shown in Fig. 7 are no longer necessary. Figure 8 shows the untrimmed and Fig. 9 shows the trimmed DNL of the same ADC in 18 bit mode. The untrimmed DNL shows mostly positive values because of the dynamic error correction shown in Fig. 5. The capacitance of the dynamic error correction capacitors is designed to ensure that no output codes are missing. Thus, resulting in large positive DNL values at major code transitions that happen prior to the dynamic error correction. After trimming, the DNL is always in between +1 LSB and −1 LSB. This means that no codes are missing and digital trimming achieves the desired result. The DNL in Figs. 8 and 9 becomes larger with codes coming closer to the full scale. This behavior is not caused by digital trimming, since the trimmed and untrimmed DNL show this characteristic. Possible causes for this might be noise within the ADC or noise in the reference path.

5 Conclusions

In this paper, a new digital trim method for SAR ADCs was introduced. The digital trim was implemented into an ADC as a design investigation and DNL measurements were performed. The DNL of the trimmed SAR ADC shows a similar characteristic of a state-of-the art SAR ADC and it was shown, that it is possible to decrease the die size. Digital trimming does not add parasitics to the CDAC and does not alter the mismatch of the capacitor array. The power consumption can be reduced because constant recharging of a trim capacitor array is no longer necessary. Also, it is not necessary to re-measure the DNL after the trim values are stored in the part. Approximately 50 % of the production costs result from the production test, of which another 50 % are caused by trimming. Reducing the time for production test will significantly cut the production costs of SAR ADCs.

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