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Design investigation to improve voltage swing and bandwidth of the SiGe driver circuit for a silicon electro-optic ring modulator

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Abstract. This paper reports on a new SiGe driver IC to address the low breakdown voltage level of modern BiCMOS transistors. An optical modulator driver IC in SiGe 250 nm technology with a supply voltage of 4.5 V is presented. This driver IC consists of pre- and main driver stages where a newly modified cascode topology and capacitance degeneration technique is employed to meet current application requirements; high voltage swing at high datarate. The simulation results show a differential output voltage swing of 3.9 Vp-p at 14 Gbps data rate, according to the FDR Infiniband standard.

1 Introduction

In recent years, many studies have worked to solve the bandwidth limitations of wire interconnection and the resulting cross talk in data communication. Photonics could be one way to solve this issue, even at higher transmission distances. By integrating optics into electronics, silicon phonic technology promises to offer a higher level of integrity, greater bandwidth and lower energy consumption in data transmission (Zuffada, 2012).

The optical modulator is a key element to implement the electrical-to-optical data conversion chain on the transmitter side. A micro-ring resonator, fabricated on a silicon substrate, is a high speed optical modulator (Zuffada, 2012). It maps voltage swing across its terminal to a specific level of optical output power. The proper Extinction Ratio (ER) is one of the main quality factors for optical modulation and is therefore dependent on the amplitude of the swing across the ring. Measurement results indicate (Giesecke et al., 2014) that voltage modulation must be in the range of 3–4 V to provide an acceptable ER. Since a back plane electrical signal could not directly fulfill this requirement (InfiniBand Architecture, 2012), an inter-stage broadband amplifier (here known as a driver IC) is needed to complete the electrical-to-optical conversion chain.

In broadband amplifier, Current Mode Logic (CML) configuration is typically used as the last stage of amplifier. Nowadays, with increasing transient frequency of modern BiCMOS transistors, their breakdown voltage capability is going to lower values (Mandegaran and Hajamiri, 2004). Therefore, obtaining high voltage swing in high transmission data rate is not straightforward.

In Sect. 2 of the present paper, a new modified cascode topology that divides all of the voltage stress among three transistors is explored, and a capacitance degenerative technique that extends bandwidth is also reviewed. Driver IC designed in SiGe 250 nm technology will be explored in Sect. 3.

2 Design concept

2.1 Modified breakdown voltage doubler of bipolar transistors

In a CML configuration, the output transistor has to sustain the entire output voltage swing. Cascode topology is a conventional solution to divide voltage stress between two transistors. A number of techniques have been reported to tune the amount of voltage drop on each transistor (Mandegaran and Hajamiri, 2004; Li et al., 2005a, b; Li and Tsai, 2006; Rakowski et al., 2012). All of these techniques are based on pushing the base of the upper transistor, Q2, to follow the output voltage as shown in Fig. 1.

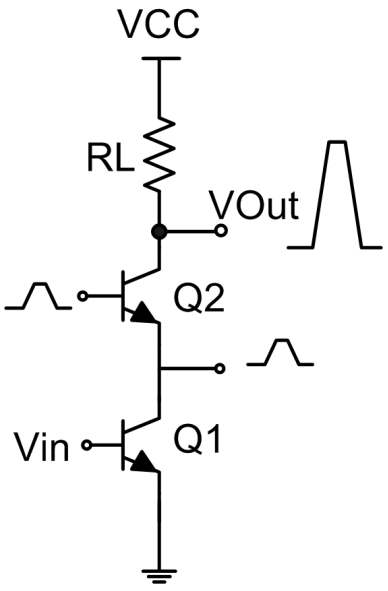

Figure 1. The idea behind modified cascode topology.

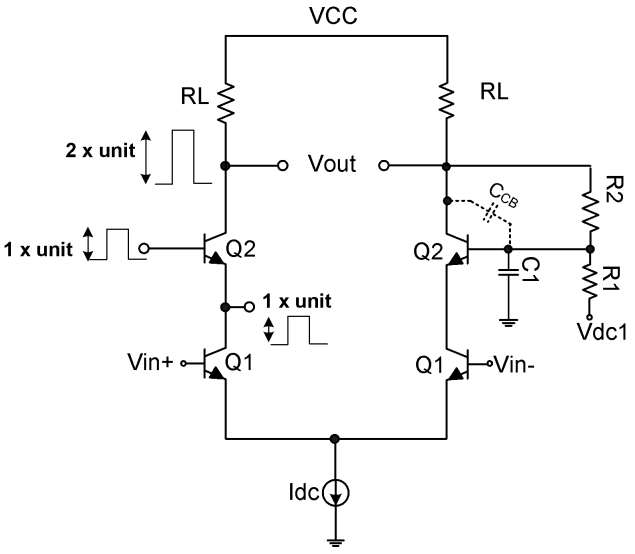

Figure 2. Modified cascode topology with feedback network and proper amplitude voltage ratio.

If the output voltage is at its maximum, it is desired to evenly divide the stress across two transistors in the case of similar devices in the stacks. A possible solution reported (Li et al., 2005a) is to use the intrinsic collector-base capacitance (CCB) of the upper transistor, Q2, to feed part of the output signal back to its base. In this way, both the base of the upper transistor and its emitter follow the collector as shown in Fig. 2.

The precise analysis of the feedback network is not straightforward, as the influence of the feedback network and transistor, Q2, must be taken into account as is explained here (Li and Tsai, 2006). The simplified feedback network, with neglecting the effects of large base-collector ohmic resistance and other parasitic capacitances, can be modeled by C1, CCB, R1, and R2 as is highlighted in Fig. 3.

A resistive feedback network (R2 and R1) defines low frequencies of amplitude voltage of base of transistor, Q2, and C1 with collector-base capacitance provides voltage drop for higher frequencies. Choosing right value for C1 is quite important as smaller capacitance brings some spikes at the base of the transistor and higher values of C1 limits the bandwidth as is shown in Fig. 3. It should be considered that R1 and R2 are chosen comparably larger than RL to reduce power consumption and have less influence on 50 ohm load impedance (Li and Tsai, 2006). Vdc controls the DC voltage of the base and emitter of Q2. Maximum single-ended output swing is calculated using the following equation:

$$\Delta V_{\text{out}} = V_{\text{out,OFF}} - V_{\text{out,ON}} = \left(2 \times V_{\text{CE,max}} + V_{\text{CE,sat}}\right) - 3 \times V_{\text{CE,sat}}. \quad (1)$$

In the present paper, the idea of using the intrinsic collector-base capacitance for the feedback network is extended into a

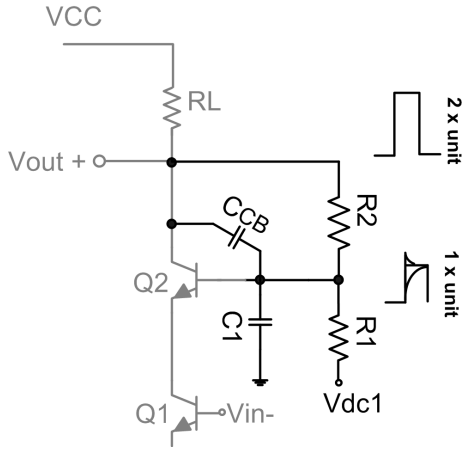

Figure 3. Simplified feedback network in half circuit differential mode.

three-stage cascode topology. This method can increase the maximum allowable output voltage swing while breakdown voltage is becoming less for upcoming downsized technologies. Now, maximum single-ended output swing is calculated using the following equation:

$$\Delta V_{\text{out}} = V_{\text{out,OFF}} - V_{\text{out,ON}} = \left(3 \times V_{\text{CE,max}} + V_{\text{CE,sat}}\right) - 4 \times V_{\text{CE,sat}}. \quad (2)$$

For an identical output swing, it can be proofed that the transistors with lower breakdown voltage, as almost two-thirds of the breakdown voltage in previous method, can be employed.

In the new implementation, the entire output swing must be divided equally among three transistors, so that the base of the two upper transistors must be pushed with the same phase as the output node (collector of Q3) with proper am-

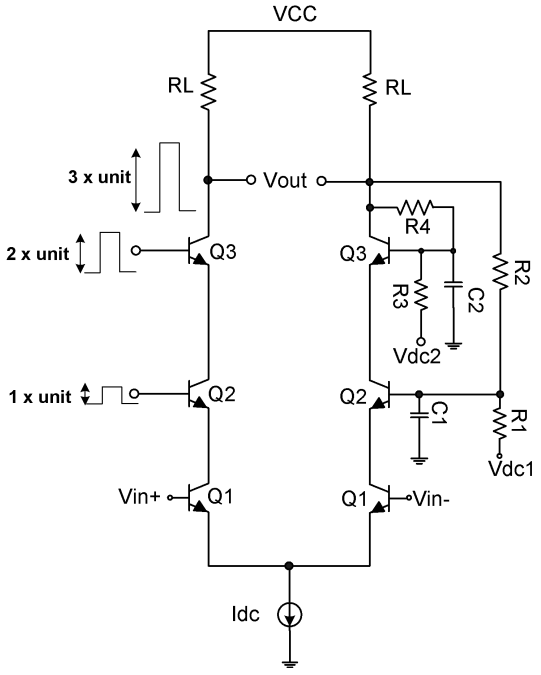

Figure 4. New modified multi-cascode topology with feedback network and corresponding voltage swing.

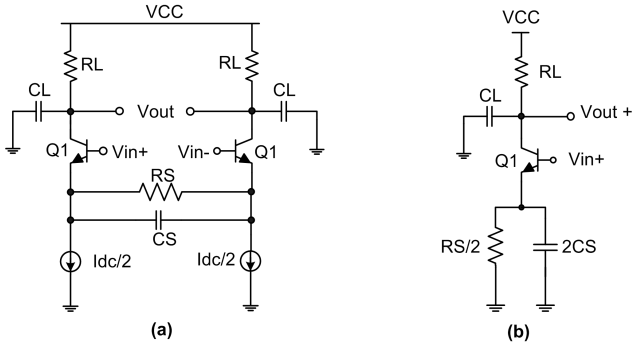

Figure 5. (a) Capacitance degeneration technique, **(b)** half circuit in differential mode.

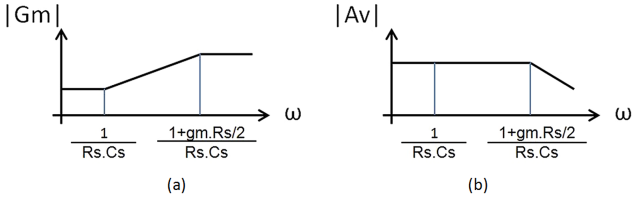

Figure 6. (a) Bandwidth of Gm, **(b)** overall system frequency response.

plitude. As is shown in Fig. 4, the feedback network must convey two-thirds, and one-third of the output signal for the base of Q2 and Q3 respectively, so as to drop one third of the whole output swing over each transistor. Here, the intrinsic collector-base capacitances, together with C1 and C2, provide a high frequency feedback network for Q1 and Q2.

2.2 Capacitance degenerative technique

In a differential configuration pair, a capacitance degeneration technique could improve bandwidth by adding a pole and a zero to the system (Razavi, 2012). The zero is designed to coincide with and cancel the pole of the system, and the 3dB bandwidth is determined by the second pole, which is away from the first one.

Figure 5 shows how the pole and the zero are added to the CML in a differential configuration. For half of the circuit in Fig. 5b, conductance of the common-emitter circuit is (Razavi, 2012):

$$G_m = \frac{g_m}{1 + g_m \times \left(\frac{R_s}{2} || \frac{1+g_m \times \frac{R_s}{2}}{R_S \times C_S} \right)}. \quad (3)$$

If one assumes that the output pole of the differential pair is dominated by $R_L \times C_L$, it would coincide with the added zero to cancel each other out, only if:

$$R_S \times C_S = R_L \times C_L. \quad (4)$$

Therefore, overall bandwidth of the system is extended to the second pole of the system, $(1 + g_m \times R_s/2)/(R_S \times C_S)$, as shown in Fig. 6.

3 Design and implementation

Using the concepts discussed in Sect. 2, a driver IC was implemented in SiGe 250 nm technology. This driver IC consists of two parts: a pre-driver stage and a main driver stage.

3.1 Pre-driver stage

Back-plane electrical signals fall within a certain standard range. This range is normally not strong enough to completely switch the current from one differential side to another one, a requirement for maximizing output swing and minimizing power consumption. In addition, a high amplitude input signal could bring the transistors into a deep saturation region where switching speed is reduced. Therefore, the pre-driver stage is placed before the main driver stage in order to prepare both the amplitude and the DC level of the input signal for the main stage driver IC.

As is shown in Fig. 7, the pre-driver stage is in a differential configuration, which consists of one common-emitter amplifier, followed by a common-collector stage. The common-emitter stage is designed to transfer low and high amplitude input signal to the specific level appropriate for driving the main stage driver IC. The main role of the common-collector stage is to provide proper impedance

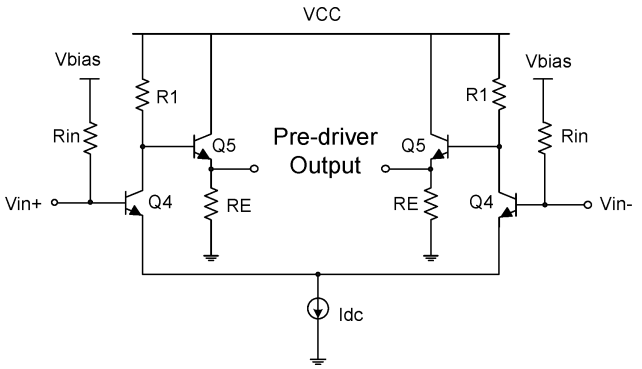

Figure 7. Proposed pre-driver stage.

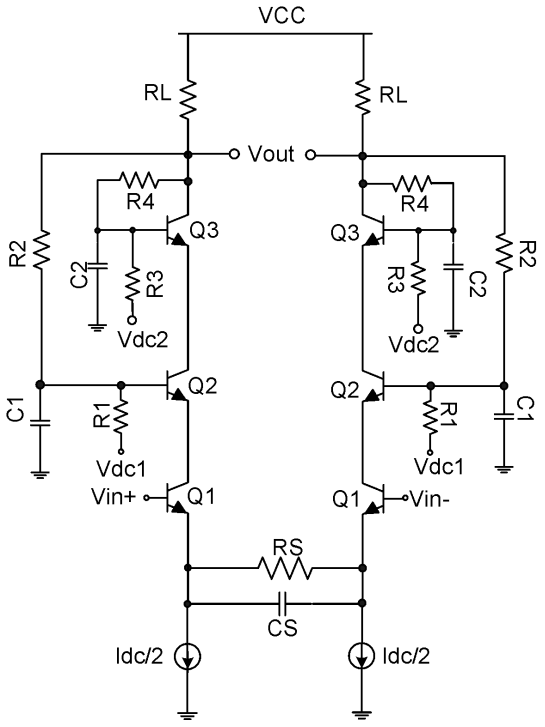

Figure 8. Proposed three stage cascode configuration.

for the common-emitter amplifier and cascade stage. In the present paper, the pre-driver output is designed to generate 500 mVp-p for the main driver stage.

3.2 Main driver stage

As target differential output swing is 4 Vp-p, supply voltage is increased to 4.5 V. Figure 8 shows how the main stage driver IC is constructed, it consists of a three-stage cascode and capacitance degeneration technique. A simulated eye diagram is depicted in Fig. 9, where its eye opening is 3.9 V at 14 Gbps.

Figure 10 shows how much voltage stress is on each device. This figure indicates that stress is less than 1.5 V, which

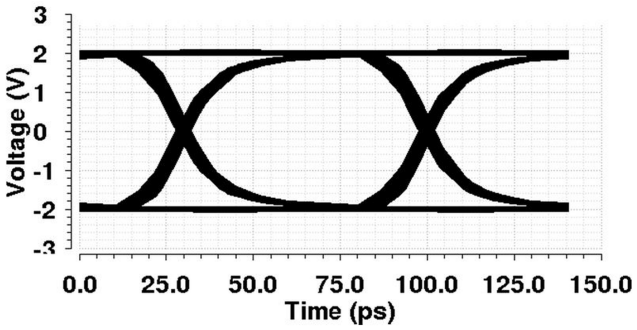

Figure 9. Simulated eye diagram of output signal at 14 Gpbs.

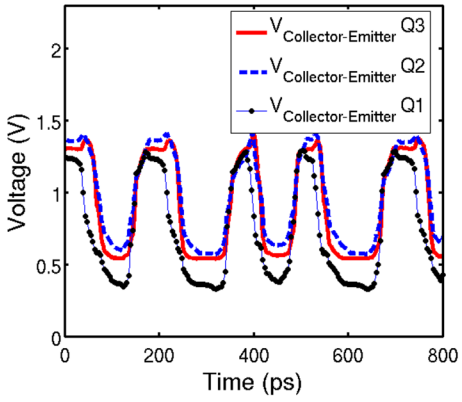

Figure 10. Simulated collector-emitter voltage stress in multi-cascode topology.

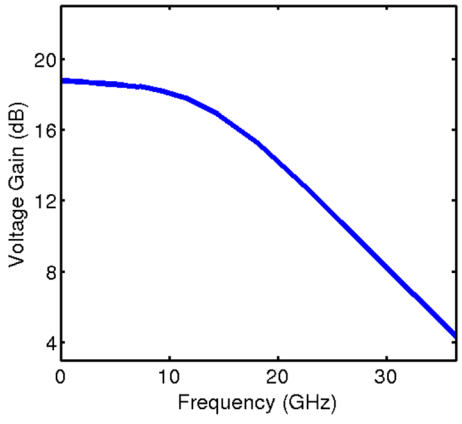

Figure 11. Simulated small signal voltage gain of driver IC.

is less than the breakdown voltage of 1.9 V in this technology, and it is shared quite evenly among devices as well. Figure 11 shows the small signal simulation of driver IC that indicates low frequency gain of 17 dB and corresponding 3 dB bandwidth of 14 GHz.

4 Conclusions

Silicon photonic technology offers a way to fully integrate optics into electronics in a single chip. A micro-ring resonator requires a comparatively high input voltage swing for proper performance (minimum ER). In the present paper, some techniques have been presented to obtain a high voltage swing in multi-Gbps data rate transmission. The technique that is introduced in this paper makes it possible to employ the transistors with lower breakdown voltage levels as two-third for high voltage swing application. Finally, the SiGe driver IC in 250 nm technology was investigated. Simulation results claim an output voltage swing of 3.9 Vp-p at 14 Gbps.

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