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# Charge pump design in 130 nm SiGe BiCMOS technology for low-noise fractional-N PLLs

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**Abstract.** This paper presents a numerical comparison of charge pumps (CP) designed for a high linearity and a low noise to be used in a fractional-N phase-locked loop (PLL). We consider a PLL architecture, where two parallel CPs with DC offset are used. The CP for VCO fine tuning is biased at the output to keep the VCO gain constant. For this specific architecture, only one transistor per CP is relevant for phase detector linearity. This can be an nMOSFET, a pMOSFET or a SiGe HBT, depending on the design. The HBT-based CP shows the highest linearity, whereas all charge pumps show similar device noise. An internal supply regulator with low intrinsic device noise is included in the design optimization.

## 1 Introduction

Fractional-N phase-locked loops (PLL) are widely used in radio frequency (RF) and high-speed digital applications. As opposed to integer-N architecture they avoid the trade-off between low phase noise and fine frequency step, which makes them especially attractive for radar systems discussed by Pohl et al. (2012), wireless sensor nodes as outlined by Ussmuller et al. (2009) or wireless base stations, see Osmany et al. (2013). In a PLL, a phase detector (PD) compares the reference phase with the divided output of a voltage-controlled oscillator (VCO). In integrated PLLs, the PD is usually composed of a phase-frequency detector (PFD) and a charge pump (CP). The CP circuit is used to inject into the low-pass filter (LPF) a current that is proportional to the phase difference at the PFD input. The PLL CP is essentially a switchable current source, in contrast to charge pumps known from power electronics where they serve as DC/DC converters. In a fractional-N PLL the divider ratio is often modulated by means of a sigma-delta modulator (SDM). Unlike the topologies employing accumulators, the SDM shifts the quantization noise to frequency offsets above the loop bandwidth. Unfortunately, this noise is folded down to low frequencies if the PD is nonlinear. This causes in-band phase noise and fractional spurs as discussed by De Muer and Steyaert (2003), Riley et al. (2003), Pamarti et al. (2004), Chien et al. (2004), Arora et al. (2005), and Hedayati and Bakkaloglu (2009). Besides this, the thermal device noise in the CP must be minimized for a low in-band phase noise as outlined by Levantino et al. (2013).

This paper compares different types of CPs with respect to linearity and device noise, where either an nMOSFET, a pMOSFET or a SiGe HBT are the crucial devices in the steady state. Since the investigated CP topologies suffer from a low output resistance, a low-noise voltage regulator is suggested in order to minimize the effect of supply noise.

## 2 PLL architecture for a low phase noise

In order to reduce CP noise, the PFD may drive two parallel CPs (Fig. 1). In this architecture, a fine-tuning loop comprising a LPF is combined with a coarse-tuning loop in parallel. The latter includes only a capacitor to ground between the CP and the VCO. A conventional LPF can be extended by adding a resistive voltage divider, so the fine tuning voltage is kept roughly at a constant level. This results in a stable VCO gain over the whole tuning range, which is preferable in order to keep the loop bandwidth at the same level. The fine-tuning varactor diode in the VCO can be made small, which improves the phase noise due to lower sensitivity. Also, the fine-tuning loop provides stability of the PLL. To preserve the wide tuning range a coarse-tuning loop must be applied. The coarse control voltage sweeps the entire tuning range and determines the VCO frequency. As shown by

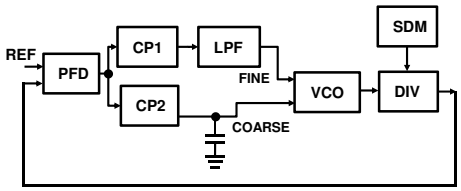


**Figure 1.** PLL architecture with two parallel tuning loops.

Herzel et al. (2003), if the dual-loop is correctly designed, a relatively large coarse loop capacitor does not deteriorate the settling speed of the PLL significantly.

The PD composed of a PFD and the two CPs converts the PLL phase error to currents. The PD nonlinearity has a strong effect in the presence of high-frequency quantization noise generated by SDM. It appears that this noise is folded down from large frequency offsets to the in-band region of the spectrum due to self-mixing in the nonlinear PD. Thus, mixed-down quantization noise cannot be filtered and deteriorates the close-in phase noise performance.

In modern fractional-N PLLs the main in-band noise sources include the reference buffer, PFD and the CP among which the latter is often the main contributor. It is due to CP device noise and already mentioned quantization noise folding. Since a fractional-N PLL often has wide loop bandwidth, the thermal noise of the CP becomes an issue.

As outlined by Herzel et al. (2010) large gate-source overdrive voltages $V_{\mathrm{ov}} = V_{\mathrm{GS}} - V_{\mathrm{th}}$ of the CP transistors may improve PD linearity and reduce device noise. Figure 2 shows a CP architecture where $V_{\mathrm{ov}}$ is maximized. The most critical transistor in Fig. 2 is M1, since it switches in the steady state. The pMOSFET M2 is active only during the settling of the PLL. In the steady state, a constant current $I_{\mathrm{OS1}}$ flowing onto the filter capacitance is delivered by the pMOSFET M4. Its value equals the average current flowing through M1. Therefore, the offset current $I_{\mathrm{OS1}}$ defines the ON time of the CP and the duty cycle in the steady state. The output of CP1 for VCO fine tuning is DC biased by a resistive voltage divider to stabilize the VCO gain and the phase noise spectrum. Let us assume that due to PVT variations the VCO frequency is shifted. In a standard PLL topology this would change the DC value of the VCO control voltage. Since in a typical integrated VCO the gain varies by a factor of three or more over the tuning range, the loop bandwidth would change drastically. To prevent this, the DC value of the fine tuning voltage can be fixed using our PLL architecture with two parallel CPs and a voltage divider for the fine-tuning loop. This approach has been discussed and verified experimentally by Osmany et al. (2013). If the DC value $\mathrm{VDD} \times \mathrm{RB1}/(\mathrm{RB1} + \mathrm{RB2})$ is close to the position of the VCO gain maximum, the PLL is robust with respect to variations of the device parameters with process, supply voltage and temperature (PVT). Because RB1 and RB2 are part of the loop filter they change the PLL transfer function. This makes the system more susceptible to low frequency noise of the VCO. If the values are too small the VCO flicker noise will be significant. As shown by Herzel et al. (2010), the values should be around 1 kΩ in case of HBT-based VCO and around 10 kΩ for MOS-based VCO. Since we will use SiGe-HBTs for the VCO in the future, we have used resistor values as small as $\mathrm{RB1} = \mathrm{RB2} = 1\,\mathrm{k\Omega}$ in this design. The typical PD characteristic shows strong nonlinearity around zero transition due to so-called *dead zone* region. It is caused by the finite speed of logic gates in the PFD. It also suffers from gain mismatch between the UP and DN current pulses. Both problems can be solved by utilizing a DC offset current source added at the outputs of both CPs. This shifts the steady state operating point of the PD to a region, where either M1 or M2 transistor responds to the phase changes at the PD input. This idea was originally suggested by Chien et al. (2004), where a DC current to ground was introduced. Osmany et al. (2013) have employed this architecture in a fractional PLL, where a robust low-noise performance was achieved over a wide tuning range. Depending on the sign of the offset current, either nMOSFETs or pMOSFETs are changing their output current pulses with time in the steady state. In a SiGe BiCMOS process, HBTs can be employed for CP design. They are promising owing to their fast switching speed. Unfortunately, they introduce shot noise which may easily exceed the thermal device noise of MOSFET-based CPs.

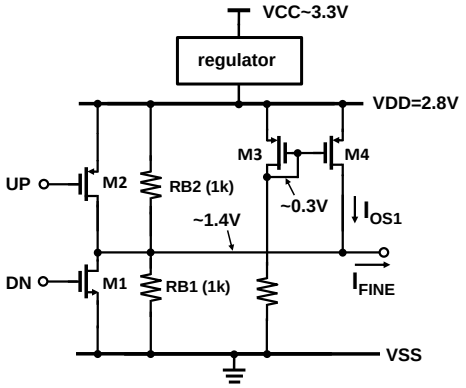


**Figure 2.** Charge pump CP1 for VCO fine tuning with DC output biasing and DC offset current.

The CP in Fig. 2 is relatively susceptible to supply noise. Therefore, it should be stabilized by an internal voltage regulator. Figure 3 shows a regulator which transforms a supply voltage VCC of about 3.3 V into a stable voltage of $\mathrm{VDD} = 2.8\,\mathrm{V}$. High-voltage MOSFETs with moderate gate lengths were employed for reliability. A bandgap reference (BGR) according to Brokaw (1974) was used to generate a temperature stable voltage of 1.1 V. The high-frequency supply noise is reduced by the low-pass filter between BGR and CMOS amplifier. This may be important if CP and VCO are operated from the same supply, since the PLL loop filter is bypassed then. Relatively large gate widths were used to re-

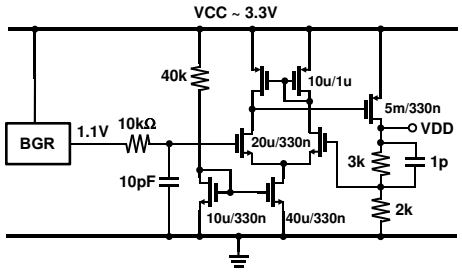


**Figure 3.** Low-noise voltage regulator for generation of a stable internal supply voltage of VDD = 2.8 V.

duce the device noise and to make the output voltage VDD independent of the load.

## 3 Charge pump figures of merit

### 3.1 Linearity

For an ideal phase detector the average CP output current $I$ is a linear function of the phase deviation $\phi$ from the steady-state average phase error $\phi_0$ at the PFD input. The linear PD gain is then given by

$$K_{\mathrm{PD}} = I_{\mathrm{CP}}/(2\pi), \tag{1}$$

where $I_{\mathrm{CP}}$ is the CP current in the ON state. For our PLL architecture with DC phase offset, the strong nonlinearities at low phase errors are avoided. Far from the origin, the PD input–output characteristic is smooth and can be approximated by a low-order polynomial. A parabolic fit may be enough here as shown by Herzel et al. (2010). Then we obtain

$$I = K_{\mathrm{PD}}\phi + \frac{\beta}{2} K_{\mathrm{PD}}\phi^2, \tag{2}$$

where $\beta$ represents the PD nonlinearity. The quantity $\beta$ is the normalized curvature of the PD input–output characteristic at the PD operating point and is given by

$$\beta = \frac{\mathrm{d}^2 I/\mathrm{d}\phi^2}{\mathrm{d}I/\mathrm{d}\phi}. \tag{3}$$

For a binary weighted CP, the quantity $\beta$ does not depend on the CP current, but only on the CP architecture. As shown by Herzel et al. (2010) the in-band phase noise due to SDM noise folding in the nonlinear PD is proportional to $\beta^2$ provided that a DC offset current is employed at the CP output for PD linearization. In other words, a reduction of $\beta$ by a factor of two reduces this phase noise contribution by 6 dB.

For the calculation of $\beta$ from the PD characteristic the phase error range should be centered at the desired static phase $\phi_0$ error which is typically between 36 and 72°. The $\phi$ range for curve fitting should be relatively narrow for a high accuracy but has to cover the phase excursions in the steady state.

### 3.2 Device noise

Commercial phase noise meters usually display the two-sided power spectral density (PSD) of the PLL output phase which is numerically close to the single-sideband phase noise. Therefore, we use the *two-sided* output current PSD of the CP current $S_{\mathrm{CP}}$ ($\mathrm{A}^2\,\mathrm{Hz}^{-1}$) for characterizing the CP device noise. The in-band phase noise PSD due to CP current noise is then given by

$$S_\phi = S_{\mathrm{CP}} \frac{N^2}{|K_{\mathrm{PD}}|^2}, \tag{4}$$

where $N$ is the feedback divider ratio. Note that circuit simulation tools usually output the one-sided current PSD ($2 \times S_{\mathrm{CP}}$ in our notation) which must be divided by two for our purpose.

Usually, $S_{\mathrm{CP}}$ is proportional to the CP current $I_{\mathrm{CP}}$ in the ON state. In fractional-N PLLs the noise-optimum loop bandwidth is typically between 300 kHz and 1 MHz. The largest contributions to the PLL jitter stem from the phase noise spectrum around the loop bandwidth. Since the noise corner frequency scales with the charge pump duty cycle as follows from Eq. (15) of Herzel et al. (2010), the CP noise corner is typically below the loop bandwidth. Therefore, CP flicker noise is usually less important than white noise (thermal, shot) in the CP.

Due to the long correlation time of $1/f$ noise compared to the sampling period at the PD input, the flicker noise PSD scales with $\alpha_{\mathrm{CP}}^2$ where $\alpha_{\mathrm{CP}}$ is the CP duty cycle. This was also discussed by Lacaita et al. (2007). Since white CP noise PSD scales with $\alpha_{\mathrm{CP}}$ only, the CP noise corner frequency is proportional to $\alpha_{\mathrm{CP}}$. For these noise sources, $S_{\mathrm{CP}}$ is proportional to the CP duty cycle $\alpha_{\mathrm{CP}} = T_{\mathrm{ON}}/T_{\mathrm{s}}$, where $T_{\mathrm{ON}}$ is the CP activation time and $T_{\mathrm{s}}$ is the sampling period at the PFD input. The static phase error at the PD input is related to the CP duty cycle by $\phi_0 = 360° \times \alpha_{\mathrm{CP}}$. In order to obtain a device noise figure of merit (FOM) which characterizes a CP *architecture* and is independent of $I_{\mathrm{CP}}$ and $\alpha_{\mathrm{CP}}$, we define a FOM by

$$\mathrm{FOM} = \frac{S_{\mathrm{CP}}}{I_{\mathrm{CP}}\,\alpha_{\mathrm{CP}}}, \tag{5}$$

which is given in units of $\mathrm{A\,Hz}^{-1}$.

### 3.3 Power supply rejection ratio

In addition to device noise, a CP may be affected by noise generated in other circuit blocks on the same die. In order to minimize the effect of this noise, the internal supply voltage VDD should be stabilized with respect to variations of the unregulated supply voltage VCC. Let us assume that a sinusoidal modulation of amplitude $V_{\mathrm{m}}$ and frequency $f_{\mathrm{m}}$ is added to the DC value of VCC. In this case, a signal of the same frequency but lower amplitude will appear at the internal supply voltage VDD. At the CP output the amplitude

will be further attenuated to a value $V_{\text{out}}$. The power supply rejection ratio of the regulated CP is defined as

$$\text{PSRR}(f_{\text{m}})(\text{dB}) = 20\log(V_{\text{m}}/V_{\text{out}}). \quad (6)$$

## 4 Charge pump design

The CP design was performed in a 130 nm SiGe BiCMOS technology described by Rücker et al. (2010). This technology features high-performance HBTs with peak transit frequencies $f_{\text{T}}$ of 240 GHz, maximum oscillation frequencies $f_{\text{max}}$ up to 330 GHz, and breakdown voltages $\text{BV}_{\text{CEO}}$ of 1.7 V along with high-voltage HBTs ($f_{\text{T}} = 50$ GHz, $f_{\text{max}} = 130$ GHz, $\text{BV}_{\text{CEO}} = 3.7$ V). Short-channel MOSFETs with 130 nm gate length are available for digital processing. Moreover, high-voltage MOSFETs with a minimum gate length of 330 nm are available. These MOSFETs are better suited for CP design since a larger voltage range can be used for VCO tuning, compared with the short-channel MOSFETs. For the used technology the threshold voltage $V_{\text{th}}$ is about 0.6 V for the high-voltage MOSFETs, which results in overdrive voltages as large as 2.7 V for a supply voltage of 3.3 V.

In the following, we consider three CPs. The first one is the nMOS-based CP shown in Fig. 2. Here, only the nMOSFET M1 changes its output current pulses in the steady state, while a constant UP current is delivered by the current mirror. The regulator derives a stable internal supply voltage of VDD = 2.8 V from a global supply voltage of VCC ≈ 3.3 V. The gate potential of the pMOSFETs in the current mirror is as low as 0.3 V to minimize their noise contribution *for a given current*. Note that both the CP and the current mirror transistors are in triode region. The current mirror with its output transistor in triode region provides a stabilized current with respect to variations of the threshold voltage $V_{\text{th}}$. In triode region the drain current depends linearly on the overdrive voltage $V_{\text{GS}} - V_{\text{th}}$, whereas in saturation it is a square-law characteristic. However, the drain current in this configuration depends strongly on the drain-source voltage, but this is not critical here due to the resistive voltage divider at the CP output. Eventually, the value of the DC offset current (and the resulting PD offset) can always be adjusted to compensate for PVT variations by using binary weighted current sources. In order to stabilize the static phase error, a classical cascode CP and an offset current source with a high output resistance should be used in the coarse tuning loop. Here, large gate-source voltages are not required, since the noise of CP2 will be minimized by the large external capacitor shown in Fig. 1.

The second CP version is pMOS-based, where the UP current in Fig. 2 is replaced with a DOWN current. This architecture has been used by Osmany et al. (2013) in a low-noise fractional-N PLL synthesizer. In that paper, binary weighted CPs were combined, where the disable functions were realized by multiplexers at the CP inputs and large MOSFET switches in the primary branches of the current mirrors. In this paper, we consider a constant-current CP for simplicity. The inclusion of switches for binary weighted digital current control is easily possible. By using a 4-bit binary weighted offset current source the phase offset can be easily adjusted.

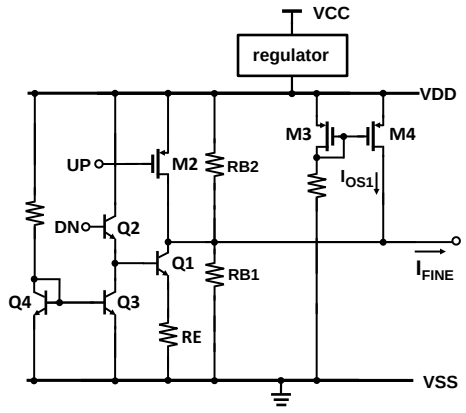


**Figure 4.** Charge pump CP1 for VCO fine tuning using SiGe HBTs.

The third CP considered here is shown Fig. 4. Here, the nMOSFET in Fig. 2 was replaced with a SiGe-HBT Q1 including bias resistance RE. Moreover, a level shifter was introduced at the DOWN input to convert the CMOS signal into an HBT compatible signal.

In the next section, the three CP versions are optimized by circuit simulations with respect to linearity and device noise. Subsequently, the resulting figures of merit are compared.

## 5 Numerical results

### 5.1 Phase detector linearity

The linearity analysis was performed by a transient analysis using Virtuoso Analog Design Environment. A 100 MHz reference was used at the PFD input, corresponding to a sampling period of $T_{\text{s}} = 10$ ns. In a parametric simulation the phase error at the PFD input was varied between 36 and 72°. This corresponds to a CP duty cycle of 10–20 % and a CP activation time $T_{\text{ON}}$ between 1 and 2 ns. For each phase error the charge pump current was averaged over the period of 10 ns. Subsequently, the first and second derivative were numerically calculated by using MATLAB. The resulting linear PD gain $K_{\text{PD}}$ and the nonlinearity parameter $\beta$ were then obtained from Eqs. (1) and (3), respectively. For the latter, a linear fit to the first derivative was calculated to obtain a mean value for the normalized curvature.

The output current pulses are shown in Fig. 5 for different delays at the PFD input for the nMOS-based. The delays where adjusted such that the CP duty cycle varied from 10 to 20 %. The oscillatory behavior at the edges is not critical as long as the plateau is flat. In this case, the area below the curve is a linear function of the delay, and the normalized curvature $\beta$ is small, as desired.

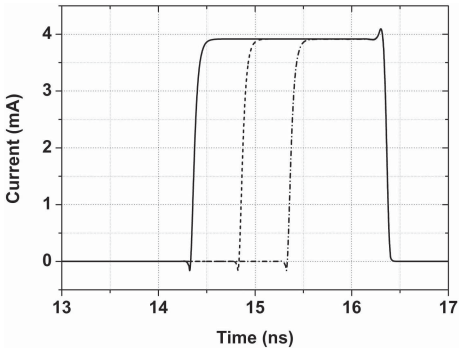


**Figure 5.** Output current pulses for three different pulse widths $T_{ON} = 1$, 1.5 and 2 ns for nMOS-based CP.

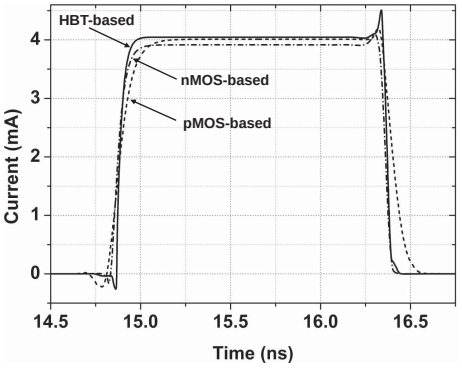


**Figure 6.** Output current pulses for the three CPs.

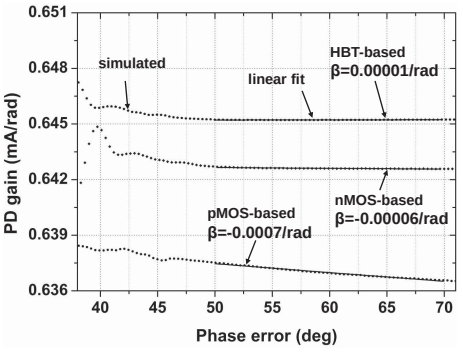


**Figure 7.** Phase detector gain as a function of phase error at the PD input for the three CPs.

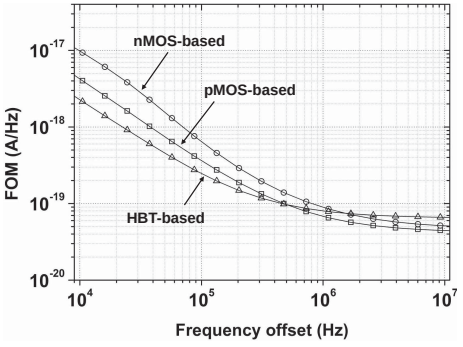


**Figure 8.** Device noise FOM according to Eq. (5) for the three CPs including DC offset currents and voltage regulator.

A single current pulse for the three investigated CPs is presented in Fig. 6. In order to obtain a high linearity, the turn-on and turn-off times should be as short as possible. It is obvious that the HBT-based CP provides the steepest current slopes. Thus, the highest linearity should be expected for this configuration. The pMOS-based CP shows the worst behaviour due to the low hole mobility.

The PD gain $\mathrm{d}I/\mathrm{d}\phi$ is shown in Fig. 7, where we have also included the pMOS-based CP for completeness. According to Eq. (3) the derivative of the PD gain needs to be estimated for the calculation of $\beta$. The mean slope of the curves depends on the phase region where the fit is calculated. In order to cover the phase excursions in the steady state, a range of $\pm 10^\circ$ around the mean value is adequate as deduced from the calculated phase distribution in a typical fractional-N PLL presented by De Muer and Steyaert (2003). The linear least-squares fits to the simulated gain curves between 50 and 70° result in the estimated values for $\beta$ at the static phase offset of $\phi_0 \approx 60^\circ$ as given in Fig. 8. Obviously, the HBT-based CP results in the highest PD linearity.

### 5.2 Device noise

The noise analysis was performed by a periodic steady-state (PSS) analysis followed by a periodic noise analysis using Virtuoso Analog Design Environment. The device noise analysis includes the low-noise voltage regulator shown in Fig. 3. We used a CP peak current of $I_{CP1} = 4$ mA and an offset current of $I_{OS1} = 0.6$ mA. For the coarse tuning loop these values were reduced by a factor of 10. The ratio $I_{OS1}/I_{CP1} = I_{OS2}/I_{CP2}$ of 0.15 corresponds to a CP duty cycle of 15 % and a static phase error of 54° at the PD input.

The FOM is depicted in Fig. 8 as a function of frequency. We observe a plateau in Fig. 8 in the lower MHz range related to white noise sources. In reality, this plateau extents into the kHz range since the $1/f$ noise corner frequency of the CP is proportional to the duty cycle $\alpha_{CP}$, as explained above. This effect is not correctly reflected by the simulated phase noise spectrum, since long-term correlation effects are not properly included in the simulator. Based on this knowledge, we use an offset of 1 MHz in the circuit simulations as a representative value for the CP phase noise plateau. However, flicker noise from the offset current source is simulated correctly. Therefore, we observe relatively large $1/f$ noise for HBT-based CP even though the $f_c$ of the used bipolar transistors is much lower (lies in 10 kHz range).

At large frequency offsets the phase noise due to device noise is highest for the HBT-based CP. It is composed of the shot noise of the bipolar HBTs in the CP core includ-

**Table 1.** Performance comparison of charge pumps.

| switching device | $\beta$ ($\phi_0 = 60°$) | FOM (at 1 MHz) | PSRR (at 1 MHz) | DC current (including biasing) |
|---|---|---|---|---|
| nMOSFET | −0.00006/rad | $9 \times 10^{-20}$ A Hz$^{-1}$ | 30 dB | 2.9 mA |
| pMOSFET | −0.0007/rad | $7 \times 10^{-20}$ A Hz$^{-1}$ | 30 dB | 2.9 mA |
| SiGe HBT | 0.00001/rad | $8 \times 10^{-20}$ A Hz$^{-1}$ | 30 dB | 4.3 mA |

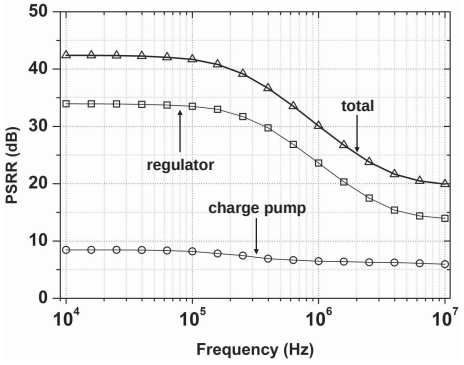


**Figure 9.** PSRR for the nMOS-based CP.

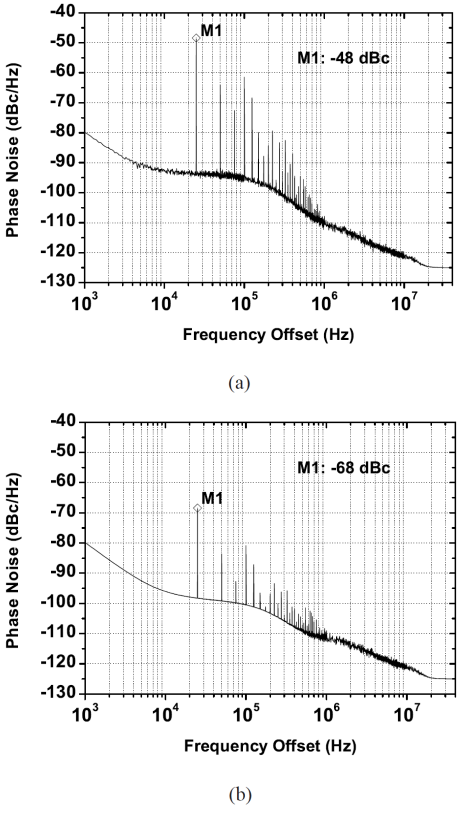


**Figure 10.** Simulated output sectrum for **(a)** $\beta = 0.01$ and **(b)** $\beta = 0.001$.

ing level shifter, the thermal noise of the CMOS offset current, the shot noise of the BGR, and the thermal noise of the voltage regulator. In order to estimate the phase noise plateau due to CP noise we consider a numerical example. We assume a PLL output frequency of 10 GHz corresponding to a feedback divider ratio of $N = 100$, a CP peak current of $I_{\mathrm{CP1}} = 4$ mA, and a CP duty cycle of $\alpha_{\mathrm{CP}} = 15$ %. Then we obtain from Eqs. (4), (5) and (1) a phase noise level of $1.2 \times 10^{-12}$ rad$^2$ Hz$^{-1}$ for the HBT-based CP at an offset frequency of 1 MHz. In decibel, this corresponds to $-119$ dB rad$^2$ Hz$^{-1}$. Despite the large duty cycle, this value is significantly lower than the measured in-band phase noise of state-of-the-art low-noise fractional-N PLLs as published by Osmany et al. (2013).

### 5.3 Supply noise rejection

The PSRR is depicted in Fig. 9 as a function of the modulation frequency for the nMOS-based CP. Here, we have also shown the PSRR of the regulator only and of the CP only. The poor PSRR of the CP results from the voltage divider at the output. However, in conjunction with the regulator the overall rejection is above 30 dB at frequencies up to 1 MHz. At frequency offsets above 1 MHz the CP noise is of little relevance, since it is effectively filtered by the low-pass filter in a PLL.

### 5.4 Performance comparison

The results are summarized in Table 1. All numbers in the table include the CP output biasing resistors, the offset current and the voltage regulator. As evident from the table, the nMOS-based CP shows the lowest device noise, whereas the HBT-based CP results in the highest PD linearity. In integer-N PLLs linearity is not relevant, and the MOS-based CP is the best solution. For fractional-N PLLs the best choice with respect to phase noise and fractional spur performance is the HBT-based CP for its high linearity. The second best solution is the nMOS-based CP for its better linearity, compared with the pMOS-based CP. Owing to the level shifter at the input the HBT-based CP dissipates slightly more current. We have simulated the PLL phase noise spectrum using the model of Herzel et al. (2010). The quantization noise was modeled as described by De Muer and Steyaert (2003). The simulated spectra for two values of $\beta$ are shown in Fig. 10. The improvement of the in-band phase noise by the higher PD lin-

earity is only moderate due to other phase noise contributions. By contrast, the in-band spurs are reduced by as much as 20 dB, since the folded quantization noise is proportional to $\beta^2$.

## 6 Conclusions

We have designed and compared three CPs in SiGe BiCMOS intended for low-noise fractional-N PLLs, where either MOSFETs or SiGe-HBTs were used as switching elements in the steady state. Using large gate-source voltages in conjunction with DC offset currents, linearity and device noise of the CMOS CPs were optimized. The inclusion of SiGe-HBTs for faster current switching is expected to reduce the in-band phase noise of a fractional-N PLLs due to the excellent phase detector linearity.

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