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Design of a 0.13 µm SiGe Limiting Amplifier with 14.6 THz Gain-Bandwidth-Product

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Abstract. This paper presents the design of a limiting amplifier with 1-to-3 fan-out implementation in a 0.13 µm SiGe BiCMOS technology and gives a detailed guideline to determine the circuit parameters of the amplifier for optimum high-frequency performance based on simplified gain estimations. The proposed design uses a Cherry-Hooper topology for bandwidth enhancement and is optimized for maximum group delay flatness to minimize phase distortion of the input signal. With regard to a high integration density and a small chip area, the design employs no passive inductors which might be used to boost the circuit bandwidth with inductive peaking. On a RLC-extracted post-layout simulation level, the limiting amplifier exhibits a gain-bandwidth-product of 14.6 THz with 56.6 dB voltage gain and 21.5 GHz 3 dB bandwidth at a peak-to-peak input voltage of 1.5 mV. The group delay variation within the 3 dB bandwidth is less than 0.5 ps and the power dissipation at a power supply voltage of 3 V including output drivers is 837 mW.

1 Introduction

The demand for data rates of tens to hundreds of Gbit s^{-1} in multimedia communication systems, e.g. for video on demand or cloud computing, has significantly accelerated the development of broadband receiver components over the last few years. In fiber-optic communication systems for long-haul communication, strong emphasis has thereby been placed on the design of limiting amplifiers. They are key components in such systems and are required to compensate the attenuation of the fiber to enable reliable decision making at the receiver side (Razavi, 2003). In this work, practical design considerations for a multi-stage Cherry-Hooper amplifier (Cherry and Hooper, 1963) are presented. The amplifier is designed for multi-THz gain-bandwidth product (GBW) performance and linear phase behaviour. A high gain is realized by cascade connection of several single-stage amplifiers and a high bandwidth by exploitation of negative feedback with emitter followers. To ensure minimum phase distortions of the input signal, the limiting amplifier is optimized for maximum group delay flatness. Even though the gain magnitude response can be constant up to a given frequency, severe phase distortions can occur below this frequency, if the group delay flatness is insufficient (Säckinger, 2005).

Section 2 describes the circuit architecture, Sect. 3 explains the design of the limiting amplifier and Sect. 4 presents the simulation results with a comparison to the state of the art. Section 5 concludes the paper.

2 Architecture

The proposed multi-stage limiting amplifier is depicted in Fig. 1. To use the limiting amplifier not solely for amplification of small input signals (e.g. output voltage of a preceding transimpedance amplifier), but also as a general signal distribution device (e.g. clock distribution to a multi-chip IQ analog-to-digital converter), the amplifier exhibits one main and two auxiliary output paths. Each path consists of three cascaded Cherry-Hooper amplifiers and one output driver. The Cherry-Hooper (CH) amplifiers exploit emitter follower (EF) feedback for bandwidth enhancement. For interfacing reason, emitter followers are inserted in between these amplifiers to lower their common-mode output levels. This is required to prevent Q_1 and Q_2 from being operated in the saturation region. The output driver is realized by two differential pairs that are decoupled by an EF pair. For best speed performance, the driver components are optimized for high slew rate. Each output driver is biased by an independent cur-

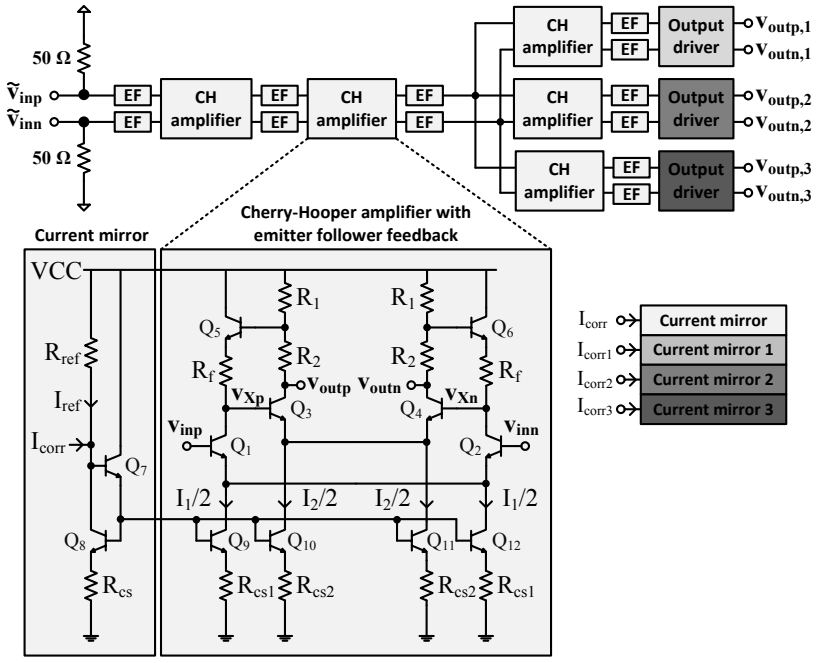

Figure 1. Limiting amplifier architecture.

rent mirror, which can be controlled externally by a parameter analyser to adjust the differential output voltage swing of the amplifier to any desired output level within a restricted range. By default, the voltage swing of the amplifier is set to $1.2\,V_{ppk}$. If only one output branch is required, the auxiliary output drivers can be completely turned off to decrease the power consumption of the limiting amplifier by approximately 46 %. For best symmetry of each signal path and to minimize bandwidth restrictions due to the large capacitive load of the output drivers, the 1-to-3 fan out implementation is realized after the third EF pair.

3 Design considerations

The proposed limiting amplifier in Sect. 2 is designed for multi-THz GBW performance and is optimized for maximum group delay flatness. To give more insight into the design approach in this work and to highlight critical design issues, the Cherry-Hooper amplifier in Fig. 1 is investigated with a large-signal analysis in this section. Strong emphasis is thereby set on the gain calculation of the amplifier to restrict the values of the circuit components to a finite set. Based on the obtained results, the design methodology for the proposed limiting amplifier, especially at high frequency operation, is explained. Under the assumption that base currents are negligibly small and that all transistors are identical, the differential output voltage of the Cherry-Hooper amplifier in Fig. 1 can be expressed by

$$\begin{aligned} v_{\text{out}} &= v_{\text{out}p} - v_{\text{out}n} \\ &\cong (R_1 + R_2) \cdot \underbrace{(i_{\text{C4}} - i_{\text{C3}})}_{=i_{\text{D43}}} \\ &= (R_1 + R_2)\, \underbrace{I_2 \tanh\left(-\frac{v_X + r_{\text{e}} i_{\text{D43}}}{2V_{\text{T}}}\right)}_{=i_{\text{D43}}} \end{aligned} \tag{1}$$

with

$$\begin{aligned} v_X &= v_{Xp} - v_{Xn} \\ &\cong \left(R_f + r_{\text{e}}\right) \underbrace{(i_{\text{C2}} - i_{\text{C1}})}_{=i_{\text{D21}}} + R_1 \underbrace{(i_{\text{C4}} - i_{\text{C3}})}_{=i_{\text{D43}}} + \underbrace{(v_{\text{be6}} - v_{\text{be5}})}_{=-v_{\text{in}} - r_{\text{e}} i_{\text{D21}}} \\ &\approx R_f \underbrace{I_1 \tanh\left(-\frac{v_{\text{in}} + r_{\text{e}} i_{\text{D21}}}{2V_{\text{T}}}\right)}_{=i_{\text{D21}}} \\ &\quad + R_1 \underbrace{I_2 \tanh\left(-\frac{v_X + r_{\text{e}} i_{\text{D43}}}{2V_{\text{T}}}\right)}_{=i_{\text{D43}}} - v_{\text{in}}. \end{aligned} \tag{2}$$

The parameters $i_{C<N>}$ and $v_{be<N>}$ denote the collector current and base-emitter voltage of transistor N, respectively. The thermal voltage of the transistors is described by V_{T} and the internal HBT emitter resistance by r_{e}. First-order approximation of Eqs. (1) and (2) and subsequent derivative with respect to v_X and v_{in} deliver a voltage gain of

$$G = \frac{\mathrm{d}v_{\mathrm{out}}}{\mathrm{d}v_X} \cdot \frac{\mathrm{d}v_X}{\mathrm{d}v_{\mathrm{in}}} \tag{3}$$
$$\cong \underbrace{\frac{-(R_1+R_2)\,I_2}{2V_{\mathrm{T}}+r_{\mathrm{e}}I_2}}_{=G_2} \cdot \underbrace{\frac{-(2V_{\mathrm{T}}+r_{\mathrm{e}}I_2)\left(R_f I_1+2V_{\mathrm{T}}+r_{\mathrm{e}}I_1\right)}{(2V_{\mathrm{T}}+r_{\mathrm{e}}I_1)\,(R_1 I_2+2V_{\mathrm{T}}+r_{\mathrm{e}}I_2)}}_{=G_1}.$$

If the bias currents of the inner and outer differential pair are equal, i.e. $I_1 = I_2 = I_0$, Eq. (3) can be simplified to

$$G \cong \left(1+\frac{R_2}{R_1}\right) \cdot \frac{1+\frac{R_f I_0}{2V_{\mathrm{T}}+r_{\mathrm{e}}I_0}}{1+\frac{2V_{\mathrm{T}}+r_{\mathrm{e}}I_0}{R_1 I_0}} \tag{4}$$

If R_f, $R_1 \gg \frac{2V_{\mathrm{T}}}{I_0} + r_{\mathrm{e}}$ and noting that the voltage gain of a differential pair with bias current I_0 and load resistance R_f is

$$G_{\text{diff. pair}} \cong \underbrace{\frac{I_0}{2V_{\mathrm{T}}+r_{\mathrm{e}}I_0}}_{=g_{\mathrm{m}}} R_f, \tag{5}$$

Eq. (4) can be expressed by

$$G \cong \left(1+\frac{R_2}{R_1}\right) \cdot G_{\text{diff. pair}} \tag{6}$$

Equation (6) illustrates the importance of the resistance R_2 in the amplifier. Without R_2 the Cherry-Hooper amplifier exhibits the same voltage gain as a differential pair with bias current I_0 and load resistance R_f; with R_2 the gain increases by factor $1 + R_2/R_1$. Figure 2 compares the theoretical voltage gain according to Eq. (4) against simulation results for a fixed differential output voltage swing of 600 mV. To obtain a good gain prediction, the HBT emitter resistance used for calculation is slightly chosen larger than in the foundry specification, as not all HBT parasitics are covered in Eq. (4) as in the circuit simulation. Equation (4) indicates that the larger the feedback resistance R_f or the resistance ratio R_2 / R_1 is chosen, the larger is the voltage gain G and vice versa. Increasing G by solely increasing R_2 / R_1 while keeping $R_1 + R_2$ and R_f constant, however, only works effectively within a restricted ratio range (Greshishchev and Schvan, 1999), as shown in Fig. 2.

A specific voltage gain can be realized by different parameter choices. An amplifier with 8 dB gain, for instance, can be designed by choosing the feedback and load resistances to (1) $R_f = 20\,\Omega$, $R_1 = 20\,\Omega$ and $R_2 = 80\,\Omega$ or (2) $R_f = 50\,\Omega$, $R_1 = 50\,\Omega$ and $R_2 = 50\,\Omega$. While both parameter choices result in the same gain and power dissipation, the amplifier exhibits different frequency behaviour (e.g. bandwidth, group delay, etc.) depending on the chosen circuit parameters (Holdenried et al., 2004). The difference in frequency behaviour can be significant and is explained in the later course of this paper with more detail. By solving Eq. (4) for R_f,

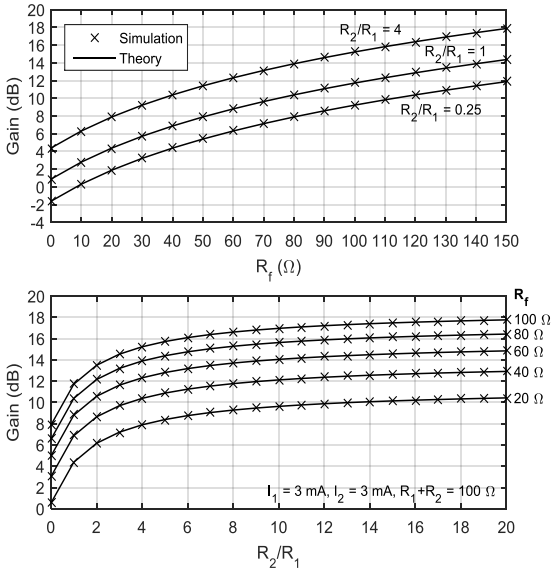

Figure 2. Theoretical and simulated low-frequency voltage gain of CH-amplifier.

all possible parameter combinations for a given gain can be calculated as

$$R_f = \frac{G\cdot(2V_{\mathrm{T}}+r_{\mathrm{e}}I_0)\,(R_1 I_0+2V_{\mathrm{T}}+r_{\mathrm{e}}I_0)}{(R_1+R_2)\;I_0^2} - \frac{2V_{\mathrm{T}}}{I_0} - r_{\mathrm{e}} \tag{7}$$

If the bias current I_0 and the differential output voltage swing of the amplifier

$$V_{\mathrm{sw}} = 2\,(R_1+R_2)\;I_0 \tag{8}$$

are set first at the beginning of the amplifier design, e.g. to meet a desired power budget or to bias the HBTs at maximum peak f_T for maximum g_{m} and linearity, Eq. (7) can be rearranged to

$$R_f = G\cdot(2V_{\mathrm{T}}+r_{\mathrm{e}}I_0)\,\frac{V_{\mathrm{sw}}+2\left(\frac{R_2}{R_1}+1\right)(2V_{\mathrm{T}}+r_{\mathrm{e}}I_0)}{V_{\mathrm{sw}}I_0\left(\frac{R_2}{R_1}+1\right)} \tag{9}$$
$$-\frac{2V_{\mathrm{T}}}{I_0} - r_{\mathrm{e}}$$

Equation (9) strongly eases the amplifier design by limiting the parameter choices for a given voltage gain. The results are illustrated in Fig. 3 for different voltage gain implementations and a fixed voltage swing of 600 mV. To realize a voltage gain of 40 dB with three cascaded Cherry-Hooper amplifiers, the gain of a single amplifier is set to 13.34 dB in this work. Based on the calculated parameter choices, the set with the most flat group delay frequency behaviour is determined by simulation. To illustrate the different frequency behaviours of the calculated parameter sets, three different

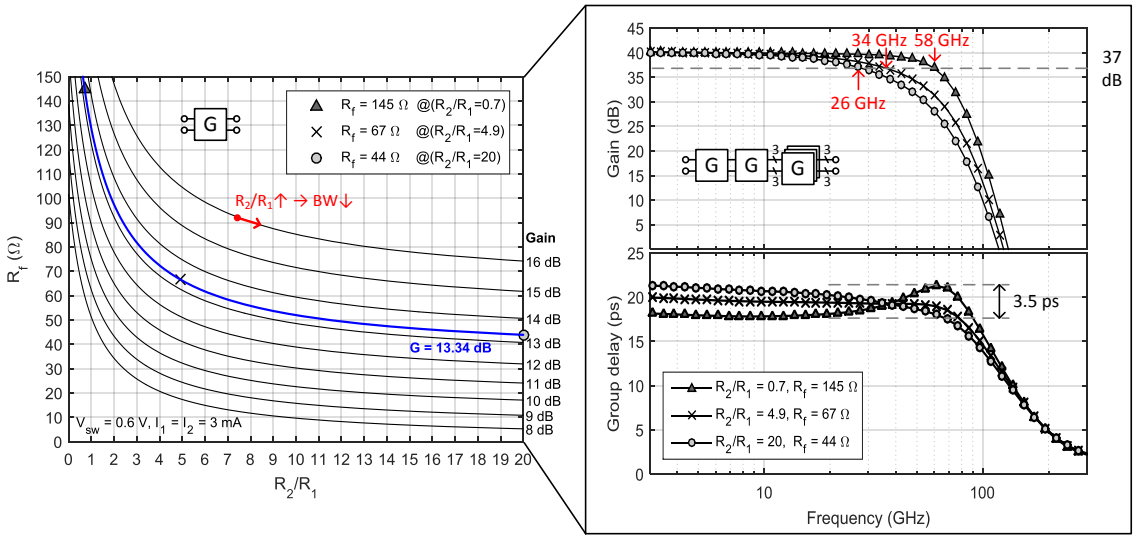

Figure 3. Theoretical parameter choices for given voltage gains and simulated gain and group delay performances.

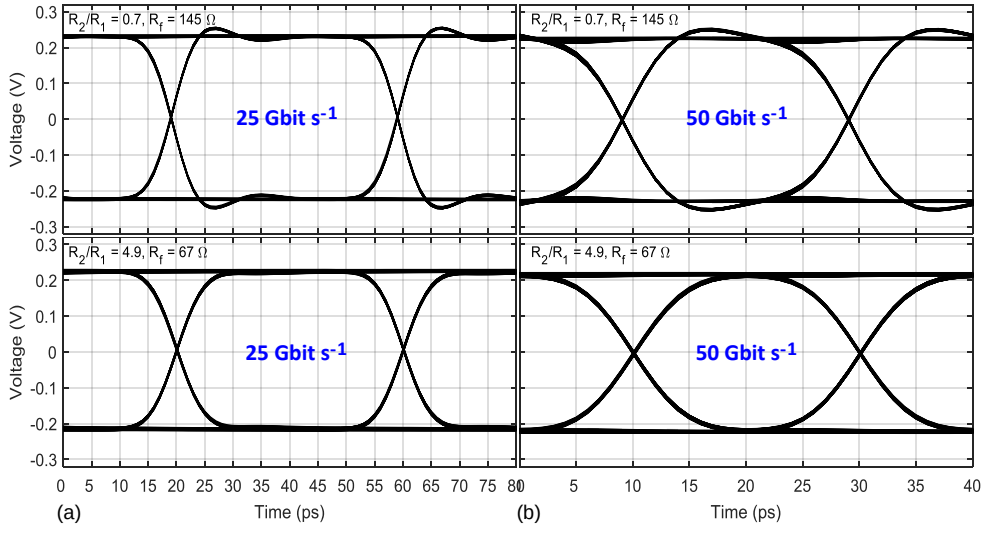

Figure 4. Simulated eye diagrams for 5 mV_{ppk} PRBS input at 25 Gbit s^{-1} **(a)** and 50 Gbit s^{-1} **(b)**.

parameter combinations are exemplarily compared against each other. By design, the voltage gain, output voltage swing and power dissipation are the same in all three cases. The gain magnitude and group delay of the cascaded Cherry-Hooper amplifiers depict which influence the circuit parameters have on the amplifier operation. From a sole speed perspective, the parameter set with the smallest resistance ratio R_2 / R_1 should be taken to achieve a high bandwidth with gain peaking. From a linearity perspective, however, a larger resistance ratio is more beneficial, since gain peaking distorts the phase of the amplifier, which hence results in large group delay variations. Figure 4 depicts the eye diagram of the amplifier configuration for the parameter set with maximum bandwidth ($R_f = 145\,\Omega$, $R_2 / R_1 = 0.7$) and compares it against the parameter set, which exhibits maximally flat group delay ($R_f = 67\,\Omega$, $R_2 / R_1 = 4.9$). For simulation, a 25 and 50 Gbit s^{-1} pseudo-random bit sequence (PRBS) with 5 mV differential peak-to-peak voltage swing is used as an input signal. Due to the larger group delay variations, the first parameter set results in a stronger misshaped eye diagram than the second set, even though its gain magnitude response is relatively flat. For the final design of the Cherry-Hooper stages in this work, therefore the second parameter set is used. For measurement purposes, additional output drivers are connected in series, which increases the gain of the amplifier to approximately 56 dB on a RLC-extracted post-layout level. The dimensioning of the output drivers is described in Grözing et al. (2010) and is therefore omitted in

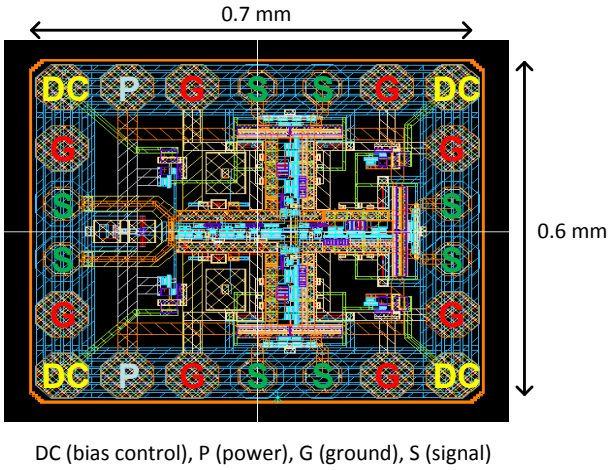

Figure 5. Layout of limiting amplifier with pad configuration.

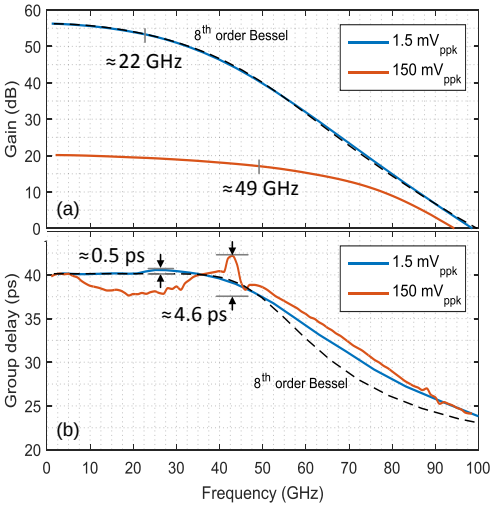

Figure 6. Simulated voltage gain and group delay performance for different input voltages on post-layout level.

this paper. The simulation results of the complete amplifier are shown in Sect. 4.

4 Simulation results

The limiting amplifier in Sect. 2 is designed in a 0.13 µm SiGe BiCMOS technology which offers 300 GHz f_T and 500 GHz f_{max} for its HBTs. Figure 5 depicts the layout of the amplifier and its pad configuration. The chip has a size of $0.7 \times 0.6\,mm^2$ and dissipates 837 mW from a 3 V power supply. Without output drivers, the power dissipation is 170 mW. To ensure best layout symmetry and approximately equal output delays, the 1-to-3 fan out implementation is realized in a symmetrical T-shape. The layout of the multi-stage limiting amplifier is RLC-extracted with a 2.5-D field solver and the HBTs are simulated with VBIC (Vertical Bipolar Intercompany) models. Since the transistors in this design are not biased far beyond their peak f_T collector currents, VBIC and HICUM (High Current Model) are considered to provide equal transistor modelling quality. For very high collector current densities, HICUM is regarded to give more realistic results.

Section 4.1 summarizes the simulated results in the frequency domain and Sect. 4.2 the results in the time domain.

4.1 Frequency domain

Figure 6 depicts the simulated gain and group delay of the limiting amplifier in Fig. 5 for different input peak-to-peak voltages and compares the results against the frequency response of an ideal amplifier with finite bandwidth and linear phase characteristic. As the Cherry-Hooper amplifiers and output drivers approximately behave like second-order systems (Holdenried et al., 2004) each, the limiting amplifier in Sect. 2 is modelled with an 8th order system. To accommodate the linear phase behaviour (or flat group delay) of the amplifier in the model, a Bessel filter is used. The comparison gives a brief upper limit estimation to which frequency a flat group delay can maximally be achieved with a finite amplifier bandwidth. An ideal amplifier with 56.6 dB DC gain and 21.5 GHz 3 dB bandwidth (GBW = 14.6 THz) exhibits for instance a flat group delay of up to 39 GHz. The proposed limiting amplifier with the same gain and bandwidth approximately covers the same frequency band, which comes close to the ideal case. Due to layout parasitics, the group delay variations (GDV) within this band are, however, about ±0.25 ps. The GBW of 14.6 THz is simulated at a differential peak-to-peak input voltage of 1.5 mV_{ppk}. With regard to the simulated input-referred voltage noise of 450 μV_{rms}, this is close to the theoretical minimum input voltage, with which an amplification of the signal can be verified under noise considerations (Greshishchev and Schvan, 1999). As the input swing further decreases, noise will predominate and signal amplification is not measurable anymore. For large input voltages, the gain compresses and phase distortion increases. At a differential input voltage of 150 mV_{ppk}, the gain decreases to 20 dB, while the 3 dB bandwidth more than doubles, as harmonic powers at high frequencies increase due to the output voltage limitation of the amplifier. The GDV, as a result of the non-linear amplification, degrades to ±2.3 ps.

Table 1 compares the GBW and GDV of the proposed limiting amplifier against state-of-the-art amplifiers. Simulations indicate that the design can improve the GBW by at least 16 % and the GDV by factor 20. It should be noted here, however, that the results are simulated and that measurement results can differ despite careful design and intensive simulations on post-layout level with 2.5-D parasitic extraction field solvers, as accurate modelling of the HBT parasitics, especially of the base resistances and diffusion capacitances, is very difficult close to f_T.

Table 1. Comparison to state-of-the-art amplifiers.

	This work (Post-Layout)	Grözing et al. (2010)	Ding et al. (2014)	Li et al. (2014)	Ahmed et al. (2015)	Gharib et al. (2012)	Gharib et al. (2015)
Technology	0.13 µm SiGe	0.35 µm SiGe	0.13 µm SiGe	0.13 µm SiGe	0.13 µm SiGe	0.35 µm SiGe	0.35 µm SiGe
Bandwidth (GHz)	21.5	21	86	78	105	32.5	25
DC gain (dB)	56.6	41	20	17.5	12	32	54
GBW (GHz)	14560	2400	860	585	418	1350	12500
Power (mW)	449*	420*	89	105	300	120	180
Inductive peaking	No	No	Yes	Yes	No	No	No
Group delay (ps)	40	–	15	35	13	–	–
Group delay variation (ps)	±0.25	–	±6	±5	±6	±10	–

* Auxiliary output paths are deactivated.

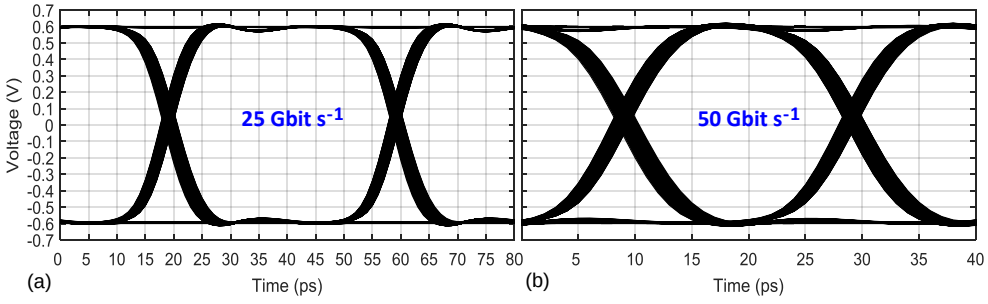

Figure 7. Simulated eye diagrams for 5 mV_{ppk} 2^{31}-1 PRBS input at 25 and 50 Gbit s^{-1} on post-layout level.

4.2 Time domain

Figure 7 depicts the simulated eye diagrams for a differential 5 mV_{ppk} PRBS input signal at 25 and 50 Gbit s^{-1}. A high gain and low group delay variations within a wide bandwidth ensure symmetrical eye diagrams of the output signal of the amplifier. The systematic peak-to-peak jitter for the 50 Gbit s^{-1} PRBS is about 2.4 ps and is mainly caused by routing asymmetry in the layout and voltage offsets of the cascaded amplifiers.

5 Conclusion

This paper presents the design of a multi-stage Cherry-Hooper amplifier in a 0.13 µm SiGe BiCMOS technology and describes a new generalized design methodology to find optimum circuit parameters for given design requirements. The proposed design methodology is based on gain derivations of the amplifier that are supported by parameter sweep simulations. To restrict the values of the circuit components to a finite set, all possible circuit parameter combinations for a given voltage swing and gain are first determined by calculation. These parameter combinations are then used as a fundament for circuit dimensioning to given high-frequency design requirements (e.g. flat group delay). The design approach can theoretically be exploited for fully-automated circuit synthesis of Cherry-Hooper amplifiers. Due to its simplicity and accurate circuit equation estimations, the design approach can be implemented by simple algorithms.

The proposed limiting amplifier incorporates a 1-to-3 fan-out implementation for binary signal distribution and achieves a simulated gain-bandwidth product of 14.6 THz with 56.6 dB low-frequency voltage gain and 21.5 GHz 3-dB bandwidth on a RLC-extracted post-layout level. The maximum group delay variation within the 3 dB bandwidth is less than 0.5 ps. Intensive simulations indicate that the amplifier can improve the GBW of state-of-the-art amplifiers by at least 16 % and the group delay variation by factor 20. The large GBW and flat group delay are achieved at cost of lower bandwidth to prevent phase distortions due to gain peaking.

Data availability. The Matlab code and simulation data that support the findings of this study are available in Zenodo with the identifier https://doi.org/10.5281/zenodo.580519 (Park et al., 2017).

Competing interests. The authors declare that they have no conflict of interest.

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