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A low complexity digital frequency calibration with high jitter immunity for ultra-low-power oscillators

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Abstract. This paper presents a highly efficient digital frequency calibration method for ultra-low-power oscillators in wireless communication systems. This calibration method locks the ultra-low-power oscillator's output frequency to the reference clock of the wireless transceiver during its send- and receive-state to achieve frequency stability over process variation and temperature drifts. The introduced calibration scheme offers high jitter immunity and short locking periods overcoming frequency calibration errors for typical ultra-low-power oscillator's by utilizing non-linear segmented feedback levels. In measurements the proposed calibration method improves the frequency stability of an ultra-low-power 32 kHz oscillator from 53 to 10 ppm $°C^{-1}$ over a wide temperature range for temperature drifts of less than $1 °C s^{-1}$ with an estimated power consumption of 185 nW while coping with relocking periods of 7 ms.

1 Introduction

The demand for low power RF communication architectures in today's rapidly growing markets as the internet of things (IoT), smart utility networks (SUN), wireless sensor networks (WSN) and cyber-physical systems (CPS) has increased to support long battery lifetime on a stringent energy budget. These architectures utilize an advanced duty-cycle scheme either based on wake-up timer for a time slot based communication protocol (TDMA) or on wake-up receiver to reduce power consumption on system level. Both architecture types require a stable ultra low power (ULP) low frequency clock source with absolute frequency accuracy to implement a reliable and power saving duty cycle scheme in TDMA systems or for precise baseband data sampling in a wake-up receiver as discussed by Burdett (2015).

In prior works, several efforts have been made to achieve absolute frequency accuracy over process variation and temperature drifts.

However, the conventional approach of using an external low frequency crystal (XTAL) as demonstrated by Yoon et al. (2016) increases the external component count and therefore increases the total cost of the wireless communication system. Other approaches proposed by Paidimarri et al. (2013) and Griffith et al. (2014) achieve absolute frequency accuracy by costly factory calibration and also require high temperature stability of the used ULP oscillator leading to increased power consumption in the oscillator design. More application tailored solutions utilize existing clock signals in a complex system with absolute frequency accuracy but different frequency and design requirements as a reference for an on-chip calibration method. Shrivastava and Calhoun (2012) propose a periodic recalibration scheme based on an existing clock signal to achieve absolute frequency accuracy and compensate frequency drifts over temperature changes relaxing the design requirements of the ULP oscillator's temperature stability leading to potentially lower power consumption and lower area. Nonetheless, this calibration technique uses a successive approximation algorithm which typically have high jitter sensitivity degrading the frequency calibration accuracy. These on-chip calibration methods like FIR-filter based calibration loops suffer from contradictory requirements of low bandwidth of the loop to suppress jitter resulting in high settling time and the calibration accuracy degradation by increased noise.

This work presents a calibration technique overcoming the contradictory requirements of high jitter immunity to guarantee the optimum calibration word and fast settling time by using multi-level bang-bang algorithm. This technique has been used in Scholl et al. (2016) to dramatically increase the
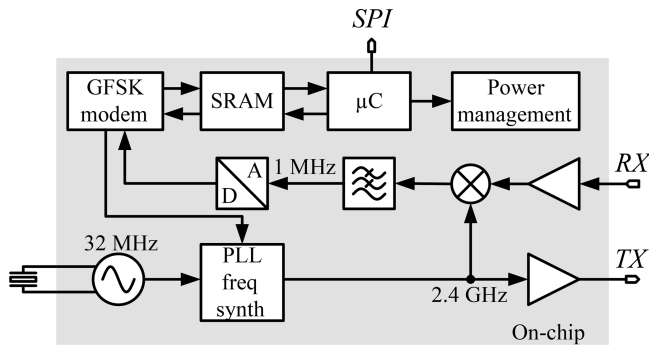
Figure 1. System overview of a wireless transceiver.

Figure 2. Typical operation scheme of wireless communication systems.

performance and especially the temperature stability of an ULP oscillator. The non-linear segmentation of the calibration error in the feedback path allows a large feedback gain for large frequency error leading to a fast settling but also has a very small feedback gain once the frequency tuning word has settled to achieve high jitter tolerance. For a faster relocking in active states of the TRX the calibration algorithm is synchronized to the ULP oscillator to reduce the error signal in the first calibration cycle of the relocking to a minimum. The low complexity of the proposed calibration technique leads to an efficient digital implementation with low power consumption.

2   Ultra low power clocks in wireless transceivers

In Fig. 1 a block diagram of a simplified wireless transceiver (TRX) is depicted. The frequency synthesizer (PLL) is used to generate a local oscillator (LO) signal to down convert the received RF signal to the baseband which is filtered and digitized for further signal processing and demodulation. Additionally, the PLL is used to generate a modulated RF signal which is amplified and fed to the antenna during transmit state. To meet the strict requirements for absolute frequency accuracy of the transmitted signal and also for the LO signal, resulting from the dense channel allocation in the limited RF band, a precise crystal oscillator is used in every TRX as an absolute frequency reference. This oscillator's frequency depends on the exact application and communication standard but is typically in a range between 10 and 50 MHz.

Since many of these wireless TRX are used in devices which are battery operated there is a high demand to reduce average power consumption of the TRX to extend lifetime of the devices. Therefore, advanced duty cycle schemes have been implemented for TDMA protocols exploiting the deterministic timeslot for transmit and receive operation and powering down most circuits of the TRX in between. In these systems it is critical to determine the time point before the next dedicated timeslot to turn-on all necessary circuits. This determination is realized with a wake-up timer counting clock cycles of either the main crystal oscillator or of a dedi-
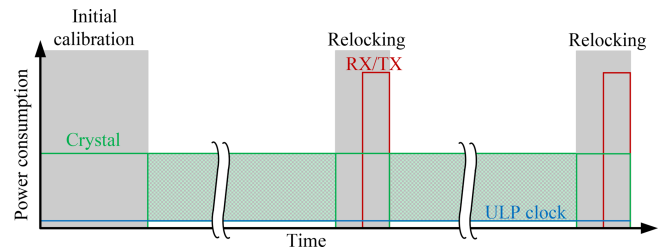
cated ULP oscillator typically in the range of 32 and 64 kHz. This low frequency ULP oscillator is implemented to measure a timespan with a certain required accuracy while having much lower power consumption compared to the crystal oscillator. Thus the main crystal oscillator is only active during the send- and receive-state of the TRX if a dedicated ULP oscillator is implemented and the power consumption can be further reduced as visualized in Fig. 2. In this phases the main crystal oscillator can also be used as reference frequency to calibrate the ULP oscillator to overcome frequency deviations due to process variation. The red curve indicates the power consumption of all blocks necessary to receive or transmit data as these are only active during the dedicated time slots. The green curve gives the power consumption of the crystal oscillator while the blue curve represents the power consumption of the ULP oscillator. In light green the area representing the energy which can be saved by implementing an ULP oscillator is visualized.

3   Frequency calibration methods

In Table 1 different implementation approaches as analyzed by Franklin et al. (2014) for frequency calibration loops are compared for the most relevant performance characteristics in this application as design complexity, area demand, power consumption and a performance indication for the tradeoff between frequency accuracy and settling time.

Analog filter based frequency calibration loops offer low power consumption due to the full custom transistor level design flow but also suffer from the complexity and various design choices of this design flow. This designs and especially the low frequency analog filter, necessary to suppress the high jitter of the clock signal to achieve high frequency accuracy, demand for large area. Furthermore, it is challenging to apply very low duty-cycling ratios resulting from the short locking periods in which the reference clock is available to this calibration loop due to the analog output voltage drift caused by leakage currents.

IIR filter based frequency calibration loops overcome these output voltage drift issues because digital circuits and digital signal representation are inherently tolerant to leakage current. The downside of this calibration approach are
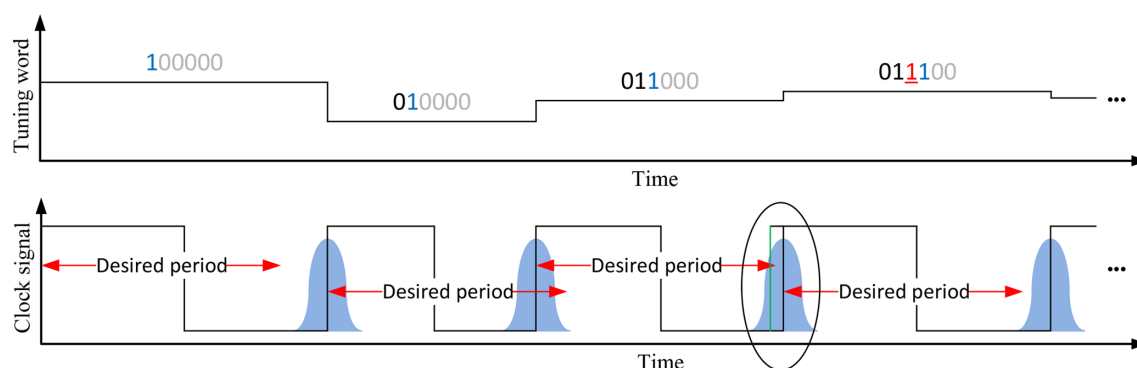
Figure 3. Frequency calibration cycle of SAR logic for oscillators with high jitter.

Table 1. Comparison of different calibration methods.

	Complexity	Area	Power	Performance
Analog filter based	−	−	+	+
IIR filter based	−	0	−	+
Bang-bang algorithm	+	+	0	−
SAR algorithm	0	+	0	0

the digital multiplications needed in the IIR filter resulting in high power consumption.

The bang-bang algorithm is based on a very simple principle as it increases the digital tuning word by a fixed step size if the frequency of the ULP oscillator is too high and decreases the tuning word by the same amount if the output frequency is too low. Due to its simplicity this calibration approach can be implemented with high power and area efficiency. On the other hand the fixed step size leads to an unfavorable tradeoff between settling time, calibration accuracy and jitter immunity making this approach not suitable for applications with low duty-cycle ratios.

Frequency calibration with a SAR algorithm can also be implemented very area and power efficient because it is using binary decisions based on the sign of the frequency deviation and there are no calculations with the actual frequency deviation word. Additionally, the utilized binary search approach, which can also be seen as an inverse binary weighted step size, leads to a fast settling of this calibration approach. A critical drawback of this approach is the missing relocking capability leading to a full calibration cycle in every relocking period independent from the actual frequency deviation. Even more critical are the facts that the SAR logic is very prone to jitter because the step size is not adapted to the current frequency error and an error at the beginning of the calibration cycle cannot be corrected in later steps heavily degrading the calibration accuracy. Fig. 3 illustrates a calibration cycle of a SAR logic for an oscillator with high jitter and it also demonstrates how the jitter affects the calibration accuracy. The upper graph shows the output tuning word of the SAR logic controlling the frequency of an oscillator whereas

the lower graph gives the actual clock signal of the oscillator in the black curve, the desired period length in red arrows, a Gaussian distributed jitter probability in blue and the clock signal with jitter as a green edge within the circle. In the first two calibration steps the algorithm performs as expected by testing if the oscillator's frequency is too high or low compared to the desired value for the tuning word "100000" and "010000". In the third step the frequency tuning word is set to "011000" and the frequency is measured to be high because the ULP oscillator's clock edge occurs earlier due to jitter. Therefore the third bit is falsely detected as a "1" and consequently all following bits will be detected as "0" because the oscillator's output frequency is too low.

4 Multi-level bang-bang algorithm

To overcome the limitations of the SAR and bang-bang algorithm but also avoiding the power consumption of the IIR filter based calibration a multi-level bang-bang algorithm as shown in Fig. 4 is presented in this work. The non-linear segmentation allows a large feedback gain for large frequency error leading to a fast settling but also has a very small feedback gain once the frequency tuning word has settled to achieve high jitter tolerance.

The frequency error Z_{err} is calculated from the ULP oscillator's clock and the reference clock from the crystal oscillator of the wireless transceiver by a frequency detector consisting of a counter, a register and a digital subtraction. The counter is clocked with the reference clock and its value is stored in a flip-flop at the synchronized rising edge of the ULP oscillator's clock signal. To fasten the relocking during active state of the reference clock signal the counter's restart bit is synchronized to the ULP oscillator's clock signal minimizing the first calculated error value of each relocking cycle. The frequency error Z_{err} is calculated from the stored counter value by subtraction a constant word Z_{freq}, determining the frequency ratio between the ULP clock and the reference clock. Afterwards this error signal is non-linearly segmented into three different levels representing a correc-
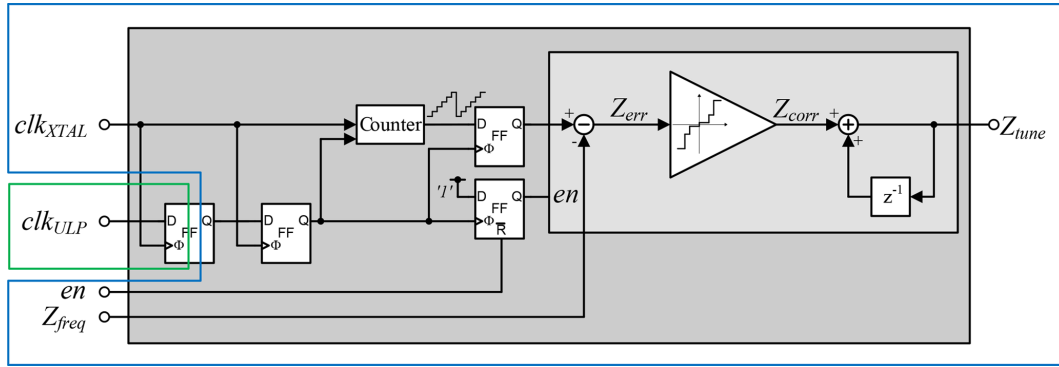
Figure 4. Implementation of the proposed digital multi-level bang-bang calibration logic.

tion word Z_{corr}. This correction word is added to the tuning word Z_{tune} as the output of the calibration logic. By choosing the segmentation levels as given in Eq. (1) the segmentation can be very efficiently implemented in digital logic.

$$Z_{corr} = \begin{cases} +32, & \text{if} \quad 32 \leq Z_{err}, \\ +1, & \text{if} \quad 16 \leq Z_{err} < 32, \\ +\frac{1}{32}, & \text{if} \quad 0 \leq Z_{err} < 16, \\ -\frac{1}{32}, & \text{if} \quad -16 \leq Z_{err} < 0, \\ -1, & \text{if} \quad -32 \leq Z_{err} < -16, \\ -32, & \text{if} \quad Z_{err} < -32 \end{cases} \quad (1)$$

To achieve optimal performance the smallest level covers all errors Z_{err} caused by jitter of the ULP oscillator after settling of the calibration loop to ensure the smallest feedback gain with highest calibration accuracy. This error range can be estimated from the 3σ-range of the rms-jitter of the oscillator. Additionally, errors resulting from non-linearities or changing of the feedback gain are avoided by this choice of range because only the smallest level occurs after settling. The larger segmentation levels represent a trade-off between stability of the feedback loop and settling time of the calibration.

To further validate the choice of error range and segmentation levels simulation results for the relocking time of different bang-bang algorithm implementations are given in Table 2. In simulation a standard bang-bang calibration loop using only the smallest segmentation level of the other implementations achieving 20.8 ms relocking time is compared to two different multi-level bang-bang calibration loops. One of these multi-level loops uses a linear segmented feedback path resulting in 7.9 ms relocking time and the other one uses a non-linear segmentation as implemented in the presented design achieving 6.6 ms relocking time.

To avoid problems related to clock domain crossing the ULP oscillator's clock signal is synchronized to the reference clock domain by a two flip-flop synchronizer avoiding metastability of this signal. Besides this synchronization all other signals, registers and computations are in the clock do-

Table 2. Comparison of different bang-bang algorithm implementations.

	Relocking Time
Bang-bang	20.8 ms
Linear feedback multi-level bang-bang	7.9 ms
Non-linear feedback multi-level bang-bang	6.6 ms

main of the reference clock avoiding problems with clock domain crossing in this design.

5 Measurement results

The presented digital frequency calibration method has been designed and evaluated using synthesized hardware description language on an Virtex-5 FPGA platform. For measurements the FPGA is connected to a custom designed ULP low frequency digitally controlled oscillator (DCO) on a separate ASIC fabricated in a 130 nm technology which was presented by Scholl et al. (2016). The ULP oscillator's clock signal and a 32 MHz reference clock signal are connected to the FPGA while the 9 bit frequency tuning word from the calibration loop is written from the FPGA to the custom ASIC with a 8 MHz SPI interface. The latency caused by communication over a SPI interface instead of parallel wired connection to the analog circuitry is neglectable in the measurement.

Additional synthesis results for a co-integrated on-chip implementation of the presented digital frequency calibration in the 130 nm technology estimate a power consumption of 26.4 μW during relocking and 5120 μm^2 occupied area. The estimated power consumption during relocking P_{cal} translates to an average power consumption P_{avg} of

$$P_{avg} = P_{cal} \cdot \frac{T_{cal}}{T_{cycle}} = 26.4 \, \mu\text{W} \cdot \frac{7 \, \text{ms}}{1 \, \text{s}} = 185 \, \text{nW} \quad (2)$$

for a periodic 7 ms relocking cycle every second.

A micrograph of the 32 kHz ULP DCO used in measurement is shown in Fig. 5, occupying 100 μm × 140 μm area.

Table 3. Performance comparison of ULP oscillators with different calibration approaches.

	Joonhyung et al. (2010)	Jeong et al. (2014)	Shrivastava and Calhoun (2012)	Paidimarri et al. (2013)	Griffith et al. (2014)	Scholl et al. (2016) (This Technique)
Process	180 nm	180 nm	130 nm	65 nm	65 nm	130 nm
Area	0.017 mm^2	0.245 mm^2	0.250 mm^2	0.032 mm^2	0.015 mm^2	0.014 mm^2
Frequency	31.24 kHz	0.011 kHz	100 kHz	18.5 kHz	33 kHz	32 kHz
Power	360 nW	5.8 nW	150 nW	120 nW	190 nW	80 nW
Accuracy	4000 ppm °C^{-1}	45 ppm °C^{-1}	14 ppm °C^{-1}	22 ppm °C^{-1}	38 ppm °C^{-1}	10 ppm °C^{-1}, 53 ppm °C^{-1}*
Temp Range	−45–80 °C	−10–90 °C	20–70 °C	−40–90 °C	−20–90 °C	10–100 °C
Cal. Method	Multi-Stage Bang-Bang	NA	SAR Alg.	Factory Cal.	Factory Cal.	Presented Technique

* Without periodic relocking. NA: not available.
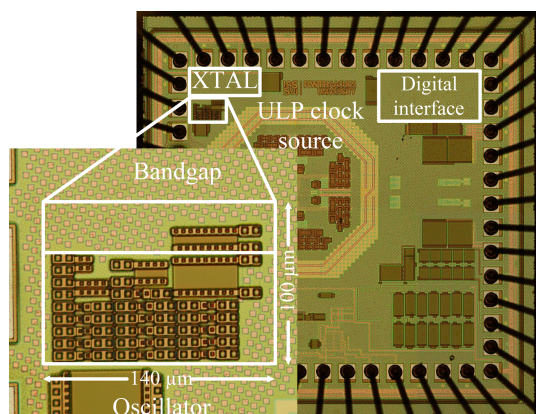
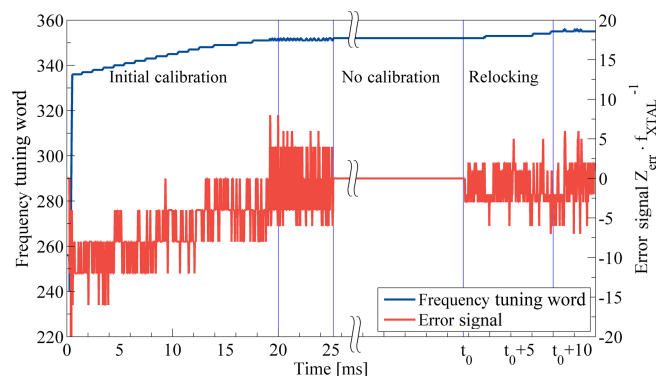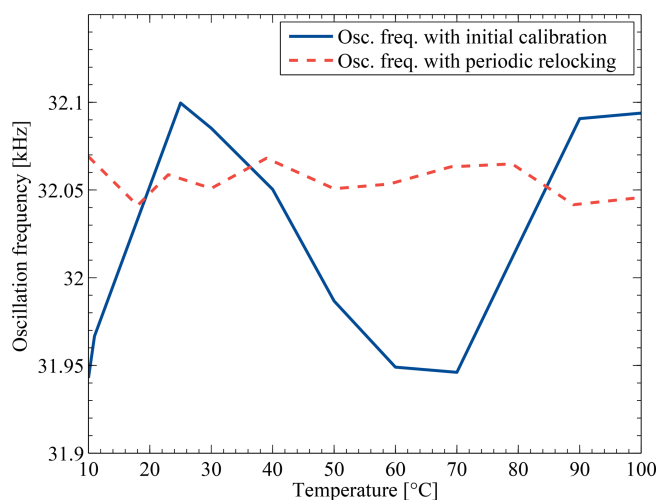**Figure 5.** Chip micrograph of the low frequency ULP DCO used in the measurement setup.

Figure 6. Measured calibration cycle with initial locking and relocking after provoked frequency error.

Figure 7. Measured improvement in the temperature stability of the ULP oscillator's frequency with initial calibration and periodic recalibration for small temperature gradients of 1 °C s^{-1}.

The power consumption of this ULP oscillator is 80 nW from a 1.2 V supply voltage. This design has a measured rms-jitter of 1.0 µs resulting from the current-source-based oscillator topology demanding for high jitter immunity of the digital frequency calibration method.

Figure 6 shows a measured calibration cycle with initial locking and relocking after a provoked frequency error demonstrating fast relocking capability and high jitter immunity. The blue curve illustrates the output Z_{tune} of the digital frequency calibration loop whereas the red curve represents the Z_{err} signal in the digital logic indicating the current frequency error. During the 20 ms initial calibration phase different feedback levels can be observed as the slope of the frequency tuning word changes. After provoking a small frequency error the digital calibration loop relocks the oscillator's output frequency within 7 ms.

In Fig. 7 the measured output frequency of the ULP oscillator over a temperature range from 10 to 100 °C and temperature gradients of 1 °C s^{-1} is shown. The blue line represents the measured oscillator's output frequency with an initial calibration cycle whereas the red dash-dotted line shows the output frequency after periodic relocking every second. The presented periodic relocking calibration scheme improves the ULP oscillator's frequency stability over temperature from 53 to 10 ppm °C^{-1}.

Table 3 gives a comparison between other published works and the ULP low frequency clock generation from Scholl et al. (2016) utilizing the proposed and analyzed frequency calibration method to improve the system performance. With the frequency calibration method discussed in this work the previous published clock generation system im-

proves the temperature stability of the oscillator from 53 to $10\,\mathrm{ppm}\,^\circ\mathrm{C}^{-1}$ and therefore exhibit the temperature stability of other published works for similar temperature ranges with lower power consumption.

6 Conclusions

A highly efficient, low effort digital frequency calibration method with high jitter immunity specially tailored to ultra-low-power oscillators in wireless communication systems has been presented. By overcoming typical issue of ULP oscillators and enabling fast relocking with a non-linear segmented feedback in the calibration loop, the temperature stability of a custom designed ULP oscillator has been improved from 53 to $10\,\mathrm{ppm}\,^\circ\mathrm{C}^{-1}$ for small temperature gradients of $1\,^\circ\mathrm{C}\,\mathrm{s}^{-1}$ and periodic relocking after 1 s. Measurements validate the design choices and demonstrate fast and precise settling for ULP oscillators with high jitter output signals while maintaining low power consumption and area. Due to its simplicity and flexibility, it can be added as a straight-forward temperature stability enhancement technique for ULP clock sources in wireless communication systems.

Data availability. The data are available upon request.

Competing interests. The authors declare that they have no conflict of interest.

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