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10-bit tracking ADC with a multi-bit quantizer, variable step size and segmented current-steering DAC

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Abstract. This paper presents a 10-bit tracking ADC using a multi-bit quantiser and a segmented current-steering DAC. The quantiser allows a dynamical adjustment of the step size dependent on the input signal waveform. This mitigates the limited slew rate of delta encoded ADCs. Energy consumption induced by 1 LSB ripple is removed by the quantiser. The segmented current-steering DAC allows simple control, good monotonicity and improved transient response when compared to previous design as well as potential power reduction.
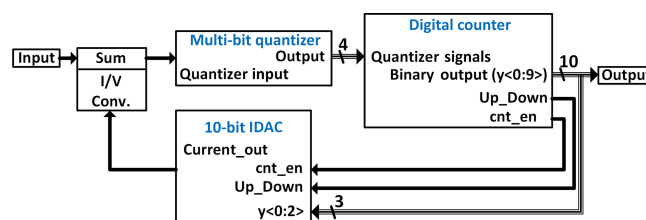
Figure 1. Toplevel of the proposed tracking ADC.

1 Introduction

Several different topologies exist for ADCs. The type of tracking ADCs is located between nyquist rate and delta sigma ADCs according to their sample rates. The main advantage is, that one conversion per clock cycle is achieved. The main drawbacks of tracking ADCs are the limited slew rate and the output ripple. The slew rate can be enhanced by increasing the clock rate (Huang, 2013a), which would also increase the energy consumption. A better option is to increase the step size of the ADC. The presented ADC (Fig. 1) has a sample rate of up to $50\,\mathrm{MS\,s^{-1}}$ and a variable step size of 1 or 2 LSB steps which is achieved by a multi-bit quantiser (Shaker, 2010). The ripple of the output signal is caused by toggling the DAC by 1 LSB every clock cycle when the input amplitude varies less than 1 LSB. This problem is also solved with the quantiser used here.

A current-steering DAC can be used in the feedback path. To achieve higher resolutions with good performance it is necessary to segment the feedback DAC (Moody, 2014). In the ADC presented here the DAC is segmented into 3-bit binary encoded registers and 7-bit thermometer encoded registers. A binary encoding has the advantage of short conversion time, though also has worse monotonicity at higher resolutions. The MSBs are therefore thermometer encoded, which has a better monotonicity and means that less effort is required for error compensation (McDonnell, 2017). A drawback of this type of encoding is a slower transition, though this is less essential for MSBs. The main disadvantage, however, is that a binary to thermometer decoder is needed, which would increase the power consumption (Radulov, 2006; Nazari, 2016). In order to avoid having to use this decoder a control with an up/down signal is implemented. This is well suited for tracking ADCs, due to their limited slew rate. An application example for a tracking ADC is shown in Kanzian (2018). It is used in a controller of a dc-dc converter.

This paper is organised as follows: Sect. 2 describes the ADC's components, Sect. 3 describes the layout of the DAC and comparators, Sect. 4 presents simulation results and finally Sect. 5 provides a brief conclusion.

Table 1. Overview of the quantiser level, the closed switches in a comparator attaining the desired level, the comparators's output and the resulting step size and direction of the DAC.

Comparators	Level	Closed Switches	Output of Comparators				
1	$+3$ VLSB	SW_0_P, SW_3_N	0	0	0	0	1
2	$+1$ VLSB	SW_1_P, SW_2_N	0	0	0	1	1
3	-1 VLSB	SW_2_P, SW_1_N	0	0	1	1	1
4	-3 VLSB	SW_3_P, SW_0_N	0	1	1	1	1
Resulting Step Size			-2	-1	0	$+1$	$+2$

2 Components

The ADC presented in Fig. 1 comprises, apart from the multi-bit quantiser and the 10-bit current-steering DAC which are discussed in the following, a digital counter. The digital counter generates the control signals for the DAC and provides the binary output, the supply voltage for all circuits is 1.2 V.

2.1 Multi-bit quantiser

The multi-bit quantiser consists of 4 comparators. One comparator circuit is given in Fig. 2. The quantiser level is realised by programming comparator offset. Both input ports are connected to source followers and resistor chains. Resistors of $1\,k\Omega$ are used to generate identical voltage offsets in steps of 1 LSB. The eight switches connect the latch stage common source input to the source follower buffer's selected resistor tap. The switching levels are $\pm 1\,V_{\mathrm{LSB}}$ and $\pm 3\,V_{\mathrm{LSB}}$. Table 1 gives a summary of realised comparator levels and the required switch connectivity. Another feature of the comparators is the reduced kickback noise during the settling phase of the latch stage (Huang, 2013b). The transistors with the XOR-signal at the gate therefore disconnect the inputs from the analog outputs. The logic following the latch generates the XOR-signal and a stable output during the reset phase of the comparator.

Table 1 provides an overview of the different comparators' switching levels as well as the resulting step sizes. In order to count up one step, comparator number 1 ($+3\,V_{\mathrm{LSB}}$) must be at zero while all others have to be at 1. For zero step size, which is important for ripple cancellation, the first two comparators have to be at zero, with the other two at 1. The remaining levels count up by 2 steps, then down by 1 and again down by 2 are described in Table 1.

2.2 Current-steering DAC

An overview of the current-steering DAC is shown in Fig. 3. The DAC consists of four parts: the *IDAC control*, a 3-bit binary coded register, a 3-bit unary coded register and a 4-bit unary coded register. The digital counter (Fig. 1) delivers the control signals *cnt_en* and *Up_Down*. The three LSBs $y\langle 0:2\rangle$ of the counter's output are directly connected to the
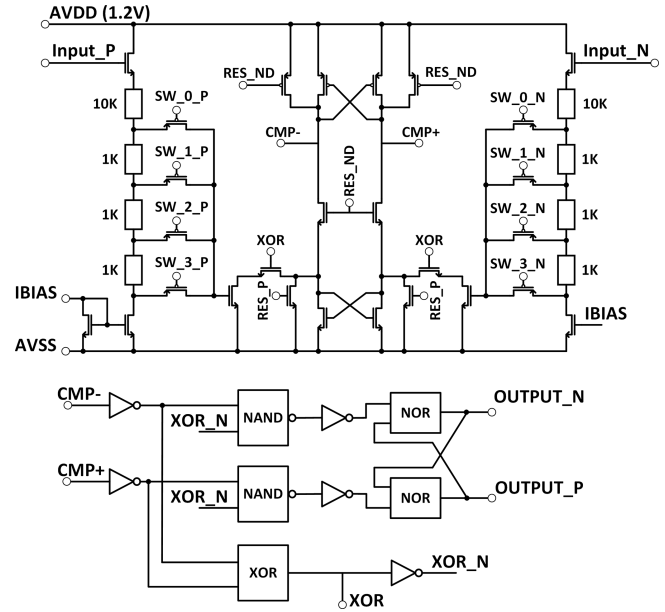

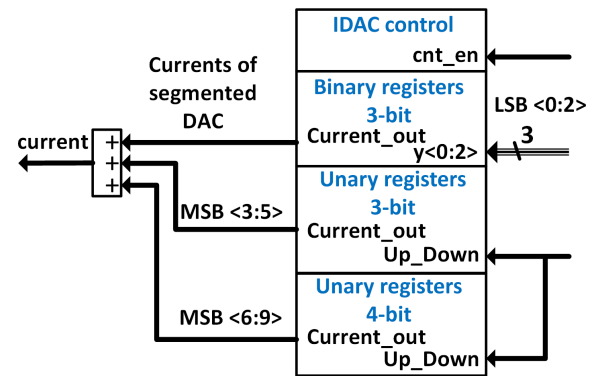**Figure 2.** Transistor level of a comparator and digital output.

Figure 3. Overview of segmented current-steering DAC.

3-bit binary coded register. The IDAC's output current is fed back into the ADC's input, which is also differential.

The 3-bit binary coded register consists of 7 current sources, where each has an output current of $I = 100\,\mathrm{nA}$. This register is directly controlled by the digital counter's 3 LSB. The 3-bit unary coded register consists of 7 current sources with a unit current of $I = 800\,\mathrm{nA}$ while the 4-bit unary coded register has 15 current sources where $I = 6.4\,\mu\mathrm{A}$ per source. The *Up_Down* signal, which is connected to the unary registers, controls the direction of switching. The *cnt_en* signal activates the switching of the unary registers in *IDAC control*. *IDAC control* then operates the current sources in unary coded register sections.

The DAC unit cell's schematic is presented in Fig. 4. The analog part consists of a current source and a switch. The current source is cascaded and biased for low voltage output. The differential switch connects the source either to the
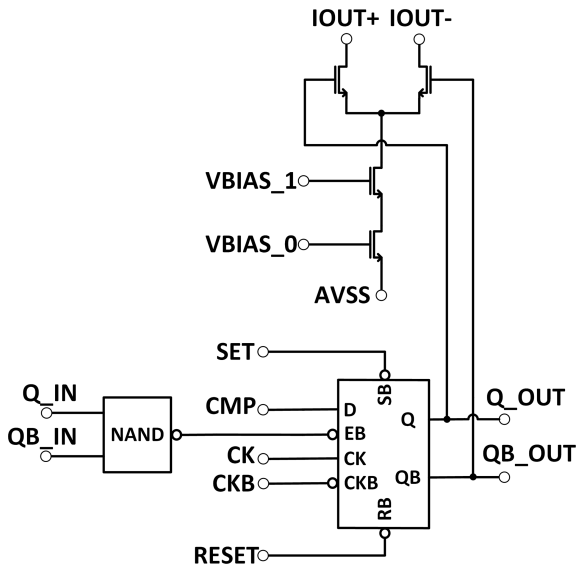
Figure 4. Schematic of a DAC unit cell.

Figure 5. Layout of all comparators.

positive or negative output current rail. The switches are controlled by a flip-flop, enabled by *Q_IN* and *QB_IN* through a NAND gate. In the unary coded register section these inputs are connected between the previous unit cell output and the next unit cell input. This allows for a sequential switching of the DAC cells. In the binary coded register section the flip flop is always enabled. The flip-flop can be set with the *CMP* input signal from the comparator.

3 Layout

The circuit is designed using a 65 nm low-power CMOS technology of TSMC. The four comparators are shown in Fig. 5. All comparators have a dimension of 98 µm × 60 µm. From the bottom to the top the layout depicts the offset resistors at the input, the offset switches that connect the input with the latch stage, the analog part, and finally a digital output and serial connection of registers. In Fig. 6 the layout of the current-steering DAC is depicted. It has a dimension of 130 µm × 169 µm. The registers' current sources are arranged symmetrically so as to achieve a good monotony. All sections of registers have their own biasing network.

4 Simulation

Large signal transient transistor level simulation results are discussed in Figs. 7 to 11. The input signal in Fig. 7 is a sine wave with a frequency of $f_{SIG} = 50$ kHz and an amplitude of $V_{AMP} = 300$ mV. The LSB voltage is $V_{LSB} = 1$ mV and the system frequency is $f_{CLK} = 50$ MHz, which is the $f_{CLK} = 50$ MHz, which is the maximum sample rate. 5 µs the ADC has to compensate the DC input signal as after reset the
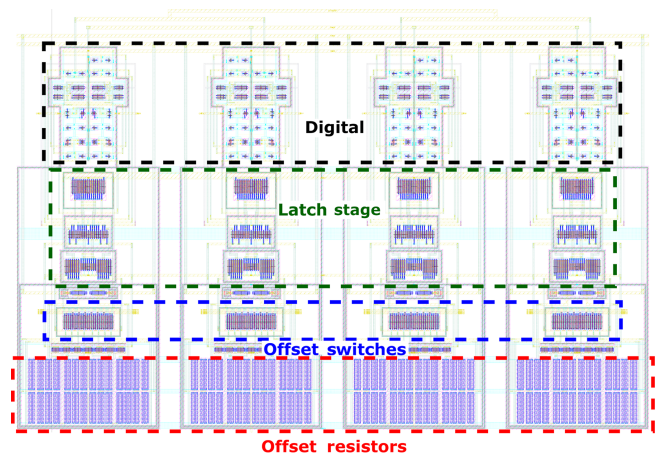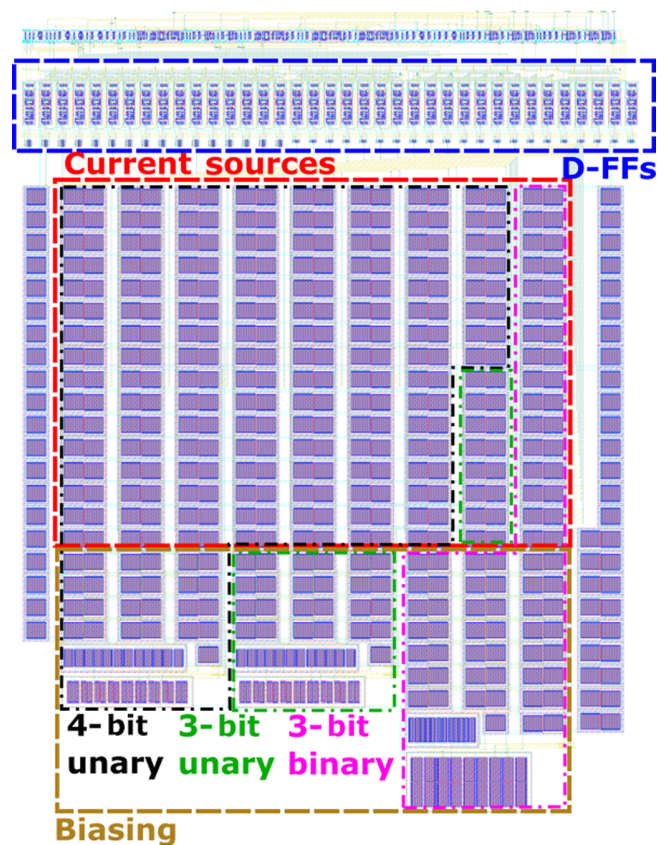

Figure 6. Layout of segmented current-steering DAC.

DAC is set to its minimum value. After start-up the ADC is able to convert the input signal. Figure 8 depicts a closeup of the sine wave peak. Step sizes of 1 and 0 LSBs can be observed. This results in a constant output signal over several clock cycles. Figure 9 illustrates the input signal's the steepest gradient. Step size is here increased to 2 LSB.
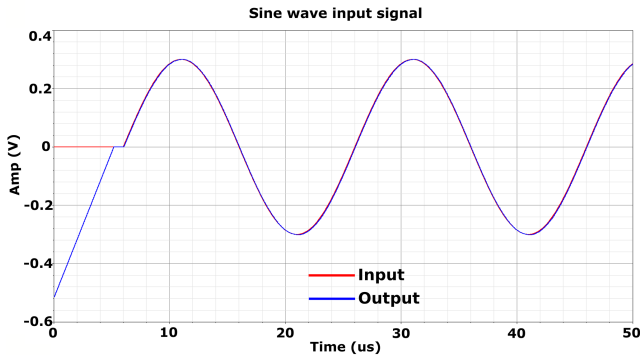
Figure 7. Conversion of sine signal (transistor level simulation).
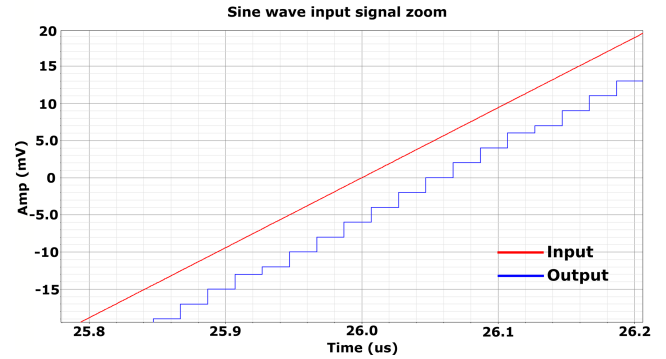

Figure 8. Closeup of the sine signal peak (transistor level simulation).

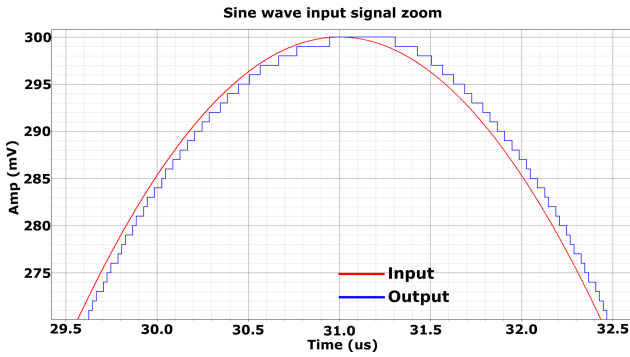**Figure 9.** Closeup of the sine signal's steepest gradient (transistor level simulation).
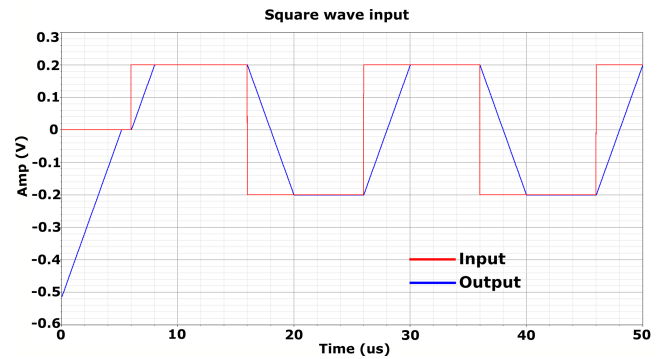

Figure 10. Conversion of rectangle signal (transistor level simulation).

The second input signal (Fig. 10) is a square wave with a frequency of $f_{SIG} = 50$ kHz and an amplitude of $V_{AMP} = 200$ mV. The LSB's voltage and the system frequency is the same as in the previous simulation. After startup and the first rising edge of the input, the ADC enters the fastest mode with a slew rate of 2 mV/20 ns. The major problem of tracking ADCs is the limited slew rate, and in this case it has already improved by a factor of 2. A closeup of the square wave is depicted in Fig. 11. The second major disadvantage of tracking ADCs is the ripple of the output signal. Even with a constant input signal there is a ripple of 1 LSB. The proposed ADC does not have this ripple due to the zero step size when deviation from ideal conversion is less than 1 LSB (step size 0 in Table 1. The simulation result presented in Fig. 11 shows the ripple-free ADC output signal.

Simulations for different input frequencies are captured in Table 2. In addition, the signal amplitude is varied. Due to the higher slope of the input signal, lower frequencies are converted for higher amplitudes. The SNDR was measured and calculated in the time domain with Eq. (1).

$$SNDR = 10 \times \log \left(\frac{\int v_{input}^2}{\int \left(v_{input} - v_{out} \right)^2} \right) \quad (1)$$

To ensure the functionality of the ADC, Monte Carlo simulations of the DAC were undertaken, and are presented in Fig. 12. The DNL for a counting up rail to rail cycle is captured. The clock frequency is reduced to 12.5 MHz. There are gain errors, yet the DNL is less 1 LSB.

The benefit of a tracking ADC with variable step size depends on the application where the ADC is to be used. Therefore an application where a car battery voltage is measured during cranking is here discussed. The tracking ADC principle is compared through a system level simulation using Matlab-Simulink. The input signal is a voltage captured during the start-up of an engine (Fig. 13). The resolution is 16-bit and the time steps are 10 ms. The data is available in the Supplement. In Fig. 13 this signal is converted with an ideal ADC, an ADC according a proposal of Huang (2013a), which is extended to 10-bit, and the proposed 10-bit ADC. A closeup of the voltage peak is depicted in Fig. 14. The ideal ADC has a clock frequency of $f_{ideal} = 2$ kHz, ADC of Huang (2013a) has $f_{Huang} = 25$ kHz and the proposed ADC of $f_{10\,bit} = 25$ kHz. The LSB voltage is $V_{LSB} = 16$ mV.

In Table 3 a summary of conversion, comparator and register clocks as well as accuracy is provided. The ideal ADC and the ADC of Huang (2013a) have a similar number of comparator clocks. The proposed ADC has twice as much

Table 2. Results for varied input frequencies and signal amplitudes ($V_{LSB} = 1$ mV) (system level simulation).

Amp = 0.5 V		Amp = 0.4 V		Amp = 0.3 V		Amp = 0.2 V	
f_{SIG}	SNDR	f_{SIG}	SNDR	f_{SIG}	SNDR	f_{SIG}	SNDR
22.5 kHz	58.7 dB	30.1 kHz	56.5 dB	41.6 kHz	53.8 dB	72.9 kHz	49.5 dB
25.6 kHz	58.1 dB	33.9 kHz	55.9 dB	48.4 kHz	53.0 dB	75.9 kHz	49.3 dB
30.1 kHz	57.3 dB	37.0 kHz	55.4 dB	52.3 kHz	52.6 dB	80.5 kHz	48.6 dB
33.9 kHz	35.7 dB	41.6 kHz	41.0 dB	56.8 kHz	34.5 dB	85.1 kHz	34.8 dB
37.0 kHz	23.5 dB	48.4 kHz	19.7 dB	59.9 kHz	26.5 dB	88.9 kHz	27.7 dB
41.6 kHz	15.5 dB	52.3 kHz	15.2 dB	63.7 kHz	20.7 dB	91.9 kHz	23.9 dB
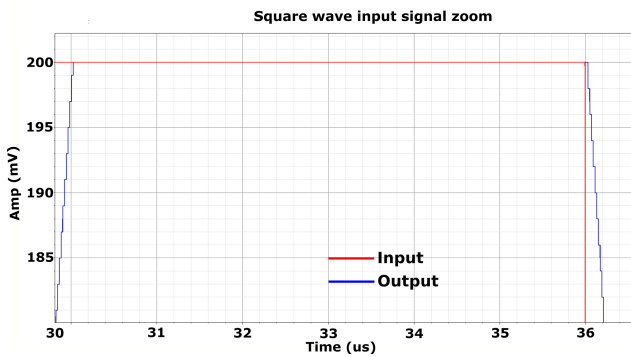
Figure 11. Zoom into rectangle signal (transistor level simulation).
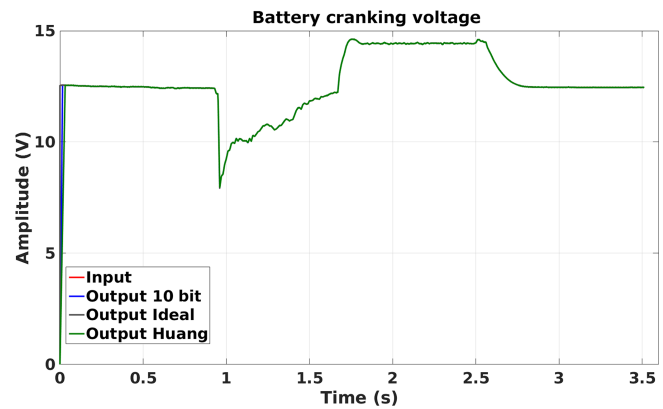
Figure 13. Cranking signal of a battery (system level).
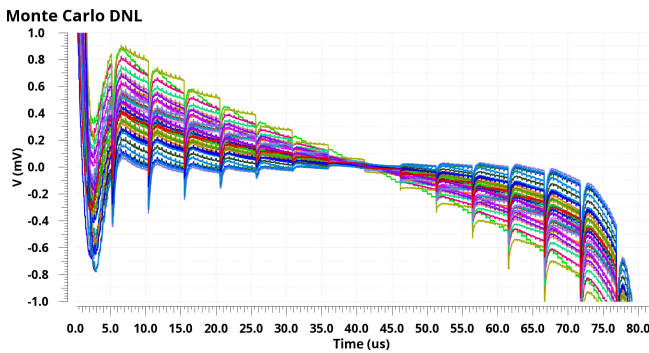
Figure 12. Monte Carlo simulation of the DNL from the DAC ($V_{LSB} = 1$ mV), slope is from -512 to $+512$ mV from 1 to 82 µs.
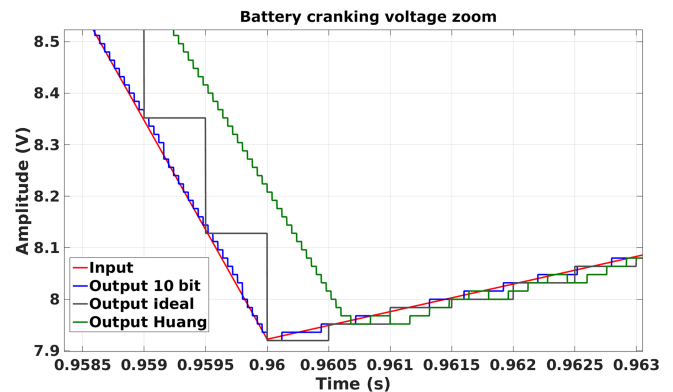
Figure 14. A closeup of the cranking signal of a battery (system level).

comparator clocks due to its constant clock rate and because it has the largest number of comparators. According to the register clocks Huang (2013a) has the most clocks by a large margin, due to the high clock rate, the lack of ripple reduction and the large amount of thermometer coded registers. In comparison, the proposed ADC requires only 7 % of clock cycles and 0.2 % of total register clocks. The ideal ADC has nearly twice as many register clocks as the proposed ADC. The average error is calculated in the signal range from 0.9 to 2.8 s. The ideal ADC yields the best results and the proposed ADC is slightly better than Huang (2013a).

5 Conclusions

This paper presents the design and simulation of a 10-bit tracking ADC with a multi-bit quantiser and a segmented current-steering DAC. The variable step size improves the limited slew rate by a factor of 2 if clock rate is held constant. The step size is controlled by the quantiser depending on the transient of the input signal.

A further advantage is the removal of the output signal ripple. This also reduces the clocking and hence the DAC´s

Table 3. Results of ADCs for converting the test signal and the average error.

	Ideal ADC	Tracking ADC Huang (2013a)	Proposed 10-Bit Tracking ADC	
			Fine	Coarse
Samples	7024	22 723	37 746	
Comparator Clocks per Sampling	10	1	1	
Comparators	$\times 1$	$\times 3$	$\times 4$	
Total Comparator Clocks	70.24×10^3	68.17×10^3	150.98×10^3	
Register Clock Cycles	7024	22 723	1512	243
DAC Registers	10	1024	3	128
Total Register Clocks	70.24×10^3	23.27×10^6	35.64×10^3	
Average Error	4.7 mV	27.4 mV	7 mV	

registers' energy consumption for low frequency input signals.

The tracking ADC presented here runs on a constant clock rate. Even if we consider an SAR used as an ideal ADC with 10 comparator cycles per conversion, our ADC exceeds the total number of comparator clocks due to sample rate and the number of comparators. According to Huang (2013a), a similar step would be a combination of variable clock sizes and variable step size. Compared to the tracking ADC of Huang (2013a) our tracking ADC improves the register's product of the DAC´s thermometer coded register chain and register clocks by nearly 4 decades. This makes a tracking ADC with 10-bit resolution reasonable at all.

Author contributions. SB developed the Matlab models, designed the circuit and draw the IC layout. He prepared the original draft of this article. DK aquired funding by DFG, contributed to the concept, and contributed to review and editing this article.

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