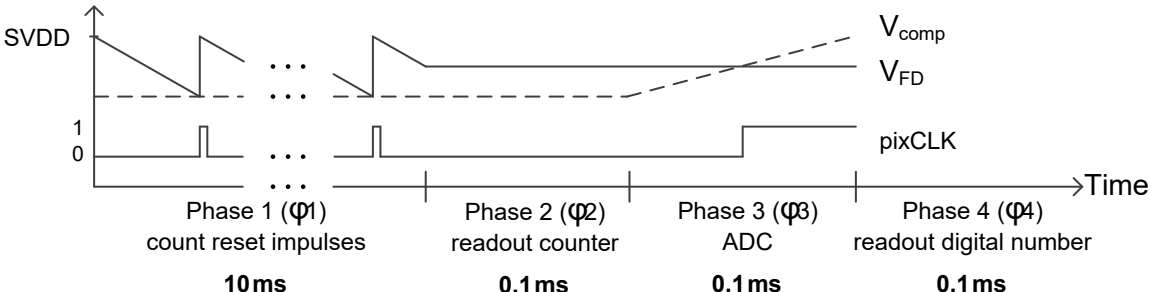
SVDD
1
0
V_{comp}
V_{FD}
pixCLK
Time
Phase 1 (φ1)
count reset impulses
10 ms
Phase 2 (φ2)
readout counter
0.1 ms
Phase 3 (φ3)
ADC
0.1 ms
Phase 4 (φ4)
readout digital number
0.1 ms