Advances in Radio Science (2004) 2: 211–214

Advances in Radio Science

Consideration of parasitic effects on buses during early IC design stages

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Abstract. Complex integrated systems contain more and more on-chip components which exchange data and access memories via buses. To consider parasitic effects on bus structures during the early design phase appropriate models and wiring methods must be available. A RC-Pi model is proposed to model the load of a bus driver cell that also considers capacitive coupling between the signal lines. On the basis of simple estimations it is shown under what conditions the influence of inductance on the bus is negligible. Furthermore a method to consider inductive effects is shown. An early consideration of parasitic effects on global interconnect structures and an assertion which effects have to be considered is mandatory to effectively estimate the behavior of wires. Hence it also helps to avoid wrong assumptions.

1 Introduction

In novel technologies the performance and speed of integrated systems is increasingly dominated by on-chip interconnects. Hierarchical design approaches are used to deal with the complexity of whole Systems-on-Chip. Several system parts are developed independent. This is also necessary for enabling the possibility to reuse system parts or modules from previous developed systems. Bus systems are used for inter block communication. Physically a bus is a bundle of parallel routed wires. The bus structure, i.e. the two dimensional cross section of a bus should be defined while the logical top level design is done. The topology of a bus can be extracted from a floorplanning step. Hence, an early performance estimation of a bus structure is possible. Such an approach requires accurate bus models which consider also capacitive coupling effects. This results from the fact that the capacitance of minimal dimensioned buses is dominated by the coupling capacitances. The validity and reliability of the model has been investigated. An easy method to decide if inductance has to be considered is shown. To accurately simulate inductive effects a partial element equivalent circuit (PEEC) model (Ruehli, 1972) is used. But unlike in Gala et al. (2000) our proposal is to use model order reduction.

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2 RC-load model

A modeling approach is used which decouples the typical nonlinear driver behavior and the linear network of bus wires. The load for the driver caused by the bus is described in a π-model for this purpose. The structure and complexity of the load model is independent from the complexity of the bus structure, i.e. the topology and number of branches. Thus the model permits an integrative algorithm to determine the drivers' output signals. It should be possible to determine the output signals of all branches of the linear network after the drivers' output signals, i.e. the bus input signals are known.

A π-model which describes the load admittance of the driver was presented in Tahedl and Pfleiderer (2003). The model is based on the first three moments of the bus admittance where an estimation of the bus length for all branches and the positions of nodal points is required. The model is an extension to the model presented in O'Brien and Savarino (1989) from single wires to capacitive coupled interconnect buses. Compared to interconnect models where a Thevenin model is used for driver modeling, every model for the driver's nonlinear behavior is possible. Because the Thevenin resistance is often unknown, it is preferred to use timing libraries in early stages of design (Sheehan, 2002), especially when analog simulations with Spice or Spectre are not applicable.

2.1 Model computation

The derivation of the model was presented in Tahedl and Pfleiderer (2003). The used π-model is depicted in Fig. 1. The model is fully described with three parameter matrices C_n, C_f and R_π. To compute these matrices the first three admittance moments of the bus structure are matched to the

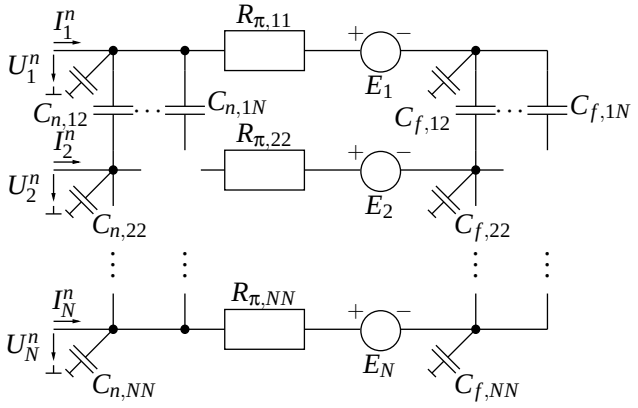


Fig. 1. Capacitive coupled RC-π-model.

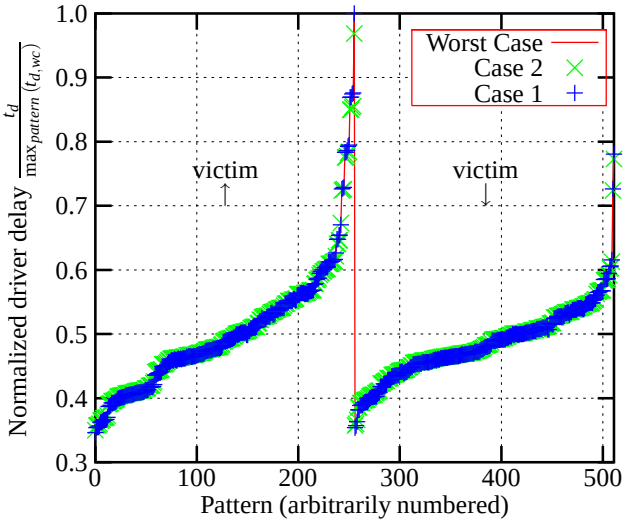


Fig. 2. Dependency of the driver delay on the switching condition in adjacent wires of a bus. The delay is plotted for two cases of wire densities in adjacent metal layers where the technology specific limits for the cases of metal density were chosen. The patterns are sorted by the worst case driver delay for each switching direction on the victim wire.

first three admittance moments of the model. Consequently C_n, C_f and R_π depend on the bus structures first three admittance moments. A bus is modeled by piecewise homogenous segments and lumped elements, e.g. vias between metal layers. The first three admittance moments of a lumped element or a distributed segment depends on the respective capacitance and resistance matrices as well as the first three admittance moments of the load to the element under consideration. Additionally, of course, the moments of a segment depends on the segment length. This dependencies cause a recursive computation of the first three admittance moments of a bus structure. The computation is started at every far-end of the structure. At a nodal point the respective admittance moments of the branches are summed up.

A mathematical simulation approach is suggested instead of the more physical representation depicted in Fig. 1. The physical representation may result in negative capacitances. Additionally some current driven voltage sources are necessary. However, the passivity of the model is proven mathematically.

2.2 Model validity and accuracy

The π-model is valid as long as the bus is sufficiently short. It is assumed that this is true due to the application of repeater insertion algorithms for performance optimization. Anyhow, if reversely scaled buses are used where inductive effects are still negligible or repeater insertion is not applied, an approach for computing a feasible model is presented in Tahedl and Pfleiderer (2003). Therefore a specific saturation length is required where the driver delay saturates. This length strongly depends on the driver's output waveform and can differ for each wire in the bus. The bus is modeled as a bus with open ended wires with saturation length. No closed form expression for the saturation length was derived by now.

Model validity depends on the knowledge of the saturation length and on a statement that inductive effects are negligible. If the model validity can be proven, the accuracy of the load estimation is defined by the accuracy of the structure prediction and by the order of modeling accuracy. For example in a first step the same layer could be assumed for the whole tree without any vias. In some further steps informations on different layers as well as lumped models for vias or bends may be available. The model accuracy depends on the knowledge of the three-dimensional interconnect structure and the model is suitable through all stages of a circuit design process from first performance analysis steps to analysis of final extracted structures and for performance checks before tape-out. As long as the model is valid no differences compared to simulations with long RC-chains are recognizable.

2.3 Bus example

It is possible to estimate the driver delay in early design stages because the influence of wires in the adjacent layers of a bus structure on the driver delay is almost negligible ($< 4\%$). This was shown on the example of a bus in a complex environment. Therefore two cases of wire densities in adjacent layers were assumed. For the two cases the technology specific limits for the metal density were chosen. The dependency of the driver delay from the switching condition in adjacent wires of the bus is depicted in Fig. 2.

3 Inductive effects

Inductive effects have to be considered as a general rule only for long and wide wires which typically can be found in the upper metal layers. Essentially this results from the low resistance and hence the low damping of the wires. A couple of

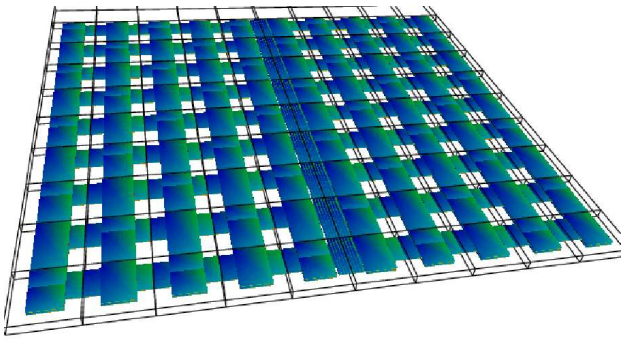


Fig. 3. Three layer power/ground grid with 8 signal lines on the uppermost layer.

formulas to decide when on-chip inductance has to be considered, especially for transmission lines, are well known. In the following we modified a formula (Ismail and Friedman, 2001) to use values of lumped elements.

$$\frac{t_r}{2\sqrt{LC}} < 1 < \frac{2}{R}\sqrt{\frac{L}{C}} \tag{1}$$

The right side of the inequality considers the damping. The left side in principle the relation between the transition time at the driver input and two times the time of flight. The left side of the condition is only valid if the width of the transistor is chosen to match the impedance of the signal line or to be smaller. This is true in most practical cases, because wider transistors are unwanted and lead to overshoots. Therefore inductance can be neglected as long as this inequality is not fulfilled. To get the parameters of the resistance and inductance ports can be defined at the driver side of the signal line. At the receiver input the signal line can be shorted and the impedance can be obtained. As we will show later this is accurate enough to decide if inductance has to be considered for the early design phase.

For an accurate simulation the actual current loop must be considered. During a switching operation of a driver the coupling capacitors to Vdd or Ground along a signal line will be charged. Respectively the opposite capacitors will be discharged. Hence the current loop will be shorter than assumed before. The effective current loop is frequency dependent. Further it depends on switching events, the resulting voltage fluctuations of nearby gates, the decoupling capacitors and even the package. For this reason we decided to simulate a structure similar to the one depicted in Fig. 3. It's based on the forecasts of a 53 nm copper technology from the ITRS roadmap (ITRS, 2001). We considered a three layer power and ground grid with a bus on the uppermost layer like in Gala et al. (2000). But our approach is to use model order reduction which is considered unsuitable in Gala et al. (2000) for the fully-dense matrix of their model.

3.1 Inductance extraction

In order to get a PEEC model we used a precorrected-fast-Fourier-transform (FFT) approach (Hu et al., 2003) to simulate the on-chip inductance. The merits of this method are that the dense inductance matrix is not calculated explicitly, but a very accurate and fast computation of the product of the inductance matrix with a given vector is provided. Further this method doesn't suffer the problems of other sparsification techniques which are also described in detail in Hu et al. (2003). It considers all mutual partial inductances and is based on accurate partial inductance formulas. For the partial self-inductance we use the formula from Ruehli (1972).

3.2 Model order reduction and simulation

Using a modified nodal analysis (MNA) formulation the linear part of the model is represented as:

$$\begin{aligned} \mathbf{C}\dot{x}_n &= -\mathbf{G}x_n + \mathbf{B}u_N \\ i_N &= \mathbf{B}^{\mathbf{T}}x_n. \end{aligned}$$

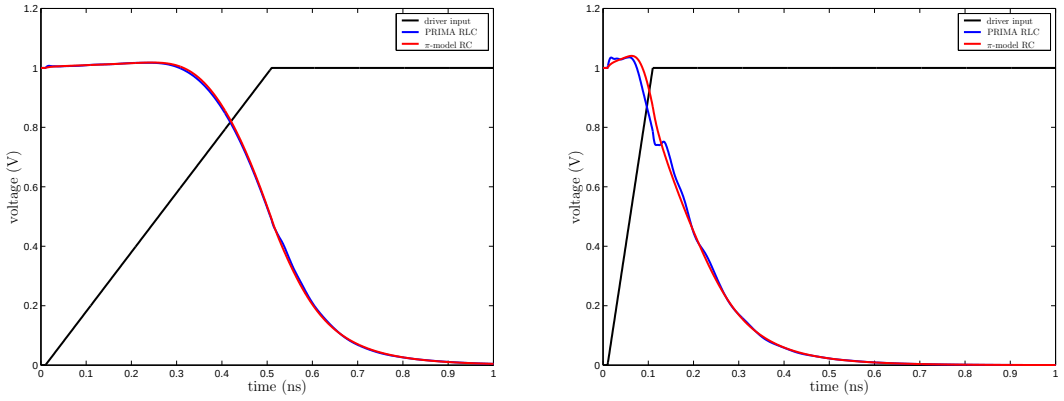
Essentially $\mathbf{C}$ and $\mathbf{G}$ are the susceptance and conductance matrices. The vector x_n consists of the MNA variables (voltages and currents) and the vectors u_n and i_N are the corresponding port voltages and currents. The PRIMA (Odabasioglu et al., 1998) algorithm reduces the MNA matrices to

$$\begin{aligned} &\tilde{\mathbf{C}} = \mathbf{X}^{\mathbf{T}}\mathbf{C}\mathbf{X} \qquad \tilde{\mathbf{G}} = \mathbf{X}^{\mathbf{T}}\mathbf{G}\mathbf{X} \\ &\tilde{\mathbf{B}} = \mathbf{X}^{\mathbf{T}}\mathbf{B}. \end{aligned} \tag{2}$$

The matrix $\mathbf{X}$ spans a block Krylov subspace and can be calculated for example with the block Arnoldi algorithm as illustrated in Alg. 1. Therefore to obtain a reduced model the explicit inductance matrix which is a submatrix of $\mathbf{C}$ is not necessary. Only the calculation of the product of the matrix $\mathbf{C}$ with some vectors is required in Eq. (2) and Alg. 1. To simulate Eq. (2) together with the nonlinear elements the MNA variables of the reduced system are interpreted as voltages. The symmetric part of the matrices $\tilde{\mathbf{C}}$ and $\tilde{\mathbf{G}}$ will be interpreted as resistors and capacitors in a SPICE netlist. The non-symmetric part will be realized with capacitors and resistors in series with a voltage controlled voltage source to ground. The connection between the ports and the "internal" network will be accomplished by the introduction of voltage controlled current sources at the ports and the internal nodes. There are different realizations imaginable, a similar realization can be found in Heres (2003).

One drawback of the approach is that the expansions point is set to $s_0 = 0$. For a different expansion point s_0 it is possible to replace the $\mathbf{G}^{-1}$ in Alg. 1 by $(\mathbf{G} + s_0\mathbf{C})^{-1}$, but this is numerically expensive. The expansion around zero leads to slightly bigger models than the expansion at higher frequencies to obtain a comparable accuracy.

Algorithm 1 Block Arnoldi with double orthogonalization.



(a) t_r=500ps (b) t_r=100ps

Fig. 4. Simulation results of the driver output for different rise times.

$qn = ceil\,(q/N)$
$[\mathbf{X_0}, \mathbf{R}] = qr\,(\mathbf{G^{-1}B})$
for k=1 to qn
  $\mathbf{X_k} = \mathbf{G^{-1}C X_{k-1}}$
  for np=1 to 2
    for i=1 to k
      $\mathbf{X_k} = \mathbf{X_k} - \mathbf{X_i}\left(\mathbf{X_{i-1}^T X_k}\right)$
    end
  end
  $[\mathbf{X_k}, \mathbf{R}] = qr\,(\mathbf{X_k})$
end
$\widetilde{\mathbf{X}} = \left[\mathbf{X_0}, ..., \mathbf{X_{qn-1}}\right]$
$\mathbf{X} = \left[\widetilde{X}_0, ..., \widetilde{X}_q\right]$

3.3 Simulation results

We investigated a bus with a length of 3.5 mm and the surrounding powergrid. For this topology the right side of Eq. (1) is considerably greater than 1. The left side is approximately 1 for a transition time of 100 ps. So for transition times larger than 100ps inductive effects should be negligible. The simulation results in Fig. 4 confirm this. It is also apparent that with a transition time of 100 ps already the first inductive effects arise. Hence our proposed π-load model can be deployed as long as Eq. (1) is not valid. In the other case model order reduction can be used to get a model which considers the inductive effects.

4 Conclusion

To analyze the output of a driver an accurate RC load model that considers capacitive coupling has been used. As long as inductive effects can be neglected and the bus is sufficiently short the model is valid. We have demonstrated that it is possible to use simple conditions to decide whether inductance has to be considered or not. If inductance is not negligible a reduced PEEC model which can be realized as a simple SPICE netlist can be used instead of the RC model.

Acknowledgement. This work was partially supported by Atmel Germany GmbH and the German Bundesministerium für Bildung und Forschung with the indicator 01M3060C. The authors are responsible for the content.

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