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Improving the positive feedback adiabatic logic familiy

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Abstract. Positive Feedback Adiabatic Logic (PFAL) shows the lowest energy dissipation among adiabatic logic families based on cross-coupled transistors, due to the reduction of both adiabatic and non-adiabatic losses. The dissipation primarily depends on the resistance of the charging path, which consists of a single p-channel MOSFET during the recovery phase. In this paper, a new logic family called Improved PFAL (IPFAL) is proposed, where all n- and p-channel devices are swapped so that the charge can be recovered through an n-channel MOSFET. This allows to decrease the resistance of the charging path up to a factor of 2, and it enables a significant reduction of the energy dissipation. Simulations based on a 0.13μm CMOS process confirm the improvements in terms of power consumption over a large frequency range. However, the same simple design rule, which enables in PFAL an additional reduction of the dissipation by optimal transistor sizing, does not apply to IPFAL. Therefore, the influence of several sources of dissipation for a generic IPFAL gate is illustrated and discussed, in order to lower the power consumption and achieve better performance.

1 Introduction

The technology progress together with the system on a chip (SoC) approach leads to an increasing number of transistors on a chip. As a result, even in modern technologies with reduced supply voltage the dynamic power dissipation of integrated circuits continues to increase. As long as the system is mains-operated the cooling of the chip and the generation of a constant DC voltage represent the main challenges. In battery-operated or mobile systems, the dynamic power increase leads to reduced operating time because the capacity of batteries does not increase in the same way. In future, also the leakage losses will become a major concern especially for mobile systems.

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Low power digital signal processors work at frequencies up to 200 MHz. In this frequency range, adiabatic circuits allow a significant reduction of the energy dissipation breaking the fundamental limit of static CMOS ($\frac{1}{2}CV_{DD}^2$). The adiabatic logic families using cross-coupled transistors show very low energy consumption and robust operation. One of the first logic families proposed was the Efficient Charge Recovery Logic (ECRL) (Moon et al., 1996). Using not only cross-coupled p-channel transistors but a complete latch consisting of cross-coupled inverters leads to the logic family 2N-2N2P (Kramer et al., 1995) and the Positive Feedback Adiabatic Logic (PFAL) (Vetuli et al., 1996; Blotti et al., 2000). Among these three implementations, PFAL exhibits the lowest energy dissipation. A comparison of these logic families can be found in Amirante et al. (2001).

In PFAL, the main dissipation of energy occurs in the p-channel transistors used in the latch. To enhance the conductivity of the p-channel devices their width can be increased. However, there is an upper bound for the device width because the cross-coupled transistors also act as a load capacitance (Fischer et al., 2003). In this paper, we propose an approach where the charging resistance is lowered not by optimal device sizing but replacing p-channel transistors with n-channel transistors. As a consequence, all transistors are swapped and the maximum value of the supply voltage V_{DD} is chosen as reference potential instead of ground. This paper describes the properties of this new logic family which we call Improved PFAL (IPFAL). The energy dissipation is reduced over the whole frequency range compared to PFAL. It is shown that circuit optimization in dependence of the fanout is different from the original PFAL. As the charging path is less dissipative other mechanisms exhibit significant contributions to the total energy loss.

2 Adiabatic logic families

Static CMOS circuits use pull-up and pull-down networks connected to the DC voltages V_{DD} and ground. As a consequence, the load capacitance C_L is charged or discharged

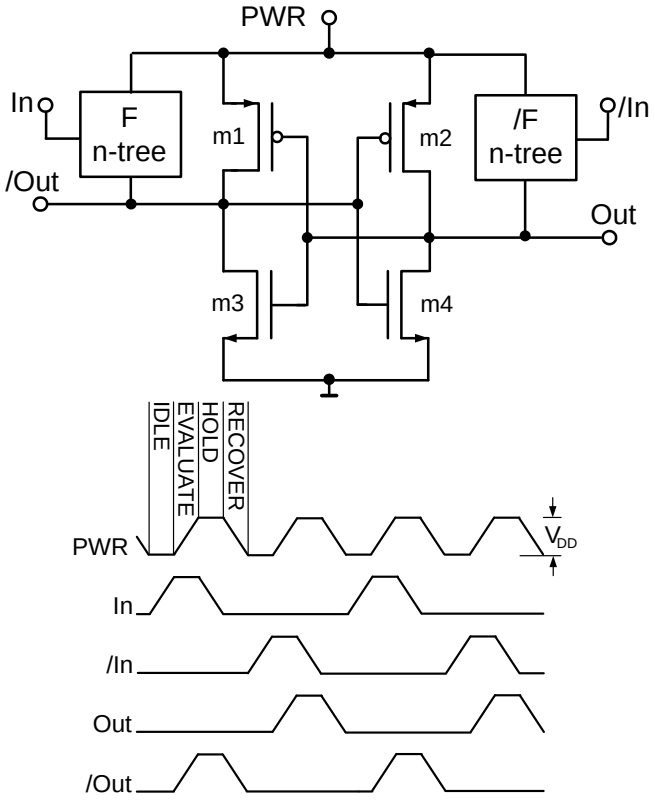

Fig. 1. Top: Timing diagram of a PFAL inverter with the oscillating power supply PWR, the dual rail encoded input signal (In and /In) as well as the dual rail encoded output signal (Out and /Out). Bottom: General schematic of the Positive Feedback Adiabatic Logic (PFAL).

with a voltage step, leading to an energy consumption of $\frac{1}{2}C_L V_{DD}^2$. In adiabatic circuits instead, the switching operation is optimized with respect to energy dissipation. An oscillating power supply is used, as shown in Fig. 1. The loading and unloading of the load capacitances is performed with voltage ramps which result in a minimized voltage drop over the switching transistors. The voltage ramp is provided by the oscillating power supply PWR. The evaluate (charge) and the recover (discharge) phase should take the same time T_{charge} as the hold phase in which the valid output signals are evaluated by the succeeding stages. An idle phase of the same duration time is inserted, in order to achieve a symmetric trapezoidal waveform, which is advantageous for signal generation. A system is powered by four power supply signals with a phase shift of 90°. The energy dissipation per switching operation of a gate supplied by a trapezoidal waveform with $T_{\text{charge}} \gg R_{\text{charge}} C_L$ can be determined according to the equation

$$E_{adiab} = \frac{R_{\text{charge}} C_L}{T_{\text{charge}}} C_L V_{DD}^2 \tag{1}$$

where R_{charge} is the resistance of the charging path.

Moreover, energy can only be recovered as long as the transistor in the charging path is conducting. When the supply voltage goes below the threshold voltage V_{th}, the transistor is turned off and a residual charge remains on the output node. This charge is discharged non-adiabatically at the beginning of the next cycle when the new logic value is evaluated. This term does not depend on the operating frequency and represents the main part of the non-adiabatic dynamic losses (Fig. 2, top). The energy dissipated in such a non-adiabatic discharge process is equal to

$$E_{Vth} = \frac{1}{2} C_L V_{th}^2 \tag{2}$$

Other parts of the non-adiabatic dynamic losses derives from coupling effects whose contributions to the energy dissipation depend on the topology.

Among the MOSFET-only logic families, PFAL shows the best properties in the high frequency range (Amirante et al., 2001, 2002). Figure 1 shows the general schematic of a PFAL gate. The input n-channel transistors evaluating the logic function F are connected between the oscillating power supply and the output nodes. The cross-coupled inverters (latch) drive the dual-rail encoded output signals Out and /Out. The timing of the signals is explained with an inverter as example (timing diagram of Fig. 1). The power supply PWR has a phase shift of 90° compared to the dual-rail encoded input signals In and /In. When the input signal In is Low (/In is High) the output signal Out follows the oscillating power supply PWR whereas /Out stays at ground and vice versa.

The figure of merit for the evaluation of adiabatic circuits is the energy dissipation per cycle. In Fig. 2 (bottom), the energy dissipation per cycle of a 8bit PFAL Ripple-Carry Adder (RCA) is compared to the corresponding implementation in static CMOS. At high operating frequency, the energy consumption of static CMOS is frequency independent whereas in adiabatic circuits the dissipation is inversely proportional to the charging time according to Eq. (1) and therefore directly proportional to the operating frequency. In the low frequency range, both circuits are affected by leakage currents. In PFAL, the off-resistance of the n-channel transistors connected to V_{SS} (m3 and m4) determines the leakage losses. This part of the energy dissipation characteristic is inversely proportional to the frequency. Up to a operating frequency of 100 MHz, the 8bit PFAL RCA exhibits a large energy saving factor compared to the static CMOS implementation. At $f = 20\,\text{MHz}$, a energy saving factor up to 7 can be achieved, as was confirmed by measurements in a $0.13\,\mu$m CMOS technology (Amirante et al., 2003).

3 Improving PFAL

The energy dissipation of PFAL is simulated in a $0.13\,\mu$m CMOS technology with BSIM 3V3.2 parameters by means of the inverter chain shown in Fig. 3. Only the energy dissipation of the third stage was taken into account. The first two stages provide a realistic input signal, whereas the last two represent the load capacitance.

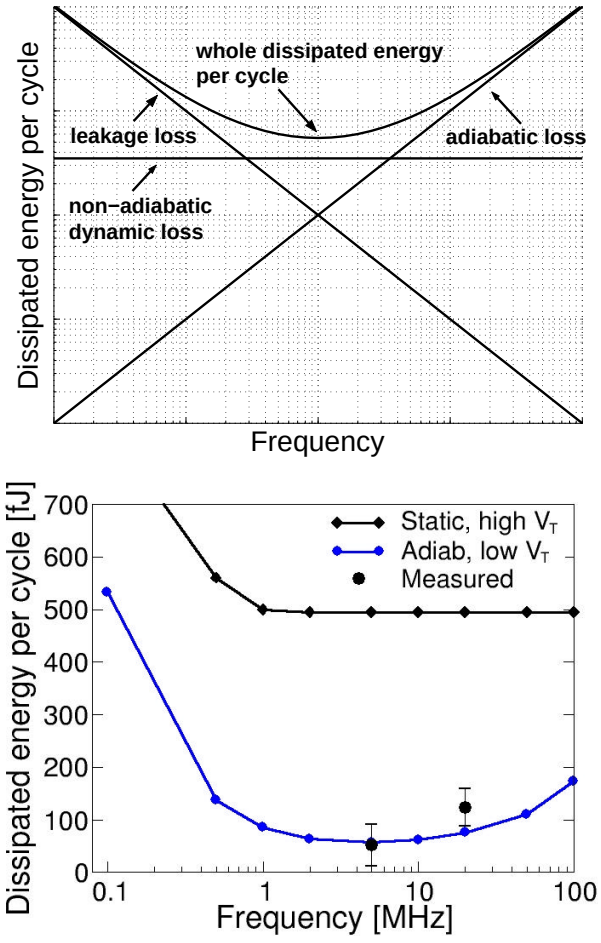

Fig. 2. Top: Different sources of the energy dissipation in adiabatic logic gates. Bottom: Comparison of a static CMOS implementation of an 8-bit Ripple Carry Adder (RCA) with high V_T transistors to an adiabatic implementation in PFAL with low V_T transistors, both simulated, and measurement result for the adiabatic implementation. The 8-bit PFAL RCA dissipates less energy up to an operating frequency of about 100 MHz (Amirante et al., 2003).

The resistance of the charging path R_{charge} is mainly determined by the p-channel transistor. Since the voltage drop over the transistor is very low the MOSFET works in the linear region. For this operating point the charging path resistance can be approximated by the long channel approximation of the p-channel transistor on-resistance $R_{p,on}$:

$$R_{\text{charge}} \approx R_{p,on} \approx \frac{1}{\mu_p C_{OX} \frac{W_p}{L} V_{GST,avg}} \tag{3}$$

where μ_p is the hole mobility, C_{OX} the oxide capacitance per unit area, W_P the transistor width, L the channel length and $V_{GST,avg}$ the gate overdrive voltage averaged over the time.

The on-resistance of the p-channel transistors $R_{p,on}$ can be improved choosing a larger width during the design. Using this approach, the charging path resistance can be decreased, however at the cost of increased internal capacitances. Therefore, to increase the p-channel transistor width is a useful approach only if the internal capacitances remain lower than the external load capacitance. A detailed description of the device sizing rules for PFAL gates can be found in (Fischer et al., 2003). Figure 3 shows the energy loss of an inverter with a fanout of 10 in dependence of the p-channel transistor width. For such a high external load capacitance, the energy dissipation is lowered by a factor of 1.5 with double transistor width. At $f = 500\,\text{MHz}$, the dissipation amounts to $0.88\,fJ$ with a width of $0.16\,\mu$m compared to $0.60\,fJ$ using a width of $0.32\,\mu$m.

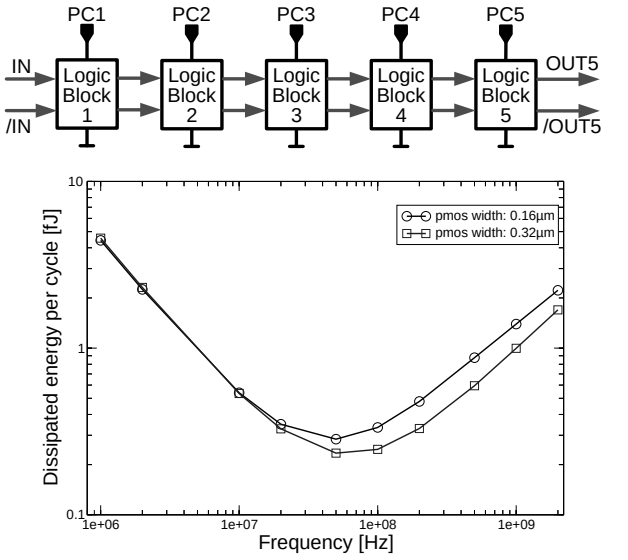

Fig. 3. Top: Energy dissipation is investigated by means of an inverter chain driven by the oscillating power supplies PC1 to PC5. The dissipation of the third stage is determined. Bottom: The energy dissipation of a PFAL inverter strongly depends on the sizing of the p-channel transistors. The n-channel transistor width is kept minimum sized. The fanout value amounts to 10.

In digital circuits with a low fanout value, larger transistor widths give rise to an increase of the energy dissipation and therefore no improvement is possible by width scaling. As an alternative optimization approach, we propose to replace the p-channel transistors with n-channel devices and vice versa. As reference potential, now the maximum value of the supply voltage V_{DD} is chosen instead of ground (see Fig. 4). This new logic family is called Improved PFAL (IPFAL). The waveform of the oscillating power supply does not change, but now the highest potential corresponds to the idle phase because it is equal to the reference potential. In IPFAL, ramping down the supply voltage means charging the capacitances (evaluate phase) whereas the discharging occurs while the supply voltage is ramping up (recover phase). The hold phase takes place when the voltage reaches its lowest value, that is when the difference to V_{DD} is maximum. Compared to PFAL, this means a swap of the single phases with respect to the supply voltage value. In terms of logic values and in analogy to PFAL, a charged capacitance represents a logical 1 whereas an unloaded capacitance stands for a logical 0. Therefore, the lowest potential represents a logical 1 whereas the highest stands for a logical 0.

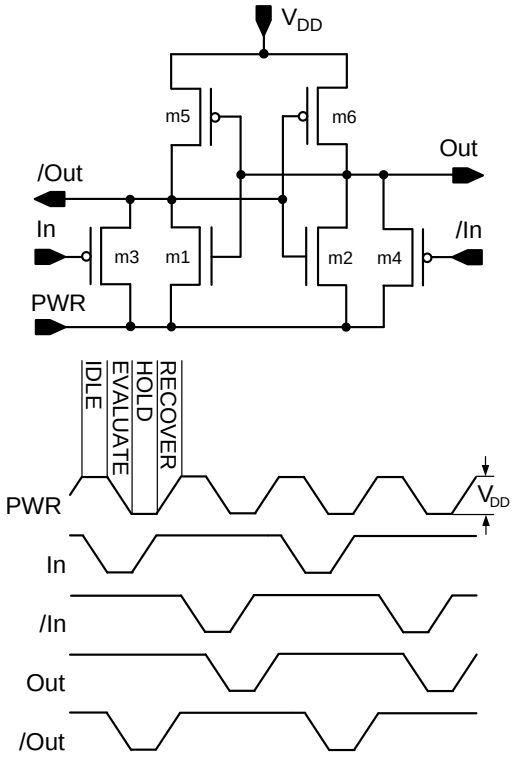

Fig. 4. Schematic (top) and timing diagram (bottom) of an Improved PFAL (IPFAL) inverter.

4 Comparison of the energy dissipation

Figure 5 shows the energy dissipation of PFAL and IPFAL with a fanout of 1 using minimum sized transistors. As expected, the higher conductivity of the n-channel transistors leads to a decrease of the adiabatic energy loss at high frequencies due to the reduced charging path resistance. At $f = 500\,\mathrm{MHz}$, the energy dissipation of PFAL amounts to $0.22\,fJ$ compared to $0.15\,fJ$ in IPFAL. In spite of the expected gain factor of 2 due to the the mobility difference between holes and electrons, only a gain factor of 1.5 is observed showing that additional loss mechanisms play a role in IPFAL. The lower energy dissipation in IPFAL at low frequencies is due to the dependence of the leakage current on the transistors connected to the reference potential (PFAL Fig. 1: m3 and m4; IPFAL Fig. 4: m5 and m6). For equally sized devices, the leakage current is lower in p-channel than in n-channel MOSFETs. Therefore, IPFAL shows a lower energy dissipation than PFAL also in the frequency range dominated by the leakage current. At $f = 1\,\mathrm{MHz}$, the energy dissipation of PFAL amounts to $0.46\,fJ$ compared to $0.25\,fJ$ in IPFAL.

For other fanout values, PFAL offers a simple sizing rule, as only the width of the p-channel transistor in the charging path has to be adapted to the increased external load capacitances. The n-channel transistors m3 and m4 are kept minimum sized, because they provide a good clamp of the output nodes to ground even for this transistor width. In IPFAL, when width of the n-channel transistor in the charging path is increased, the p-channel transistors m5 and m6 must also provide a good clamp of the output nodes to the reference voltage V_{DD}, which is not achieved keeping the p-channel transistor width to the minimum size. Therefore, when the width of the n-channel devices is enlarged, also the p-channel transistor width have to be increased. In Fig. 5 (bottom), three sizing examples for IPFAL with a fanout value of 10 are compared: minimum sized transistors ($W_p = W_n = W_{\mathrm{minimum}}$), $W_p = 2 \cdot W_n = 2 \cdot W_{\mathrm{minimum}}$ and $W_p = 2 \cdot W_n = 4 \cdot W_{\mathrm{minimum}}$, where W_p is the width of the transistors m5 and m6. Over the whole frequency range IPFAL exhibits lower energy dissipation than PFAL. In IPFAL, the lowest energy dissipation in the high frequency range is achieved with minimum sized transistors. Increasing the n-channel transistor width leads to a decreased charging path resistance. However, due to the larger p-channel transistors the internal capacitances are increased, thus compensating the energy decrease. Hence, it results an increase of the total energy dissipation for larger transistor widths. At low operating frequencies, the circuit with the largest transistor widths exhibit the lowest energy dissipation. For these values of the transistor width, the threshold voltages take their highest values (narrow width effect) and the leakage current is minimized.

As a result, the simple sizing rule used to dimension PFAL gates can not be adopted for IPFAL. Contrary to optimizing just the n-channel transistors in the charging path, a load-dependent gate optimization of the n- and p-channel transistors must be performed due to the several concurrent loss mechanisms and to the $V_{th}(L)$ characteristics of a technology.

5 Conclusions

In modern technologies, adiabatic logic families using only MOSFETs show the lowest energy dissipation. Among these logic families, the Positive Feedback Adiabatic Logic (PFAL) gives the largest energy saving factor with respect to static CMOS circuits. Performance improvements of adiabatic logic gates can be achieved decreasing the charging path resistance. In PFAL, the charging path resistance is determined by p-channel transistors. Widening these transistors leads to a resistance decrease but also to a load capacitance increase due to the cross-coupling of the transistors in the latch. Therefore, an upper bound for the p-channel device width is determined by the ratio of internal and external capacitances.

An Improved PFAL (IPFAL) is proposed, where the p-channel transistors are replaced by n-channel devices and vice versa. The maximum value of the supply voltage V_{DD} is the reference potential. Therefore, the highest potential represents a logical 0 whereas the logical 1 corresponds to the lowest potential. The energy dissipation of IPFAL is reduced by a factor of 1.5 with respect to PFAL over the whole frequency range. In the high frequency range, this additional energy savings was achieved reducing the charging

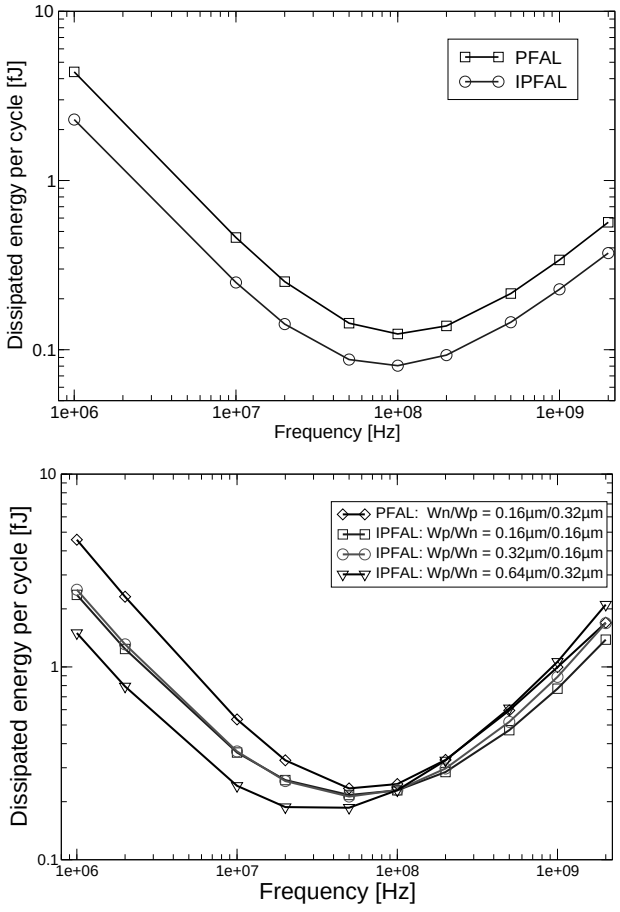

Fig. 5. Top: Comparison of the energy dissipated in PFAL and IPFAL inverter using minimum sized transistors ($W_n/W_p = 1$) and a fanout of 1. Energy dissipation is reduced by a factor of 1.5 in IPFAL because the charging device is a n-channel transistor whose conductivity is higher than that of a p-channel device with the same dimensions. Bottom: Energy dependence on the transistor sizing for PFAL and IPFAL inverters with a fanout value of 10. In PFAL, only the width W_p of the p-channel transistors in the charging path must be adapted to the increased external load. In IPFAL, widening only the n-channel transistors in the charging path is not useful due to concurrent contributions to the energy loss. Therefore, also the p-channel transistor width is increased.

path resistance by the use of n-channel transistors. At low operating frequencies, the energy dissipation is dominated by the leakage current through the p-channel transistors m5 and m6 (Fig. 4). Since p-channel transistors exhibit lower leakage currents than n-channel devices, IPFAL enables a decrease of the dissipation also at low operating frequencies.

For higher fanout values, PFAL gates can be adapted increasing the p-channel transistor width. Unfortunately, this simple sizing rule can not be exploited for IPFAL. Here a load-dependent gate optimization considering both n- and p-channel devices has to be performed. At low fanout values typical for digital systems, Improved PFAL exhibits the lowest energy dissipation among all adiabatic logic families, especially in the high frequency range.

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