Advances in Radio Science (2004) 2: 233–236

Advances in Radio Science

Circuit architecture derivation starting from a formal requirements specification considering a DDS as example

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Abstract. Based on a formal specification of a direct digital synthesis (DDS) and assuming the availability of a set of possible circuit architectures we derive a customised system configuration. We calculate the design parameters that can be used for the specification to synthesise the circuit components.

We show how the derived parameters and the selected IC technology influence the complexity of the circuit implementation.

1 Introduction

There exists a lot of challenging reasons for the present endeavours made in modernization and improvement of the design flow in the context of integrated circuit design.

One of the key points is the demand to reduce the time-to-market of the circuit design. Other important reasons are lowering costs and improving reliability by attending the fact that the circuit complexity is continuously increasing. Generally, it can be stated that there exists a design gap of rising importance that must be bridged.

Related to this background, different concepts have been introduced during the last years to improve the situation. Common to all these concepts is the fact that some effort has been spent in reinforcing computer aided design (CAD) to replace human design activities. This is possible by fulfilling the basic pre-condition of a preferable complete formalization of the different steps of the design process.

In general the design flow can be roughly divided into the following successive steps:
- definition of the specification,
- choice of the system architecture,
- block specification,
- choice of the circuit architecture,
- circuit design,
- testing.

At present CAD-concepts are in practical use on a remarkable high level with respect to the last three or four design steps. This is due to the existence of sufficient accurate behavioural models for analogue and digital circuits. There are corresponding algorithms that allow CAD activities, especially in circuit design.

In principle, adjacent design-strategies, like “Design reuse” and “IP Design”, can be ranged in here because of their being regarded to circuit design (Seepold, 2002).

With respect to the first two or three design steps the level of CAD-activities is rather unsatisfying. At present, research activities are aimed at a formalization of the specification to get a suitable platform for a systematic and CAD based selection of system architectures and performing the subsequent design steps.

The paper is focused on the first two design steps and the transition between them. Based on an example, options for a formal definition of the specification and a systematic choice of the system architecture are presented.

2 System design flow

We consider the system design flow as it is shown in Fig. 1.

Starting with an abstract system requirements specification a selection is performed from a set of system architectures. Also design parameters are calculated, which can be used in the next design steps, e.g. as part of the specification for a register transfer level synthesis.

Afterwards a step follows, which we will not describe in detail in this article. We estimate statements about the possibility and complexity of an implementation in a selected IC technology. This leads to a proposal for a technology selection if there is more than one opportunity.

In the following we show the transition of a system specification into parameters for the register transfer level synthesis by using the direct digital frequency synthesis (DDS) as an example.

Such a component can be used as oscillator or modulator in a mobile radio system.

In this context the reduction of the system size and of the clock frequencies is of extraordinary importance, because this results in a reduction of power consumption.

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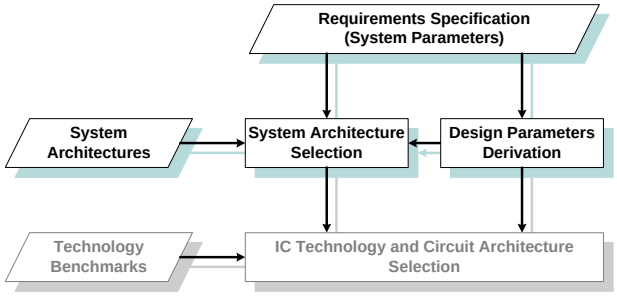

Fig. 1. IP based system design flow.

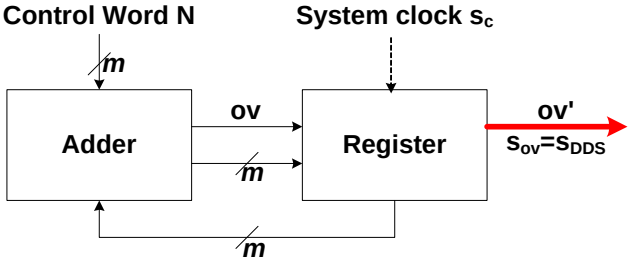

Fig. 2. Phase accumulator of a pulse output DDS.

The estimations of various DDS architectures have been published in Richter (1999). There Richter derived the mathematical models and the correlation of system configuration and system parameters. These models have been verified by simulations and measurements of prototypes in different technologies.

Related to the set of tasks presented above these relations were transformed to emphasise the view of the system synthesis.

The aim is to derive the minimum necessary hardware costs and to choose which system configuration has to be used, in order to fulfil the system specification.

An example of these costs is the word width of implemented mathematical operations. The reduction of the signal processing complexity is a further example.

3 DDS principle and system architecture

A DDS is a digital procedure/algorithm to generate a signal, whose phase and frequency are directly tuneable.

A centre frequency f_{DDS} is derived from a reference frequency f_c and a controllable factor R. The relationship is shown in Eq. (1).

$$f_{DDS} = R \cdot f_c \text{ with } 0 < R < 1. \quad (1)$$

A special realisation of such a system is the pulses output DDS. Its base component is a phase accumulator. A special implementation is shown in Fig. 2.

The factor R is formed by the relationship of a control word N and the number of states, which an accumulator with word width m can accept (Eq. 2).

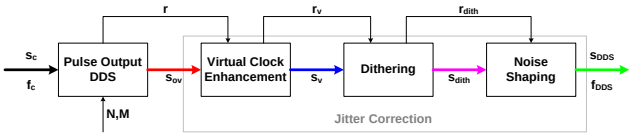

Fig. 3. DDS system architecture.

The control word N is constantly added to the accumulator value. The limited word width results in a sequence of overflow pulses. The pulse period T_{DDS} is related to the output frequency with

$$f_{DDS} = \frac{1}{T_{DDS}} = \frac{N}{M} \cdot f_c \text{ with } N, M \in \boldsymbol{N} \text{ and } N < M \quad (2)$$

The usage of a rational divisor R leads to a jitter of the pulse sequence between two possible period lengths of the timing pattern of f_c. Hence the pulses are either generated at the correct time or they are delayed. The amount of this error can be computed from the remainder value of the accumulator after an overflow.

The spectrum of the output signal contains a large number of discrete spurs (Fig. 4a, red spectrum).

In order to improve the spectral characteristics the following procedures for jitter correction can be implemented.

(1) The virtual clock enhancement function reduces the jitter of the pulses. This results in a reduction of the power of the discrete spurious signals. It computes a more exact pulse output time due to the closer timing pattern of the virtual clock frequency $f_{c,v}$

$$f_{c,v} = B \cdot f_c \text{ with } B = 2^v. \quad (3)$$

The improved spectrum is shown in blue in Fig. 4a.

(2) Dithering and noise shaping eliminate all discrete spurs, but transfer the power of the jitter signal into a continuous noise signal with spectral shaping. Resulting spectrum improvements are illustrated in Figs. 4b and 4c, respectively.

In Fig. 3 the architecture of a DDS is shown. The components of the jitter correction are optional and can be selected according to the architecture.

4 System specification: parameter and conditions

An implementation of a frequency synthesis system is characterised by a set of parameters, like:
- the output frequency f_{DDS}, which can be specified as list of discrete frequencies or frequency ranges,
- the frequency resolution Δf_{DDS} or the minimal increment of f_{DDS} or R,
- the switching speed or the latency time for the adaption to a new value of f_{DDS} after a change of R,
- the phase behaviour during frequency change,
- the spurious free dynamic range $SFDR$,
- the signal-to-noise ratio SNR and also
- the centre frequency offset specification $\delta(f_{DDS})$.

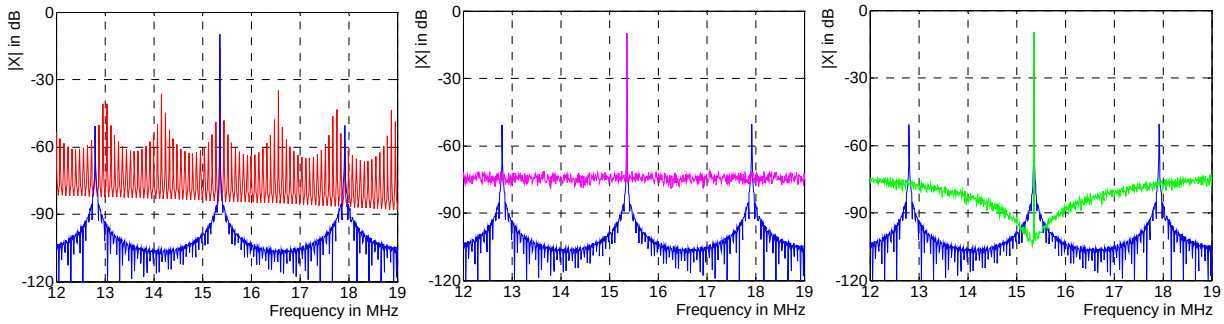

Fig. 4. **(a)** Pulse output DDS spectrum (red) versus spectrum after virtual clock enhancement (blue). **(b)** Spectrum after virtual clock enhancement (blue) versus spectrum after virtual clock enhancement and dithering (magenta). **(c)** Spectrum after virtual clock enhancement (blue) versus spectrum after virtual clock enhancement and noise shaping (green).

Additionally, a set of secondary conditions influences the system performance. The long-term stability of the reference clock $\delta\,(f_c)$ is exemplarily mentioned.

5 Derivation of design parameters for the RT level

According to the design flow shown in Fig. 1, a set of design parameters is derived from the system specification. In the case of the DDS these parameters are:
- the selection of an optimal reference clock frequency f_c,
- the minimum word width m of the phase accumulator,
- the minimum factor of the virtual frequency enhancement B and/or the word width v of the offset time and
- the selection of the jitter correction functions.

5.1 Minimum word width of operations

The necessary word width of the phase accumulator depends on several requirements and conditions. For this example we look to the phase accumulator introduced in Fig. 2.

On the one hand the necessary word width m can be determined from the relationship between used reference clock frequency f_c and the frequency resolution $\Delta\, f_{DDS}$. This function is illustrated for a special example in Fig. 5.

It shows that an optimal selection of f_c leads to a decrease of the implementation costs.

On the other hand the necessary word width m is fixed by the requirement to the centre frequency offset specification $\delta\,(f_{DDS})$.

This parameter depends on the quality of the system clock f_c and as well as on the accuracy of the number representation of the divisor relationship R.

The function can be determined with regards to the computation of errors. It is illustrated for a special example in Fig. 6. Again, an optimal selection of f_c leads to a decrease of the implementation costs.

The actually necessary word width is the maximum of both computed values.

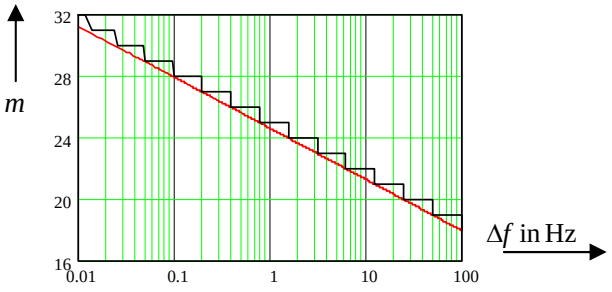

Fig. 5. Phase Accumulator word width required by frequency resolution specification.

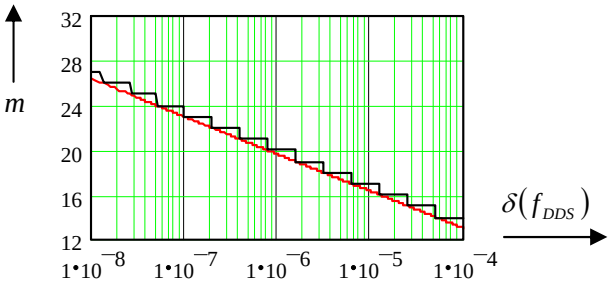

Fig. 6. Phase accumulator word width required by centre frequency offset specification.

5.2 Factor of the virtual clock frequency enhancement

The basic function of the virtual clock enhancement is based on the computation of the quotient from accumulator remainder value at the time of a generated overflow pulse and the value of the control word N.

Therefore a division component has to be implemented. The word width of the division result corresponds to v (Eq. 3). The implementation cost is determined by:
- the phase accumulator style and its word width m and
- the factor B of the virtual clock enhancement.

Additionally, factor B influences the complexity and the operating cost for the generation of the corrected pulse sequence, which is to operate by $f_{c,v}$.

The goal of the computations is to determine the minimum necessary v and/or B.

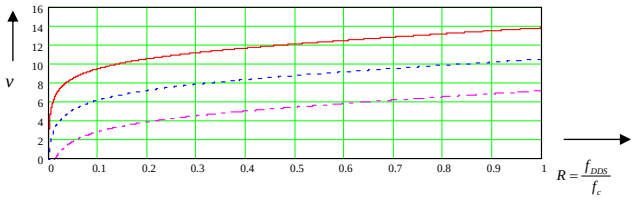

Fig. 7. Virtual clock enhancement factor (v) required by SFDR specification (red: SFDR = −80 dBc, blue: SFDR = −60 dBc, magenta: SFDR = −40 dBc).

Due to the virtual clock enhancement an absolute decrease of the jitter signal is observed. However, discrete spurs remain in the spectrum. Therefore the quality of the spectrum can be specified by the $SFDR$.

The formulas for the computation of the $SFDR$ of a DDS were derived by Richter (1999) and have been verified by simulations and measurements. Likewise, this has been done for the relationship to the improvement of the $SFDR$ using virtual clock enhancement.

The relationship is illustrated for a special example in Fig. 7.

Contrary to the conclusion drawn for the accumulator word width, in this case it is preferable to choose f_c much larger than f_{DDS}.

Figure 8 shows another example, which combines the virtual clock enhancement and a noise shaping algorithm.

The unwanted error signal at the DDS output is now a continuous noise signal.

Therefore the SNR has to be specified for a defined offset to the carrier signal, since it is not constant over the entire spectrum due to the noise shaping.

Usually the SNR is specified for several bandwidths.

It is possible to compute the envelope of the spectrum of the error signal.

The SNR is shown in Fig. 8 for a constant Δf over an entire tuning range f_{DDS}. It demonstrates to what extent the change of v affects the quality of the signal.

Only the respective local minima of these functions are relevant for the design decision.

6 Summary of the functional relationships

Considering 4 examples we have demonstrated, how the RT level design parameters can be derived.

It has been shown that based on a formal specification a suitable system configuration can be derived. The system parameters of the DDS itself have only little direct dependence.

In the following the relations between system parameters and draft decisions are summarized:

- The phase behaviour during a frequency change can be affected by the selection of the phase accumulator style.
- The list of the tuning ranges of the output frequency f_{DDS} determines the selection of the minimum necessary f_c and thus the timing constraints for the phase accumulator.

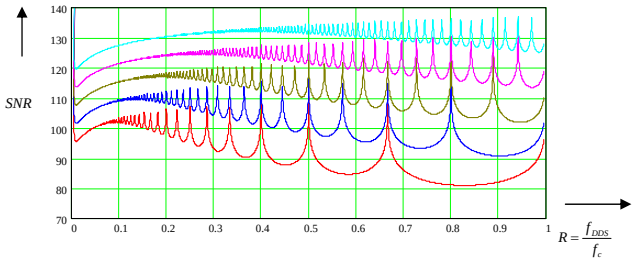

Fig. 8. SNR of a DDS after noise shaping with usage of different virtual Clock Enhancement factors (v) (cyan: v = 6,..., blue: v = 3, red: v = 2).

- The centre frequency offset specification δ (f_{DDS}) and the necessary frequency resolution Δf_{DDS} determine the word width of the phase accumulator.
- The specification of the $SFDR$ and the SNR affect the configuration of the procedures for the jitter correction including the factor of the virtual clock enhancement. From this, time conditions for the division and for the corrected pulse generation can be derived.
- The latency time for the achievement of the new f_{DDS} after a change of R is a criterion for possible pipelining of the signal processing operations.

7 Conclusions

It could be shown that a computational support is necessary for the transition of a formal system specification to a definition of the design parameters for a customised circuit synthesis (RT level specification).

This is due to the fact that the derivation of design parameters is essentially an optimisation task with many parameters.

A condition of this support is an IP-specific method adapted to each case. This consists of:

- a complete description of all specifiable system parameters (achievement parameters),
- a set of system architectures to configure and
- the complete description of the functional relationships of system and circuit parameters.

The decisions made in this design step form in the next step:

- the basis for the selection of a suitable IC technology and
- the specification for the RT level synthesis.

Acknowledgements. This work has been supported by the German Government (BMBF) under Grant No. 01 M 3059 F.

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