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Hybrid integrators with predictive overload estimation for analog computers and continuous-time ΔΣ modulators

Dirk Killat[1], **Bernd Ulmann**[2], **and Sven Köppel**[3]

[1]Microelectronics Department, Brandenburg University of Technology, 03046 Cottbus, Germany
[2]FOM University of Applied Sciences, Franklinstr. 52, 60486 Frankfurt a. M., Germany
[3]anabrid GmbH, Am Stadtpark 3, 12167 Berlin, Germany

Correspondence: Dirk Killat (killat@b-tu.de)

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Abstract. Continuous-time integrators are a central component in ΔΣ modulators, in analog computers, and general analog signal processing. If several integrators are interconnected, scaling plays an important role: In analog computers, scaling is performed with respect to the machine unit (MU). In ΔΣ modulators, scaling is performed in such a way that at maximum input signal the allowable dynamic range of no integrator is exceeded. In both cases the scaling is a compromise limiting the dynamic range.

For analog computers, it was proposed early on to extend the dynamic range by hybrid integrators. Here, an analog range overflow is processed digitally and the analog integrator is reduced to its permissible operating range within the machine unit interval. While in earlier proposals for hybrid integrators only the subsequent integrator stage processes the overflow and works with reduced analog values, our hybrid integrator can process the overflow directly, with the analog reset process being continuous-time.

In the case of highly dynamical input signals and transients, analog overload handling is further improved by a prediction of the overload that includes the currently applied input signal in the calculation. For example, with continuous-time ΔΣ modulators, overload of the analog integrator can be reliably avoided.

1 Introduction

Analog continuous-time (CT) integrators are a fundamental building block in analog computers (Howe, 2005), in continuous-time ΔΣ ADCs (Ortmanns and Gerfers, 2006), in robust analog controllers (Jin et al., 2022), and many other analog signal processing circuits. Analog computers are popular for solving and simulating differential equations, which usually involves connecting integrators in series, typically with some sort of feedback loop. The series of integrators in ΔΣ modulators makes it possible to achieve higher-order noise shaping and, accordingly, to reduce the quantization noise in the signal band.

The problem of amplitude scaling will be illustrated in the following by a spring-mass damper system (Hall and Kahne, 1970; Ulmann, 2022; Navarro, 1962): Let the system have a spring stiffness of $60\,\mathrm{kg\,s^{-2}}$, a damping coefficient of $3\,\mathrm{kg\,s^{-1}}$, a mass of 1.5 kg, and an initial displacement of 0.1 m. A Matlab-Simulink model for this is shown in the upper part of Fig. 1.

The simulation result of the unscaled differential equation is shown in Fig. 2a.

It can be seen that $\ddot{y}$, $\dot{y}$, and y are scaled unevenly, i. e., the dynamic range is not used optimally. To optimize the problem for the hardware of an analog computer, the amplitude range of the quantities must be scaled to the machine unit (MU). In modern discrete analog computers the machine unit can be e.g. 10 V (Ulmann et al., 2021), so that the amplitudes of the signals should be as close as possible to the 10 V, but the 10 V must not be exceeded. For scaling, experience with the implemented mathematical equation is required, or one can try to optimize the scaling experimentally. A solution for scaling to 10 V would be the substitution $\ddot{y} \Rightarrow \left[2/5\,\ddot{Y}\right]$, $\dot{y} \Rightarrow \left[15\,\dot{Y}\right]$ and $y \Rightarrow [100\,Y]$. To scale the model, $1/m$, d, and s are multiplied by the reciprocal scaling factors. In addition to that, the integrators must be scaled as well at their inputs (Fig. 1 below). The simulation of the model scaled to 10 V is shown in Fig. 2b.

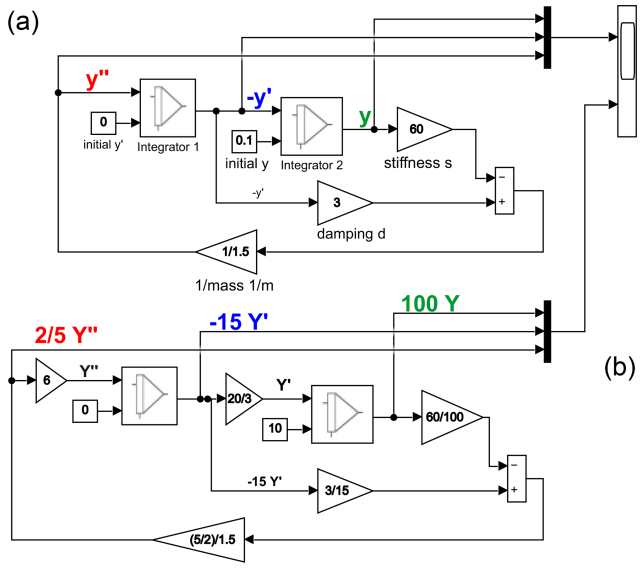

Figure 1. Unscaled **(a)** and scaled spring-mass damper system **(b)**.

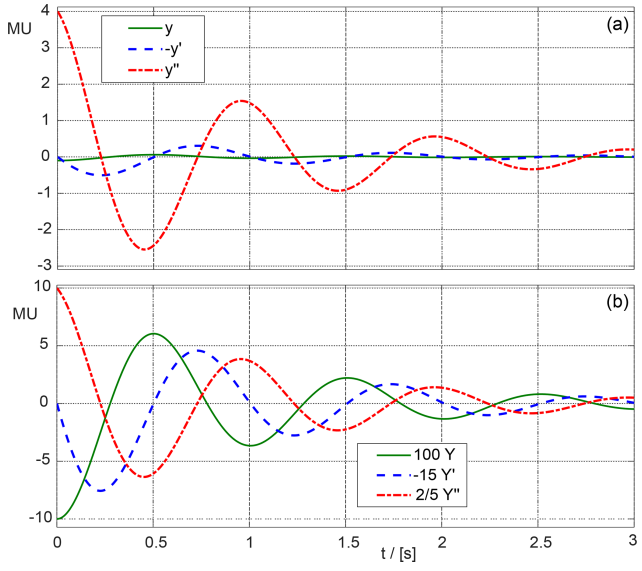

Figure 2. Simulation result of the unscaled **(a)** and scaled **(b)** spring-mass-damper system.

In addition to amplitude scaling, scaling in the time domain can also be performed. This is used to adapt the mathematical task to the bandwidth and slew rate of the electronic circuit components. Time scaling adapts the real time of the simulated model (also called wall clock) to the simulation or machine time. Thereby the simulation time can run faster or slower than the wall clock time.

The hybrid integrator solves the problem of amplitude scaling. The time scaling is independent of this. However, very different time constants in a mathematical problem also lead to problems with amplitude scaling, so that the hybrid integrator can also be used to an advantage in such cases.

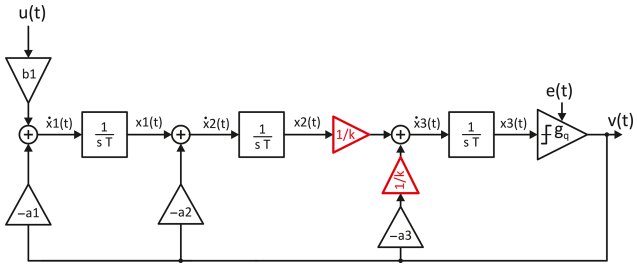

Figure 3. Scaling problem in a single-loop CT ΔΣ modulator.

The operation of scaling in ΔΣ modulators is shown in Fig. 3, showing a 3rd order modulator with distributed feedback and 1-bit quantizer. In the chain of integrators, the amplitudes must be scaled down by a factor $1/k$ towards the end, as exemplified by the 3rd integrator. There are two main reasons for this: In the case of the 3rd order modulator, stability is improved because the gain g_q of the linearized 1-bit quantizer increases and only then the modulator becomes conditionally stable (see, e.g., Ortmanns and Gerfers, 2006, Chap. 2.7.4). Another and decisive reason for scaling in ΔΣ modulators is the necessity to limit the signal amplitudes to the practical dynamic range of the analog integrators.

By downscaling the signal amplitudes the actually achievable signal-to-noise ratio is reduced. Therefore, attempts have already been made to both increasing the stability of the modulator and increasing the dynamic range (Au and Leung, 1997; Shim et al., 2005a, b) by local detection of the overflow at the individual integrators of the modulator, a subsequent AD conversion of the overflow, and a local negative feedback directly at the integrator.

Section 2 of this paper reviews the principle of the hybrid integrator originally designed for analog computers, explains the basic operation of the hybrid integrator, and presents its fundamental drawback. In Sect. 3, the hybrid integrator with CT reset presented in (Killat et al., 2022) is compared in detail with previous solutions. In Sect. 3.2, a new range overflow estimation is introduced that optimizes the dynamic range, especially for transient input signals or use in ΔΣ modulators. In Sect. 4 the operation of the hybrid integrator with CT reset and with overload estimation is illustrated by examples.

2 First proposals for hybrid integrators

The first approach to hybrid integrators was presented in Skramstad (1959) and was the starting point of subsequent work by Wait (1963); O'Grady (1966). At that time, the emphasis was on extending the dynamic range for the solution of differential equations. The devices available at that time hardly allowed a capacitive reset as proposed in the integrated solution of Bryant et al. (2012). Therefore, the overflow from the analog integrator to the digital counter had to

be realized by a time-continuous compensation in the subsequent hybrid stages of the integrators, which works well for classical problems like spring-mass-damper systems or harmonic oscillators due to the negative feedback of the integrators and is therefore often used as an example for the functionality of hybrid integrators in papers of that time.

2.1 Hybrid integrator basics

First we describe the basic principle of hybrid integration according to Skramstad (1959):

The integrator integrates the input variable X over time t with initial value $Y(0)$. T is the time constant of the integrator:

$$Y = Y(0) + \frac{1}{T}\int_0^t X\,\mathrm{d}t \tag{1}$$

In the hybrid integrator, the integration variable X and the integral Y are decomposed into an analog and a digital component:

$$X = X_\mathrm{D} + X_\mathrm{A} \tag{2}$$
$$Y = Y_\mathrm{D} + Y_\mathrm{A} \tag{3}$$

Thus, the analog and digital components of X are integrated. The initial values are also divided into analog $Y_A(0)$ and digital $Y_D(0)$ components:

$$Y = Y_D(0) + Y_A(0) + \frac{1}{T}\int_0^t (X_\mathrm{D} + X_\mathrm{A})\mathrm{d}t \tag{4}$$

The integral over the analog X_A and digital component X_D of X can be decomposed into a sum, an instantaneous term and an integral over time t. The digital component is integrated in multiples of the time interval Δt. The instantaneous value of the integral in the nth time interval is:

$$Y = Y_D(0) + Y_A(0) + \frac{1}{T}\left[\sum_{i=1}^{n-1} X_D(i)\Delta t + X_D(n-1)\tau + \int_0^t X_\mathrm{A}\mathrm{d}t\right] \tag{5}$$

here $X_D(i)$ is the value of X_D in the ith time interval. Assuming that the initial values $Y_D(0)$ and $Y_A(0)$ are both 0, Fig. 4 shows the integral of Eq. (5). The summand with index $i = 0$ to $n-1$ is the Integral 1 in Fig. 4. The second term $X_D(n-1)\tau$ is the instantaneous value of the digital integral in the time interval $[(n-1)\Delta t, (n-1)\Delta t + \tau]$ and denoted Integral 2 in Fig. 4. The third term, the analog part of the integral, is Integral 3.

Figure 5 shows the block diagram of the hybrid integrator according to Skramstad (1959). The digital part consists of two registers R1 and R2. R1 represents the Integral 1,

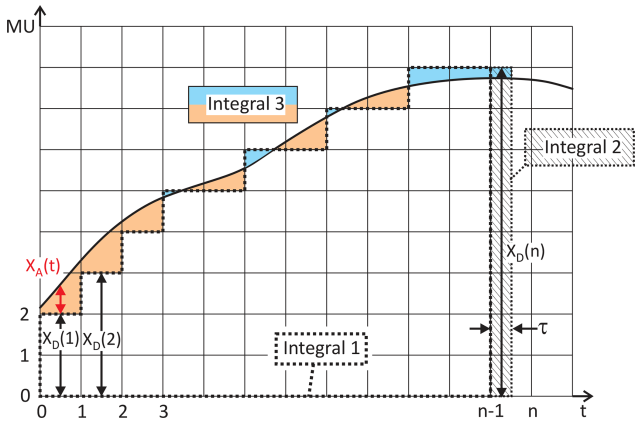

Figure 4. Contributions to the hybrid integral, following Skramstad (1959).

that accumulates with each clock, at each time step $n\Delta t$, the value $X_D(n-1)$ from the register R2 and the change $\Delta X_\mathrm{D} = X_D(n) - X_D(n-1)$. This change is generated by a window comparator with thresholds $\pm\frac{1}{2}$ MU (MU, machine unit). The digital value of Integral 1 is DA-converted by DAC1, added up with other analog components of the integral and then fed to the analog output Y_A of the integrator. Since $Y_\mathrm{A}(t)$ is supposed to represent the analog part of the integral without the digital part, DAC1 gets the −MU as reference for Integral 1.

The value $X_D(n-1)$ of the register R2 is transferred via DAC2 with +MU as reference to an integrator INT2, which is periodically reset at the instants $n\Delta t$. This generates a sawtooth voltage representing the instantaneous value of Integral 2, which is added to the output Y_A by means of a summer.

The analog portion of Integral 3 with input $X_\mathrm{A}(t)$ is integrated and added directly to Y_A. Assuming that $X_\mathrm{A}(t)$ corresponds to $Y_\mathrm{A}(t)$ of the previous integrator stage, and that $Y_\mathrm{A}(t)$ is obtained by subtracting the digital part of Integral 2, Integral 3 is the color-coded area in Fig. 4. It may become positive or negative. If several hybrid integrators are concatenated and fed back, as is the case when solving differential equations in analog computers, Integral 3 is indirectly minimized in the individual hybrid integrators by keeping $Y_\mathrm{A}(t)$ small in size by subtracting the digital parts of the total integral.

2.2 Disadvantage of the previous hybrid integrator

From Fig. 5 it can be seen that the hybrid integrator has no local feedback, i. e. if $Y_\mathrm{A}(t)$ exceeds $\pm\frac{1}{2}$ MU, this is added to Integral 1 and the analog output $Y_\mathrm{A}(t)$ is reduced in amount accordingly, but the value of integrator for Integral 3, i. e., the actual analog integrator, is not reduced in amount. The reduction occurs indirectly when the chain of integrators is fed back eventually.

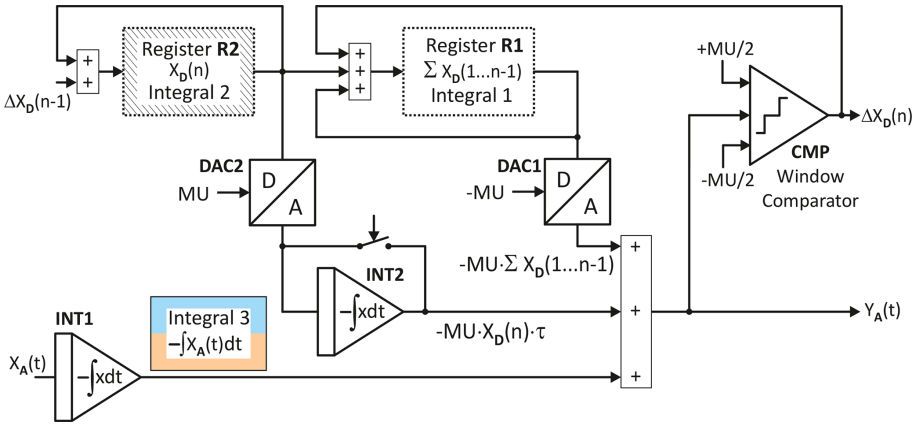

Figure 5. Hybrid integrator block diagram, based on Skramstad (1959).

The operation and efficiency of the hybrid integrator presented so far is demonstrated in Skramstad (1959); Wait (1963); O'Grady (1966) on examples with feedback, i. e., by means of using differential equations such as $\dot{y} = -y$ or $-\ddot{y} = y$. For general applications in analog computing or instrumentation, the previous hybrid integrator does not allow to constrain the actual analog integral of the hybrid integrator, because a local feedback on the analog integrator component is missing.

The issue of a hybrid integrator requiring local feedback is addressed in Bryant et al. (2012). Here, a partial capacitive reset of the integrator is performed when a window comparator exceeds its thresholds. The problem is that the reset does not have an ideal voltage waveform, i. e., the digital portion of the hybrid integrator does not match the corresponding analog portion just after the reset signal. While this can be systematically taken into account in CT-$\Delta\Sigma$-modulators by the Laplace transforms of the feedback DAC, and only influences the noise shaping, the non-ideal voltage curve in the switched-capacitor-based reset of the hybrid integrator leads to errors in the result of an analog computing circuit.

In Tsividis and Guo (2015) it is proposed to avoid a capacitive reset by reversing the integration direction when a reference threshold voltage is exceeded. A disadvantage of this method are the required continuous-time comparators, which have to detect an overflow of the integrator asynchronously. By reversing the direction of integration, a reset can be avoided, but the accuracy of the threshold of the continuous-time comparators is crucial for the transfer from the analog integrator to the digital counter.

3 Hybrid integrator with local continuous-time reset

Based on Bryant et al. (2012), a partial reset of the analog integrator will be realized when the range of the window comparator CMP is exceeded. The reset will be realized by a continuous square wave signal instead of a switched capacitor

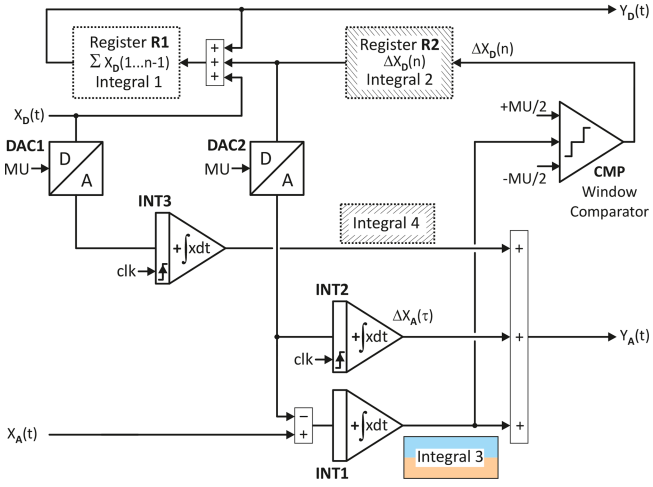

Figure 6. New hybrid integrator with local feed back.

circuit. This subsequently requires further compensation to represent the correct timing characteristics of the integrator when the digital part of the hybrid integrator switches.

3.1 Operating principle of new hybrid integrator

The improved hybrid integrator with local feedback is shown in Fig. 6. The corresponding integrals of the analog and digital parts of the total integral are depicted in Fig. 7. The digital portion of this total integral, Integral 1, is held in register R1. This register sums the digital input X_D and ΔX_D and represents the digital portion Y_D of the current hybrid value of the integrator.

The improved hybrid integrator requires three analog integrators INT1 to INT3, two of which are periodically reset by the clock. The integrator INT1 forms the analog Integral 3. Its output is given to a window comparator CMP, which generates the digital overflow ΔX_D when the thresholds are exceeded, which is then DA-converted with +MU

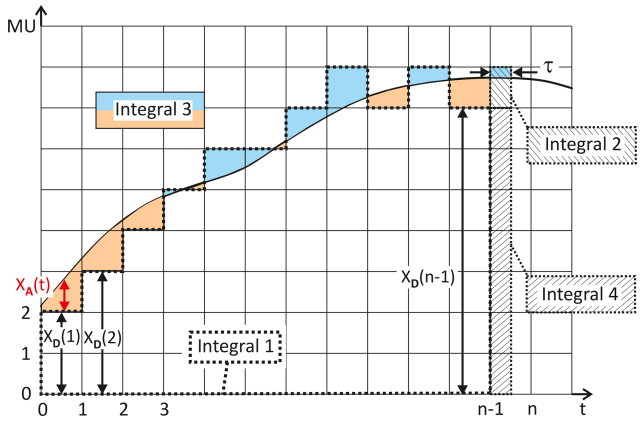

Figure 7. Composition of integral of new hybrid integrator.

as a reference in DAC2 and then negatively fed back to the analog input of the integrator INT1 for Integral 3. Since the window comparator directly measures Integral 3 and since there is negative feedback in the case of digital overflow, this improved hybrid integrator achieves a constraint on the analog Integral 3 even without arranging the hybrid integrator in a loop, unlike the solutions shown in Skramstad (1959); Wait (1963); O'Grady (1966).

The digital overflow results in a linear characteristic of the reset of Integral 3. However, because the overflow is not yet stored in the digital output register R1 with the value Integral 1, the linear reset must be compensated with an opposite ramp $\Delta X_\mathrm{A}(\tau)$ provided by the analog integrator INT2. This ensures that at each time $Y = Y_\mathrm{A} + Y_\mathrm{D}$ represents the correct value of the hybrid integral.

If a digital overflow X_D is present at the input of the hybrid integrator, it will only be taken into account in the following clock cycle of the register for Integral 1 and must therefore be DA-converted with DAC1 and then fed to the sum Y_A with integrator INT3 to obtain the correct total integral Y at any time.

Figure 7 shows the composition of the integral. Integral 1 is identical to the previously shown hybrid integrator. Integral 2 in the improved hybrid integrator no longer has the current analog represented value of $X_\mathrm{D}(n)\tau$, but only the value $\Delta X_\mathrm{D}(n)\tau$, which certainly simplifies the scaling of the summation. To obtain the correct instantaneous value for a digital input quantity, the digital input X_D must be integrated analogously and fed to the analog output component $Y_\mathrm{A}(t)$. This component corresponds to Integral 4.

The analog output $Y_\mathrm{A}(t)$ consists of three signals, Integral 3, the sawtooth shaped compensation of the time-continuous reset with $\Delta X_\mathrm{A}(\tau)$, and the analog representation of the digital input of Integral 4. Integral 3 and $\Delta X_\mathrm{A}(\tau)$ are smaller in magnitude than the machine unit (MU). Integral 4 also has a sawtooth shape, but can exceed 1 MU and reach $X_\mathrm{D}(t)\Delta t$ at its peak. If $Y_\mathrm{A}(t)$ must be explicitly generated with a summer and represented as a voltage, the fraction represented by Integral 4 limits the dynamic range. However, if the hybrid integrator is followed by another stage with a hybrid integrator, the three components of $Y_\mathrm{A}(t)$ are fed into the following analog part of the hybrid integrator via separate resistors, so that the dynamic range is not limited, because the sum signal $Y_\mathrm{A}(t)$ does not occur explicitly as a voltage. Instead the sum is formed by the summer circuit of the following analog integrator.

Figure 8 shows the signal waveforms of the hybrid integrator.

First we consider the left side of Fig. 8 where a constant input signal $X_\mathrm{A}(t)$ is present. The analog integrator signal $\int X_\mathrm{A}(t)\mathrm{d}t$ reaches a maximum of $\frac{1}{2}$ MU (with MU$= 1$) and then integrates back to zero level. To obtain the correct value of the analog component $\int X_\mathrm{A}(t)\mathrm{d}t + \Delta X_\mathrm{A}(\tau)$ in the time domain from $t = 1$ to $t = 2$ in the presence of the continuous-time reset, the value $X_\mathrm{D}(n)$ from register R2 is AD-converted and integrated with INT2 and then added to the analog integral as a ramp signal $\Delta X_\mathrm{A}(\tau)$. Without this ramp signal $\Delta X_\mathrm{A}(\tau)$ the value of the total integral in the phase of the continuous-time reset would not represent the correct value, as shown by the hypothetical waveform of $\int X_\mathrm{A}(t)\mathrm{d}t + \Sigma X_\mathrm{D}(1\ldots n-1)$ in the lower part of Fig. 8.

On the right side of Fig. 8 the input signal is switched off at $t = 2.5$ and again at $t = 3.5$. The final values of the total integral are $\int X_\mathrm{A}(t) + X_\mathrm{D}(t)\mathrm{d}t = 1.25$ and 1.75. The comparator CMP switches at $t = 1$ and, if the input signal is present until $t = 3.5$, again at $t = 3$ (red mark). Therefore the digital sum signal $\sum X_\mathrm{D}(1\ldots n-1)$ first reaches the value 1 and then the value 2. The final values of the analog part $\int X_\mathrm{A}(t) + \Delta X_\mathrm{A}(\tau)$ are $+0.25$, and -0.25 respectively. If comparator threshold is $\frac{1}{2}$ MU, the analog part of the integral can also take the opposite sign with respect to the input signal.

3.2 Improve dynamics with overload estimation

The values of the thresholds of the window comparator are not 1 MU, but 0.5 MU, as it is the case in previous integrators and in the hybrid integrator presented here. These are chosen for two reasons: First, the magnitude of the analog integral is kept minimal, even though the analog integral may change sign with respect to the input signal in this case (Fig. 8), which is not a disadvantage. Second, the analog integrator output follows with a delay in the case of time-varying input signals, so that an overload would also only be detected with a certain delay. Due to the reduced threshold, an overload can be avoided even with delayed detection.

Further improvement of the dynamic characteristics are possible if, as in the case of the overload estimation (OLE) circuit used in Shim et al. (2005a), the integrator takes into account not only the actual analog integrator output, but also the value currently present at the integrator input for detecting the overflow from the analog to the digital component of the integrator.

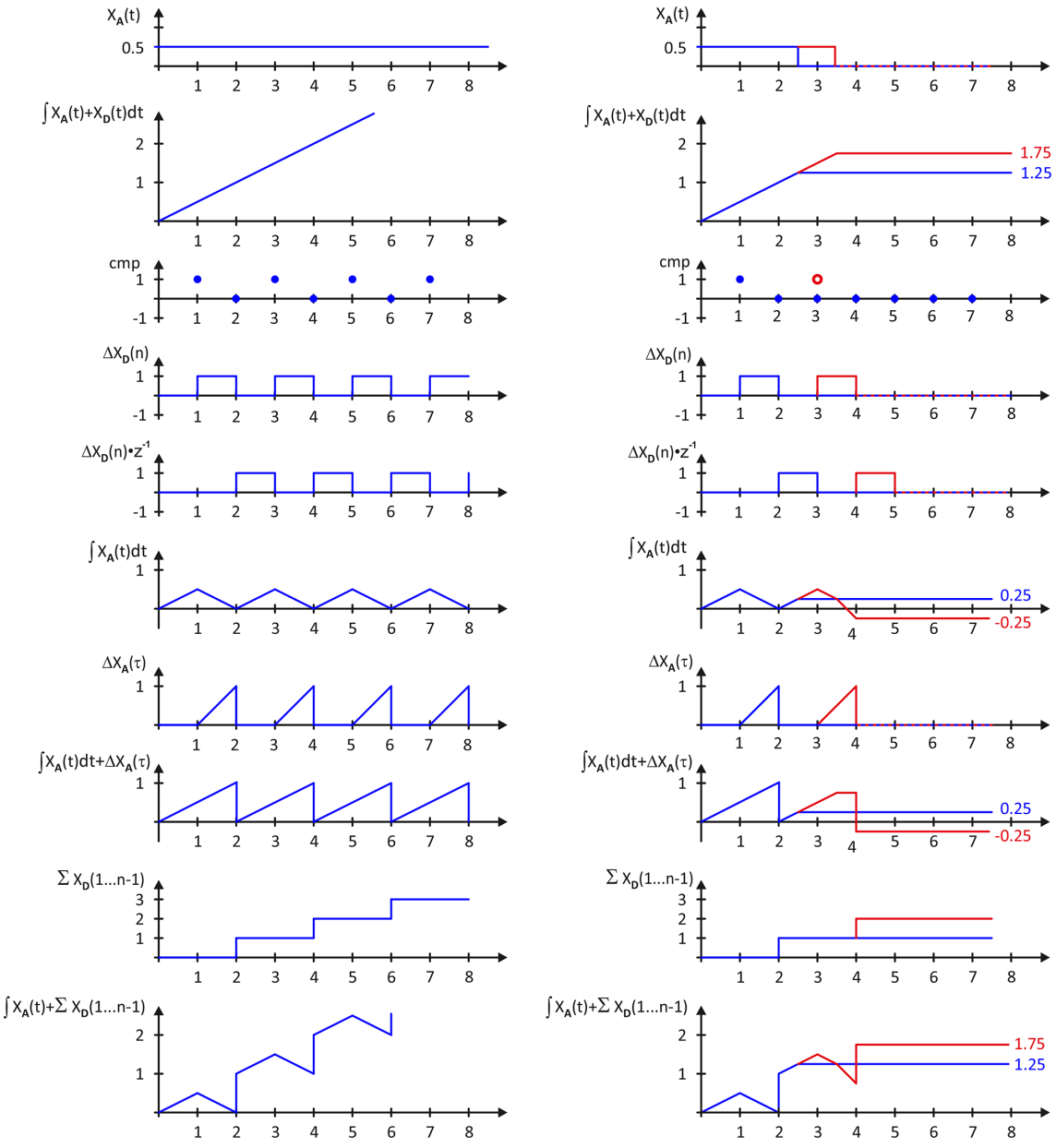

Figure 8. Signal characteristics with the new hybrid integrator.

Figure 9 shows an improved version of the hybrid integrator, where the analog input $X_A(t)$ is scaled by a gain factor for the overload estimation (OLE) G_{OLE} and is added to the Integral 3 $= \int X_A(t)dt$ and then fed to the window comparator CMP. The window comparator has adjustable thresholds, usually smaller than the machine unit MU. The advantages of predicting analog integrator overflow are particularly evident in the improved dynamic behavior of the CT $\Delta\Sigma$ modulator with hybrid integrator presented in Sect. 4.4.

4 Application examples

In the following, we will demonstrate the operation of the hybrid integrator with local feedback using two classical examples, the harmonic oscillator and a damped spring-mass system. We then show a spiking neuron according to Hindmarsh and Rose (1984), which has significantly different time constants in the three differential equations and requires the scaling of at least one variable. Finally, we demonstrate the operation and advantages of the hybrid integrator with overload estimation using a second-order CT $\Delta\Sigma$ modulator. However, we do not perform detailed analyses of SNR or noise

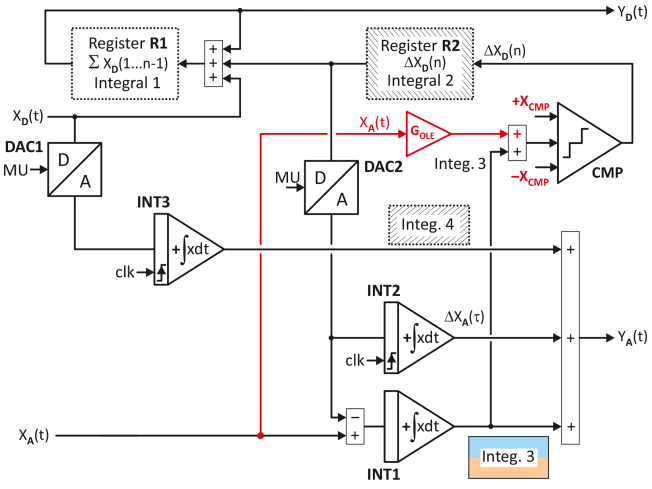

Figure 9. New hybrid integrator with local feed back and predictive overload estimation of analog integrator.

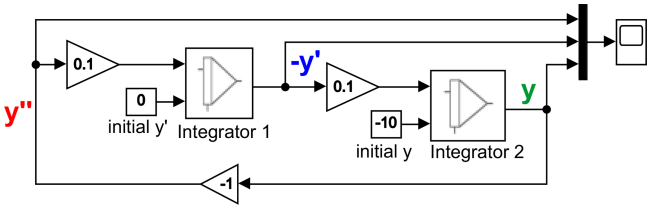

Figure 10. Block diagram of the harmonic oscillator.

shaping, but take a look at the integrator states in the presence of step changes in the input signal at the limit of the dynamic range.

4.1 Harmonic oscillator on an analog computer

In this practical example the harmonic oscillator described by the differential equation $-\omega^2\ddot{y} = y$ is implemented. Figure 10 shows the Simulink model of such an oscillator, built from pure analog integrators.

The analog computer circuit consists of integrators configured in a loop with coefficient elements $\omega = 0.1$ in between. A selection of signals from the harmonic oscillator simulation is shown in Fig. 11: The first diagram represents the signals $Y_A + Y_D$ (y, in green color) composed of analog and digital parts, $-\dot{Y}_A - \dot{Y}_D$ (y', in blue color), and $\ddot{Y}_A + \ddot{Y}_D$ (y", in red color). In the middle and bottom diagrams of Fig. 11, the analog and digital portions of $Y_A + Y_D$ (ya, in green color, yd, in light green color) and $\dot{Y}_A + \dot{Y}_D$ (y'a, in blue color, y'd, in light blue color) are shown.

The initial condition is $Y_A(0) + Y_D(0) = 10$. This is realized by an initial digital value $Y_D(0) = 10$, as can be seen in the middle of Fig. 11. Depending on how the digital LSBs are scaled with respect to the machine unit MU, not only multiples of the MU can be used as initial values in the hybrid integrator, but also fractions of a MU. Most of the amplitude

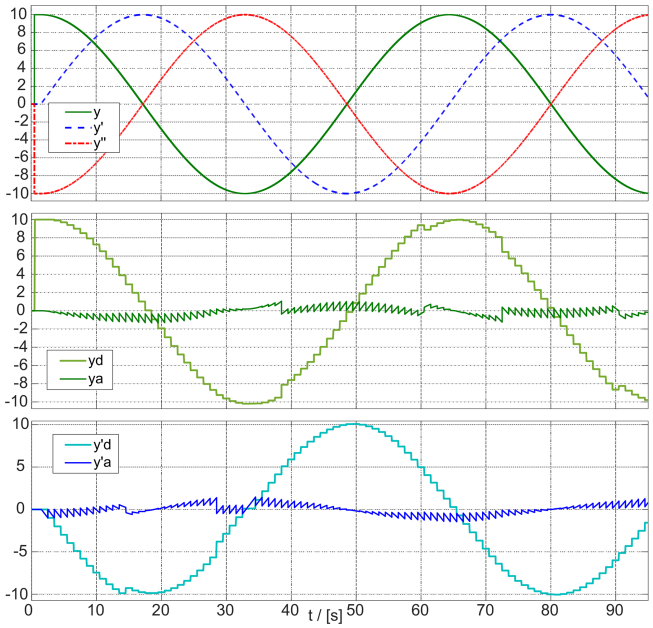

Figure 11. Simulation of harmonic oscillator with hybrid integrators.

is exchanged digitally between the integrators in the oscillator, as can be seen from the digital values Y_D and $\dot{Y}_D$ which reach full scale value 10. The analog parts Y_A and $\dot{Y}_A$ exceed MU only slightly up to approximately 1.5 MU, when $Y_A + Y_D$ and $\dot{Y}_A + \dot{Y}_D$ have their zero crossings, i. e. when their derivative is at maximum amplitude. Crucial for this is that the digital slew rate of the Integral 1 is of the order of the slew rate of the total integral of the hybrid integrator.

4.2 Spring-mass-damper system on an analog computer

As a second example for the application of the hybrid integrator a damped spring-mass system is considered. The Simulink block diagram for this is shown in Fig. 12. At the top of the block diagram, a purely analog and continuous-time system is set up as a reference. The model corresponds to the unscaled model of Fig. 1, the result should correspond to the simulation result of Fig. 2.

The integrators in the reference model are inverting. An initial value of 0.1 at the input of the second integrator thus leads to an initial displacement of −0.1. The Simulink module of the hybrid integrator is not inverting, so in Fig. 12 inverters are provided at the outputs reg_sum, A_int, and AD_int, respectively. reg_sum and A_int represent the analog and digital parts of the integral, respectively. At A_int the respective total integral is output after that the sign is changed and then output as yad (in green color), -y'ad (in blue color) and y"ad (in red color) shown in Fig. 13 above.

The period of the damped oscillation is about 1 s. For the digital part of the hybrid integrator to follow the signals, the

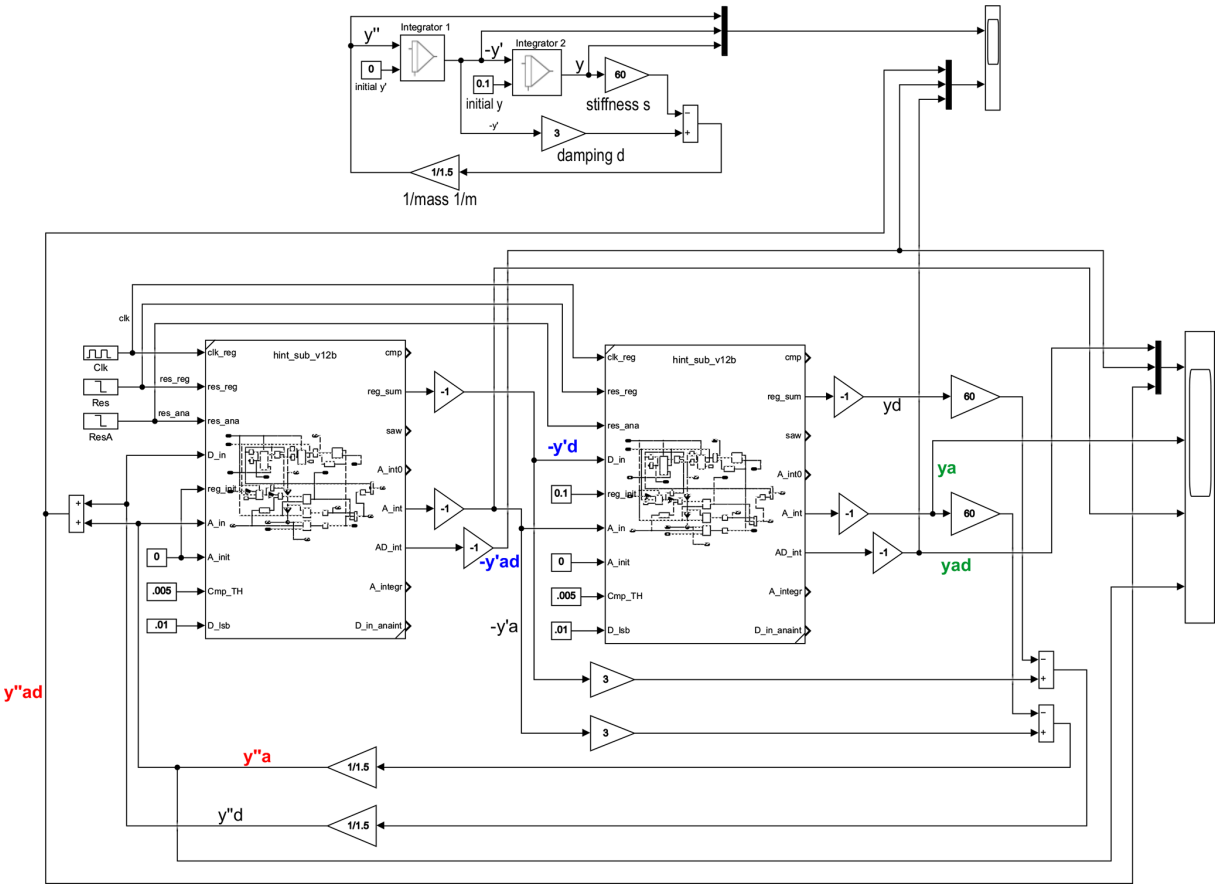

Figure 12. Matlab-Simulink block diagram of spring-mass-damper system with hybrid integrator.

clock frequency must be a multiple of the oscillation frequency. Therefore, the clock frequency was set to 100 Hz. To ensure that the digital portion of the integral has sufficient resolution, the equivalent analog value of a digital LSB was set to 0.01. The threshold value of the comparator is $\frac{1}{2}$ LSB. Since Register R1 (in Fig. 6) adds up the digital input $X_{\mathrm{D}}(t)$ 100 times per second, digital integration requires scaling down the input $X_{\mathrm{D}}(t)$ to the Register R1 by a factor of 100. If the Register R2 already contains the comparator value scaled down to the LSB, it must be scaled up again at DAC1 to generate the ramp signal $\Delta X_{\mathrm{A}}(\tau)$ with slope 1 in integrator INT2.

In Fig. 13, in addition to the overall analog-digital quantities of the spring-mass-damper system, the respective analog portions ya (in green color), -y'a (in blue color) and y"a (in red color) are plotted. Since already y'a never exceeds 3 LSB, the pure analog fraction ya is never larger than 0.7 LSB, the (not shown) analog fraction Integral 3 representing $\int X_{\mathrm{A}}(t)\mathrm{d}t$ is also only 0.2 LSB at most. With the chosen scaling with a small LSB and high clock frequency related to the oscillation frequency, no overflow from analog to digital takes place in the 2nd integrator.

The 1st integrator generates -y'a, having a maximum magnitude of 4 LSB. The fraction of Integral 3 of the first integrator is 0.5 LSB at most. Although -y'a exceeds 1 LSB this does not represent an overload: The peaks of the sawtooth-shaped waveform result from the high values at the digital input of the first integrator, which generate the periodic linear ramped integral component Integral 4 with the DAC1 and INT3. In practice, however, Integral 4 and Integral 3 are not added first, as shown in the block diagram. Instead, the summation is done with an adder circuit at the analog integrator in the subsequent second hybrid integrator.

In Fig. 13 y"a shows the largest values of all analog signals, which results from the factor 60 due to the spring constant. The analog input to the first integrator is therefore up to 30 LSB, resulting in overflows from analog to digital being generated in the first integrator, which can be seen from the steps in the sawtooth waveform of y'a.

The hybrid integrator enables simple interconnection of analog computing components without the need for scaling.

4.3 Spiking neuron

The third example is the implementation of a spiking neuron described by a set of differential equations on the analog

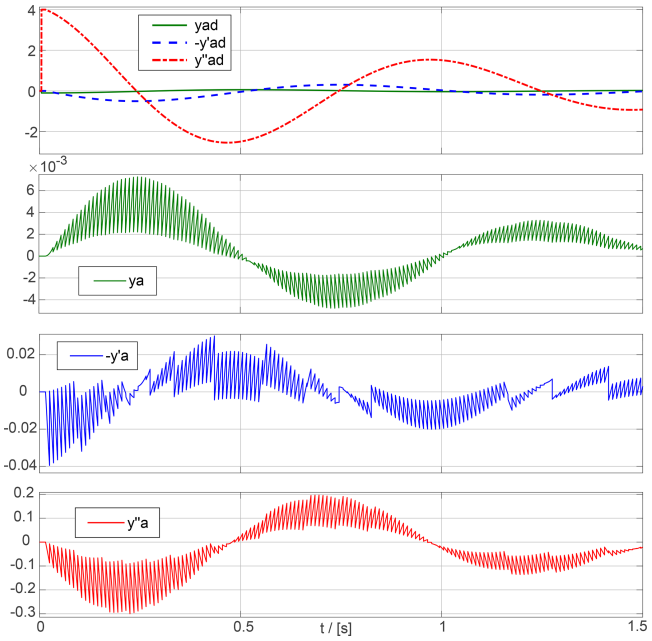

Figure 13. Matlab-Simulink simulation of spring-mass-damper system with hybrid integrator.

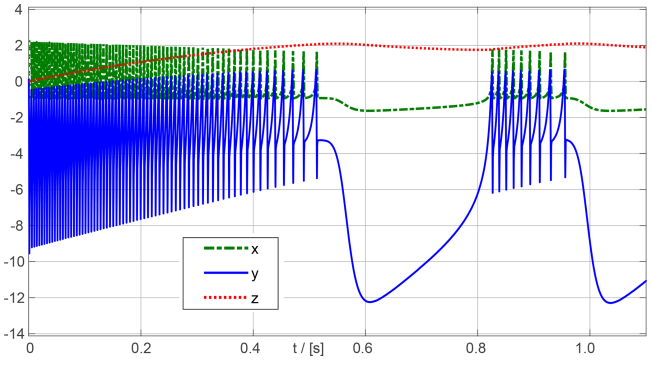

Figure 14. Simulation of spiking neuron $\dot{y}$.

computer. A well-known model here is that of Hindmarsh and Rose (1984), which consists of three coupled differential equations:

$$\dot{x} = y - ax^3 + bx^2 + I - z \tag{6}$$

$$\dot{y} = -dx^2 + c - y \tag{7}$$

$$\dot{z} = r\,(s\,(x - x_r) - z) \tag{8}$$

A bursting behavior as in Hindmarsh and Rose (1984) is obtained when $a = 1$, $b = 3$, $c = 1$, $d = 5$, $r = 10^{-3}$, $x_r = -\frac{5}{8}$ and the external current is set to $I = 2$. Scaling the equations in time by multiplying the three derivatives $\dot{x}$, $\dot{y}$, and $\dot{z}$ by a factor 1000, the neuron starts the first burst of pulses after 0.8 s simulation time, as shown in Fig. 14.

In the analog computer the integrator around y has a short time constant and simultaneously a large signal amplitude. Therefore the outputs of the integrators must be scaled down to the machine unit MU. For this purpose, x and z would be divided by 2, and y would be scaled down by a factor of 15.

An alternative to the extensive downscaling of y is the use of a hybrid integrator, as realized with the model in Fig. 15.

The three coupled differential equations require three integrators, integ_X, integ_Z, and integ_Y_hybrid. The hybrid integrator for y is operated at a clock rate of 10 kHz. The initial values for each of the three integrators are 0. The constant components are switched on after the start of the simulation and the initialization of the hybrid integrator after a clock period, i. e. after 100 µs.

The integrator for $\dot{y}$ has direct feedback, as shown by Eq. (7). The feedback is also linear, so in contrast to the integrator for $\dot{x}$, it has no second or third powers in the feedback path. Therefore, it is possible to feed back the analog and digital components y_d and y_a separately to the analog and digital inputs of the hybrid integrator. In this case, only the clock frequency must be taken into account in the time scaling process. While the scaling factor 1000 is still used at the analog input ya' and thus the simulation is accelerated accordingly compared to the real time (wall clock), for the digital feedback at -yd the scaling factor 1000 has to be reduced to 0.1 because of the clock frequency of 10 kHz. Figure 16 shows in two diagrams respectively the curves of y, ya and yd.

To ensure that the analog overdrive, which is detected by the window comparator and thus increases the digital registers, is dominant over the negative digital feedback in any case, the digital LSB must be selected to be 2. As a result, a decrease of the analog ya can be limited to -2 on average, and even for transients to about -2.5 (lower figure in Fig. 16).

This example shows that when using hybrid integrators in analog computers it is not necessary to replace all integrators by hybrid integrators, instead this can be done according to the application. Furthermore, a local digital feedback can be implemented, but it must be ensured that a negative digital feedback does not prevent the carry over from analog to digital and thus the limiting of the output of the analog integrator. The digital part of the hybrid integrator can be converted from analog to digital by passing the individual bits of yd through weighted resistors to the summation input of integ_X.

4.4 CT ΔΣ modulator

In the last example, a hybrid integrator with predictive overload estimation (OLE) according to Fig. 9 was used to realize a CT ΔΣ modulator of second order without scaling. The modulator is constructed as in Fig. 3, only with 2 integrators. The coefficients are $b1 = 1$, $a1 = 1$ and $b2 = 2$. The b-coefficients are connected to the digital inputs $X_\mathrm{D}(t)$ of the digital integrators. The hybrid integrators have a LSB = 1, comparator thresholds of $\frac{1}{2}$ LSB, and a clock period $T = 1$ s. The respective input $X_\mathrm{A}(t)$ is weighted by a factor $G_\mathrm{OLE} =$

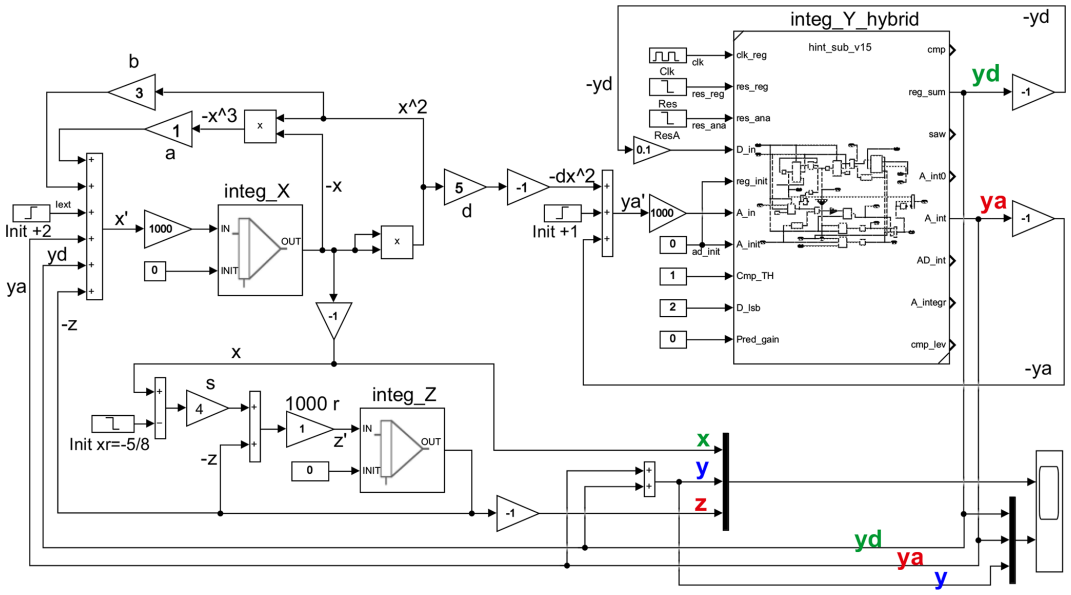

Figure 15. Model of spiking neuron with hybrid integrator for integration of $\dot{y}$.

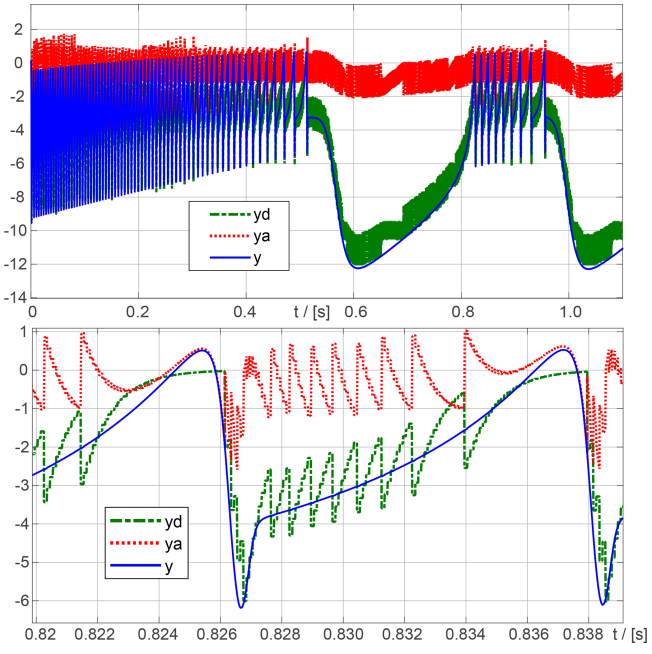

Figure 16. Simulation of spiking neuron with hybrid integrator for variable y.

0.5 for overload estimation and then added to the Integral 3. The clock of the quantizer is delayed by half a clock period, i. e. the registers and the comparator in the hybrid integrator operate on the rising clock edge, the quantizer on the falling clock edge.

In a Matlab-Simulink simulation bench, the time responses of the analog and digital components of the hybrid integrators are compared. The integrator with OLE according to Fig. 9 is compared with a version without OLE according to Fig. 6. We pay attention to how the hybrid integrators cope with overloads due to large input signals.

Both versions of the modulator, with and without OLE, of course give the same overall results, as shown by the bit stream v and the integrator outputs x1 and x2 in Fig. 17. The top plot in Fig. 17 also shows the input signal u increasing from 0.05 to 0.95 at $t = 5$ s, triggering the overload.

The two middle plots of Fig. 17 show the analog and digital components of the first integrator, the two lower plots those of the second integrator. Herein x1d, x2d, x1d_o and x2d_o are the digital parts, x1a, x2a, x1a_o and x2a_o the analog parts. Signal names ending with _o belong to the integrator with overload estimation. Signal names ending in ... a_I3 are the respective parts of Integral 3, i. e. $\int X_\mathrm{A}(t)\mathrm{d}t$. As in section 4.2, it is necessary to distinguish between the analog sum signal $Y_\mathrm{A}(t)\mathrm{d}t$ (denoted by x*a in Fig. 17) and the integral of the analog input $\int X_\mathrm{A}(t)\mathrm{d}t$. $Y_\mathrm{A}(t)\mathrm{d}t$ can be represented by the instantaneous value of the contribution of $X_\mathrm{D}(t)$ (Integral 4) and the contribution $\Delta X_\mathrm{A}(\tau)$ being much larger than $\int X_\mathrm{A}(t)\mathrm{d}t$.

First, we compare the signal characteristics of the first integrator without overload estimation (OLE) with the one with OLE. The signal curves differ from $t = 8.5$ s on. At $t = 8.5$ s, Integral 3 (x1a_I3, dotted in green) falls below the threshold of 0.5, and the window comparator yields 0. The quantizer output v is positive, so at time $t = 9.5$ s the digital component x1d is decremented by 1. Since at time $t = 8.5$ s the window comparator output becomes 0, no continuous-time reset occurs, and x1a_I3 increases from 0.5 to just below 1.5 during a clock phase.

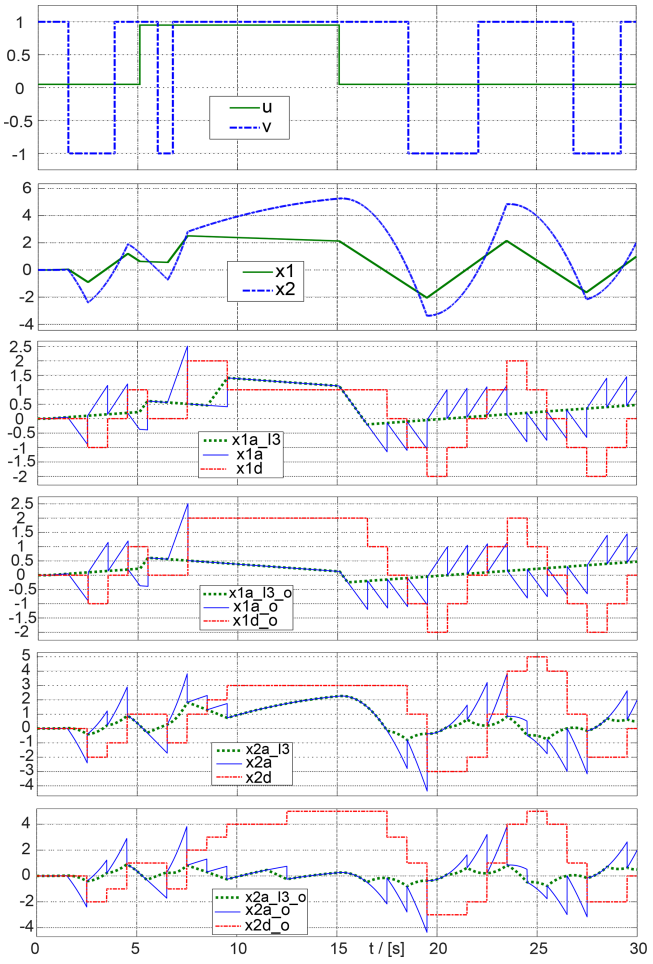

Figure 17. 2nd order CT $\Delta\Sigma$-Modulator under overload condition, using hybrid integrators, with and without overload estimation.

In contrast, for the hybrid integrator with OLE, the analog input $u = 0.95$ is multiplied by $G_{\mathrm{OLE}} = 0.5$ even after $t = 8.5$ s and added to Integral 3, the comparator threshold continues to be exceeded, and the Integral 3 continues to be subjected to a continuous-time reset until $t = 15.5$ s. Overload estimation keeps the analog Integral 3 below the threshold of 0.5.

The advantages of OLE are also evident in the second integrator: At $t = 6.5$ s, Integral 3 is just above the zero line, the window comparator in the hybrid integrator without OLE yields 0, so that at $t = 7.5$ s x2a_I3 increases to 2. In the integrator with OLE, the window comparator output is positive, so that at $t = 7.5$ s x2a_I3_o is still below 1. At $t = 11.5$ s, similar behavior can be seen: By OLE, the comparator is positive, the x2a_I3_o is reduced by time $t = 12.5$ s, and the digital part of the integral x2d_o reaches 4.

Due to the OLE, the analog integral of the 1st integrator can always be kept below 1 MU. Despite the peak values for the analog sum signal x1a_o for the first integrator, the analog Integral 3 (x2a_I3_o) of the second integrator is also kept under 1 MU.

At the output of the second integrator, the sum signal x2a_o and the digital output x2d_o must be evaluated together in the quantizer, which typically requires a suitable DA conversion of the digital value.

5 Conclusions

The new improved hybrid integrator with overload estimation is well suited for applications without negative feedback and for signals with steep transients and can therefore be used universally in analog computers, CT $\Delta\Sigma$ modulators, and analog control circuits.

A significant feature is that the digital component stored in the hybrid integrator does not have to be converted into an analog sawtooth voltage and fed to the analog output. Only the overflow of one bit corresponding to a machine unit (MU) that occurred in the hybrid integrator must be taken into account during a clock phase in the analog part, as well as the digital input to the hybrid integrator, of course. The reset of the analog component of the hybrid integrator is done continuously in time. During the reset process, an additive ramp signal is used to achieve a continuously correct value for the analog part of the hybrid integral. After the reset process, the ramp signal is switched off and the digital component is incremented. Disadvantages due to capacitive resets are thus avoided. Also, disadvantages due to asynchronous digital counters and the need for high-precision continuous-time comparators can be avoided in integration methods with integration direction reversal.

Due to the synchronous operation it is possible to use precisely clocked regenerative comparators, and because of the continuous-time reset a a precise representation of the total integral is possible. In contrast to this, of course, the overall circuit complexity must also be taken into account. In particular, this is relevant if the digital part of the analog integral has to be further processed in the analog computer, and thus the circuitry overhead and errors in the DA conversion have to be taken into account.

For overload estimation, the current analog input is added to the analog part of the integral with a weighting factor, so that in the case of dynamically changing signals or transients, the maximum magnitude of the analog integrator can be safely kept below one machine unit MU. However, the effectiveness of the overload estimation also depends on the specific signal waveform.

Through simulations of a harmonic oscillator, a damped spring-mass system, a spiking Neuron, and a CT $\Delta\Sigma$ modulator, it has been shown that scaling from the mathematical model to the real circuit with limited voltages is simplified, and the dynamic range can be extended almost arbitrarily by the hybrid representation of the integral.

Code availability. The Matlab models may be obtained by the authors and are subject to confidentiality.

Data availability. No data sets were used in this article.

Author contributions. DK developed the Matlab models. BU and SK contributed with applications, and contributed to review and editing this article.

Competing interests. At least one of the (co-)authors is a member of the editorial board of *Advances in Radio Science*. The peer-review process was guided by an independent editor, and the authors also have no other competing interests to declare.

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