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A 8X Oversampling Ratio, 14bit, 5-MSamples/s Cascade 3-1 Sigma-delta Modulator

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Abstract. A 14-b, 5-MHz output-rate cascaded 3-1 sigma-delta analog-to-digital converters (ADC) has been developed for broadband communication applications, and a novel 4th-order noise-shaping is obtained by using the proposed architecture. At a low oversampling ratio (OSR) of 8, the ADC achieves 91.5 dB signal-to-quantization ratio (SQNR), in contrast to 71.8 dB of traditional 2-1-1 cascaded sigma-delta ADC in 2.5-MHz bandwidth and over 80 dB signal-to-noise and distortion (SINAD) even under assumptions of awful circuit non-idealities and opamp non-linearity. The proposed architecture can potentially operates at much more high frequencies with scaled IC technology, to expand the analog-to-digital conversion rate for high-resolution applications.

1 Introduction

Continuing scaling of CMOS VLSI technology drives an exponentially increasing performance of digital signal processing, which drives shifting the analog-to-digital interface as close as possible to the front-end of the analog real world to eliminate some of the accurate and expensive traditional analog building blocks while offering the promise of high-integration and high-flexibility systems (Fujimori et al., 2000). In such systems, higher analog-to-digital conversion speed and resolution are endless desires, which should be fulfilled.

Sigma-delta ADCs have been applied to realize high-resolution signal conversion for broadband- communication applications. The stable single-loop high order structures have a low attenuation of quantization noises (Norsworthy et al., 1996). An alternative is to use unconditionally stable cascade multi-bit $\Sigma\Delta$ modulator (MASH) structure. But the suppression of quantization-noises of this type $\Sigma\Delta$ Modulators is decayed at high frequencies. Another problem associated with cascade $\Sigma\Delta$ modulators is high-performance integrator requirements to suppress quantization noise leakage (QNL) (Medeiro et al., 1999). In this paper a 3-1 cascaded sigma-delta ADC architecture for broadband-communication applications is presented, which combines merits of low-distortion single-loop, cascaded $\Sigma\Delta$ structures, high-order modified finite-impulse-response (FIR) NTFs architecture with multi-bit quantization.

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2 Proposed Cascade 3(4b)–1(5b) Low Distortion $\Sigma\Delta$ Modulator Architecture

The traditional theoretical signal-to-quantization noise ratio (SQNR) of **L**th-order high-pass can be increased by reducing the in-band quantization-noise power. It can be obtained by placing two complex-conjugate zeros of the NTF to replace two zeros at dc, which results in the high-pass NTF characteristic having a notch at high frequency f_0 within the signal band [0...f_{BW}]. For L≥2, the NTF can be expressed as :

$$NTF = \left(1 - z^{-1}\right)^{L-2} \left(1 - \delta z^{-1} + z^{-2}\right) , \quad (1)$$

where variable δ is equal to $2\cos(2(f_0/f_s))$ and f_s stands for sampling frequency. The notch frequency f_0 is optimized at approximately:

$$f_0 = \sqrt{(2L-3)(2L-1)} f_{BW} , \quad (2)$$

which improves the SQNR by a factor of $(L–0.5)^2$ compared to the case where all the zeros of the NTF are at DC (Hamoui et al., 2004).

The problem of this type sigma-delta modulator is that the employing numbers of multi-bit quantizer have to be very high to achieve reasonable input amplitude and the stability conditions as illustrated in Fig. 1; for the order higher than the third, the extreme high numbers of the quantization bits (over 5bits) require corresponding bits DACs, which resulting in more chip area, power consumption. The associated high-linearity DAC is also difficult to realize in the practice.

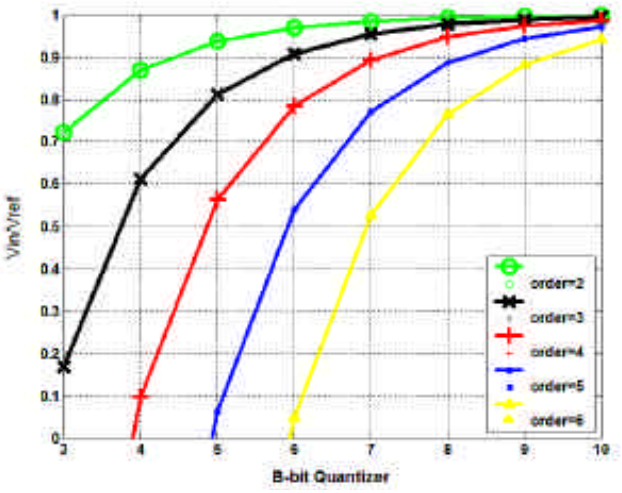

Fig. 1. Stable boundary under consideration of amplitude of input and the number of quantization bits for various orders.

Since the NTF improved FIR filter architecture has better high frequency in-band noise suppression due to the introduction of notch in the signal band, and the traditional cascaded $\Sigma\Delta$ modulator has better low frequency band noise suppression. Therefore, we obtain a new architecture by incorporate both $\Sigma\Delta$ modulators as shown in Fig. 2, where the first stage is realized by a 3rd-order NTF improved FIR structure and the second stage is a common first-order 5-bit modulator architecture.

The 3rd-order FIR NTF in Eq. (1) can be implemented by one additional feedforward path and one additional local feedback path imposed around the last two integrators in the loop filter thereby forming a resonator and, hence, requires very little analog circuitry. The modulator coefficients needed to realize the FIR NTF in Eq. (1) are determined by the parameter δ, where δ is chosen to be 1.9 to set the notch frequency at $0.8\,f_{BW}$.

The NTF of the proposed architecture can be expressed as:

$$NTF = \left(1 - z^{-1}\right)^2 \left(1 - \delta z^{-1} + z^{-2}\right) . \quad (3)$$

In the proposed modulator, a unity-gain signal transfer function (STF=1) was realized by adding the modulator's input signal to the quantizer's input (the dashed line), as shown in Fig. 2, without affecting the NTF. Consequently, only the quantization noise is processed in the integrators (Steensgaard et al., 1998). As a result, the architecture produces low harmonic distortion. Associated with multi-bit quantization which directly reduces the processed quantization errors in the loop-filter enhances modulator stability, relaxes slew-rate and settling requirements of the opamps of the integrators. Thus, it reduces the sensitivity to integrator non-idealities and, hence, helps minimizing the power dissipation.

Figure 3 shows the frequency responses of various types of NTFs. We can see, the 3rd-order modified FIR noise transfer function has a definite better noise suppression within almost entire bandwidth than 3rd-order feedforward inverse-Chebyshev FIR. Otherwise, it has also a better high frequency in-band noise suppression compared to the pure 3rd-order NTF. Consequently, it achieves the best entire in-band noise suppression. The additional cascaded stage of the proposed multi-bit cascade 3–1 $\Sigma\Delta$Modulator enhances the advantage of frequency response without concern of stability by employing 4bit quantizer in the first stage. As a result, the SQNR can be improved from the theoretical value of ca. 50 dB to over 60 dB. Thus, a 5bit quantizer was chosen in the second stage to obtain additional 30 dB.

The third-order multi-bit $\Sigma\Delta$ modulator in the first stage result in a further suppression of QNL as well as the DAC errors. The in-band error power for the proposed cascades 3-1 multi-bit $\Sigma\Delta$ modulator can be can be approximated to

$$P_{in-band} \approx \frac{\Delta_2^2}{12}\frac{\pi^8}{9M^9} + \frac{\Delta_1^2}{12}\left(\frac{4\pi^4}{5A_v^2M^5} + \varepsilon_1^2\frac{\pi^6}{7M^7}\right) + \sigma_{D1}^2 + \sigma_{D2}^2\frac{\pi^6}{7M^7} , \quad (4)$$

where Δ_1, Δ_2 represent the step between the two levels of the multi-bit quantizers in the first and second stages, respectively. The first term in Eq. (4) presents the suppression of theoretical quantization noise that is 4th-order shaped, the second term shows that the pole error is 2rd-order shaped, capacitor mismatching error source is 3th-order shaped, one order noise-shaping more than the cascade conventional 2-1-1 mb $\Sigma\Delta$ ADC. The use of 4-b quantizers in the first stage directly reduces their quantization noise, and hence further reduces QNL. As a result, the new modulator architecture significantly relaxes the requirements of high precision analog stages especially the requirement for of opamps with high dc-gain, which is more difficult to obtain as IC technologies advance, resulting in lower power supply voltages and shorter channel length devices.

Consider that the DAC-induced error power σ_{D2}^2 in the second stage will have 3rd- order shaped as expressed in the fourth term of Eq. (4), therefore, the DAC errors in the multi-bit second stage can be neglected in the noise budget. But that in the first stage has to be considered. Therefore DEM technique is incorporated in the multi-bit first stage to improve the modulator linearity.

3 Simulation Results

We simulated the proposed cascade 3(4b)–1(5b) low-distortion $\Sigma\Delta$ Modulator shown in Fig. 2 in Matlab in three cases to compare with traditional cascade 211(5 mb) $\Sigma\Delta$ modulator: ideal case, with 2% gain errors and pole errors, and with opamp nonlinearity effects. In these simulations, a sine-wave signal with an amplitude -6 dBFS was applied, the sample frequency was 40 MHz for a 2.5 MHz input signal, as well as the multi-bit DAC was assumed to be ideal.

The spectra by using both architectures in the ideal case are shown in Fig. 4, where only quantization errors are considered. The proposed architecture presents much higher attenuation at the in-band high-frequencies. The SQNR of

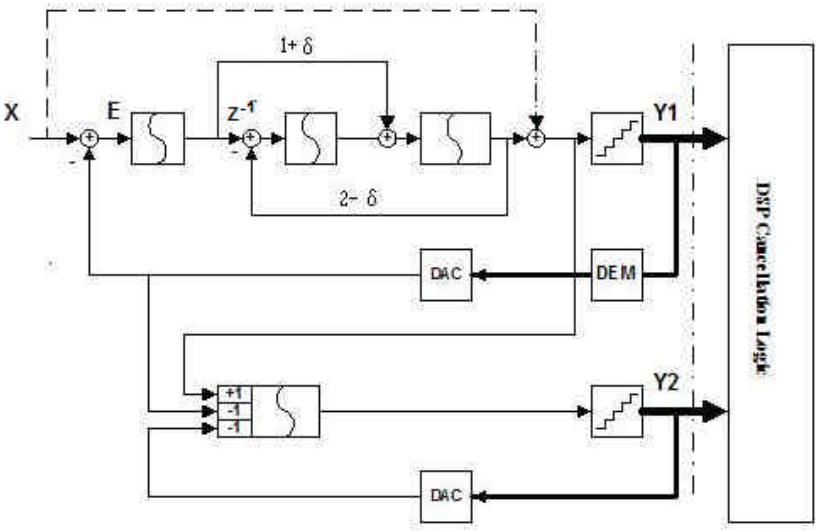

Fig. 2. Proposed 4th-order cascade 3(4b)–1(5b) ΣΔ Modulator.

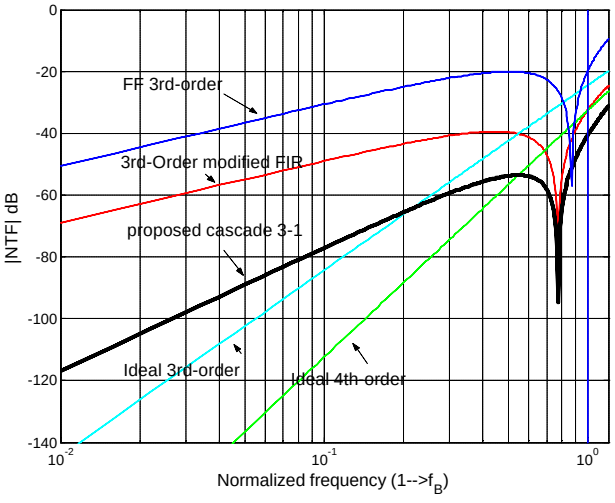

Fig. 3. The magnitude responses of the 3rd , 4th-order NTFs with various type.

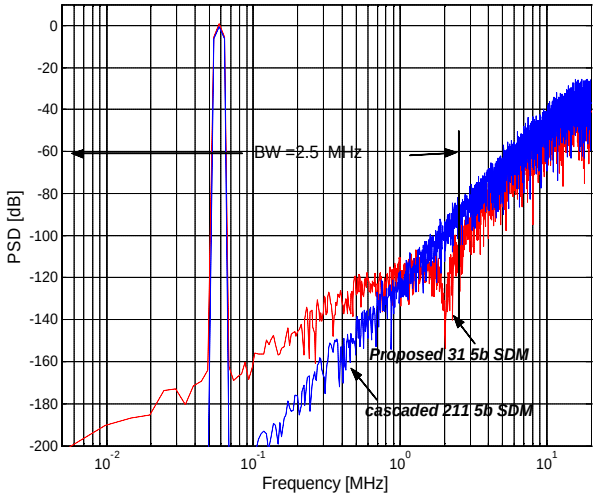

Fig. 4. The ideal output spectra of ΣΔ modulators.

the proposed sigma-delta modulator is 89.5 dB, in contrast to 71.8 dB of cascade 211 (5bit) structures. This proposed technique appears particularly effective for broadband applications.

Figure 5 shows the spectra of both architectures with 2% gain errors and pole errors. We can observe, that our proposed architecture maintains high performance even with great deviation of integrator gain factor in comparison with traditional cascade ΣΔ modulator. It indicates that the proposed sigma-delta modulator architecture does not require high opamp dc-gain and high capacitor matching as the traditional cascade one.

The spectra in Fig. 6 illustrate the non-linearity effect on proposed one and the traditional one, where the maximum dc-gain is 40 dB, 60 dB, respectively, as well as, the pamp gain varied from about half of maximum dc-gain to maximum dc-gain according to hyperbolic tangentfunction. As expected, the proposed modulator does not produce detectable harmonic distortion. Note that the simulation shows an increased noise floor. Part of this is caused by finite opamp gain. The other part is caused by the nonlinearities, which fold energy from high-frequencies down into the signal band. However, due to the absence of signal components, the proposed topology has a better noise floor.

A further simulation was performed for proposed architecture, where incorporated added common non-idealities in switched-capacitor circuits on proposed modulator, such as switched-capacitor KT/C noise, finite bandwidth and slew-rate of the opamps. Figure 7 shows the simulated spectrum,

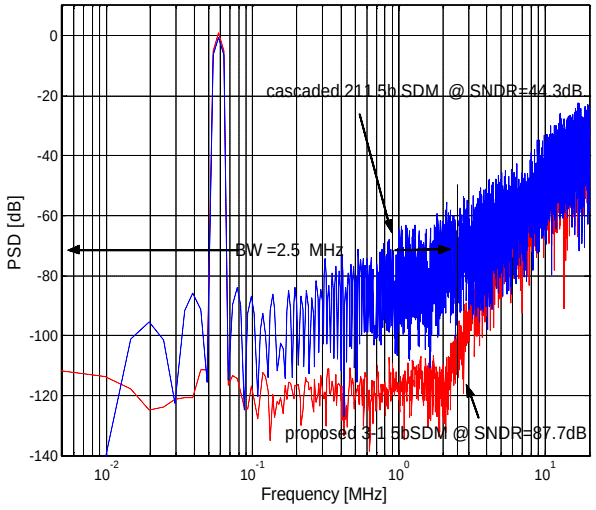

Fig. 5. The output spectra of ΣΔ modulators with 2% coefficient variation.

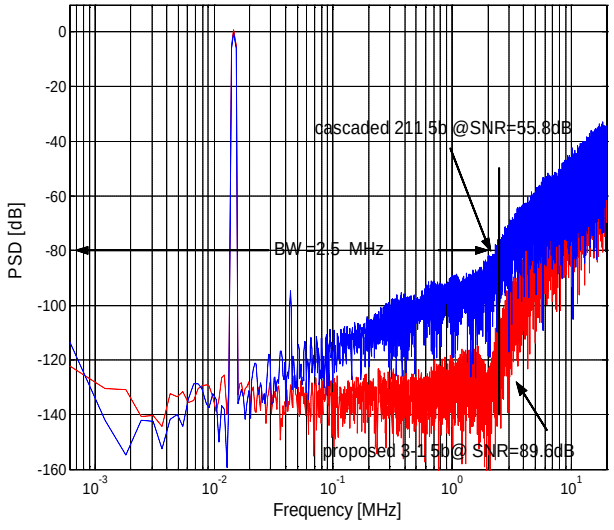

Fig. 6. The output spectra of ΣΔ modulators with non-linearity.

where we applied an opamp dc-gain of 40 dB with nonlinearity as previous simulation, a sampling capacitor of 6 pF, as well as a 100 V/us slew-rate of and 100MHz GBW of the first opamp. The spetrum presents a raised but still satisfied noise floor and still no obviously introduced harmonics or tones.

4 Summary and Conclusion

In this paper, a 14-b, 5-MHz output-rate 4th sigma-delta ADC architecture was proposed for high-speed high-resolution broadband applications. Firstly, it realized a stable 4th-order NTF improved architecture with very little additional circuitry. By using this architecture, the theoretical SQNR is improved about 10 dB at low OSR 8, and over

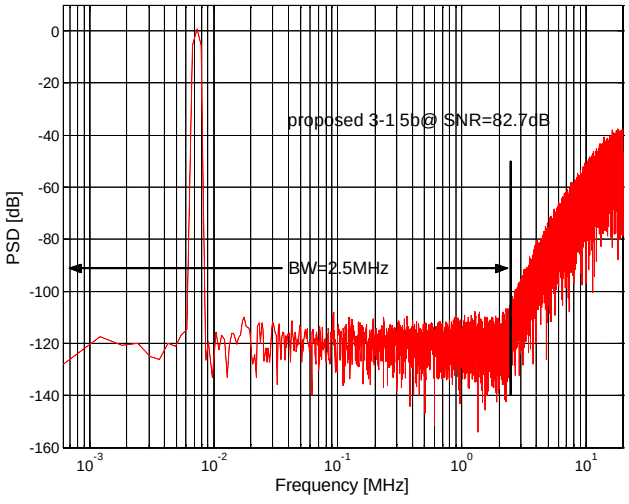

Fig. 7. The output spectra of proposed ΣΔ modulator with non-idealities.

20 dB in comparison with traditional architecture. Secondly, the QNL caused by finite dc-gain of opamps and capacitor mismatching can be suppressed by using multi-bit quantizer and one order more noise-shaping in the first stage. Finally, the non-linearities, such as opamps non-linearity, as well as circuit non-idealities are obviously sustainable in the proposed architecture, since the integrators process only low-power quantization noise only. Hence, the circuit requirements can be significantly relaxed; the power dissipation can be low. It is particularly suitable for realizing low-power wide-bandwidth ADCs in scaled IC technologies.

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