Design of a LNA in the frequency band 1.8–2.2 GHz in 0.13 μm CMOS Technology

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Abstract. The subject of this work is a low noise amplifier (LNA), operating in the frequency range 1.8–2.1 GHz. The CMOS 0.13 μm technology is used in respect to the low cost of the final device. Among the specifications, a variable gain and an adjustable working frequency are required. In particular, four different working modes are provided: 1.8, 1.9 and 2.1 GHz high gain and 2.1 GHz low gain. The amplifier is designed to be used as first stage of a receiver for mobile telephony. For this reason low power consumption is taken into consideration (low supply voltage and low drain currents). A simple digital circuit, integrated on-chip, is used to select the operating mode of the LNA by means of two input pins. A Noise figure of 1 dB is obtained with a supply voltage of 0.8 V.

1 Introduction

With the recent introduction of the new mobile telephony standard UMTS the market is pushing toward receiver solutions that are compatible with the traditional standard GSM900/1800 as well as with the new one. Towards excellent noise performance, high linearity and low power consumption, the possibility to change the operating frequency of the RF part of the receiver with a minimum amount of component is required. Among many examples in the literature, we can distinguish LNA solutions that make use of the HEMT-HBT GaAs (Kobayashi, 1996), the Si Bipolar (Adiseno, 2002), the SiGe BiCMOS (Ryynänen, 2003), (He, 2004) and the standard CMOS technlogy. While the GaAs semiconductor is relegated to the very high frequency field because of the high costs the bipolar and BiCMOS technologies are today still very popular. Thanks to the considerable progress in the miniaturization of the standard CMOS, sustained by the digital market, and to the consequent cost reduction is now CMOS the most promising technology for the forthcoming RF applications. A fully standard CMOS 0.13-μm process with six metal layers was empolyed in this work. Since the reduction of the supply voltage, in order to

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allow longer battery endurance on portable devices, will be a great challenge a low supply voltage of 0.8 V was used.

2 Circuit Design

The LNA operates in a receiving chain and must be preceded by a pre-select filter. This filter needs, in order to work properly, a fixed value of the input impedance of the amplifier. Moreover it works in differential mode, indicating that the LNA must use a differential topology as well. In our case a value of 200 Ω is required for the differential input impedance.

2.1 Input Matching

Two possible architectures where examined in order to find the best solution to adapt the circuit to the source, like shown in Fig. 1. The aim was namely the achievement of a very good matching to 200 Ω differential ($S_{11} \leq$ -15 dB) for every frequency mode with the same external matching network. Furthermore this network is required to be very simple and to use standard passive components. The first one (Fig. 1A) is the classic common source transistor with source degeneration inductor (Karanicolas, 1996), (Gatta, 2001): this topology gives approximately the following input impedance:

$$Z_{in} = \frac{g_{m1}L_s}{C_{gs}} + sL_s + \frac{1}{sC_{gs}},\qquad(1)$$

where g_{m1} is the transconductance of the transistor, C_{gs} its gate-source capacitance and L_s the degenerating inductor. It was decided not to use this structure because of some drawbacks: the high chip area requirement (inductor) and the poor stability, caused by the parasitic capacitance between source of the input MOSFET and bulk. At last its intrinsic narrowband behaviour caused by a good input matching only in a narrow frequency range dissuaded us to use this topology. The structure that was chosen is a common-source with feedback resistor between output node (drain) and input (gate) (Fig. 1B). The resistor modifies the input impedance of the
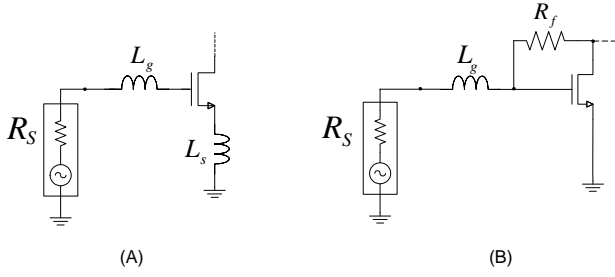
(A)   (B)

Fig. 1. Basic architectures. **(A)** Source Degeneration, **(B)** Feedback Resistor

circuit, that is initially mere capacitive, producing a resistive term. This is given in an approximated form by:

$$Z_{in} = \frac{R_f + Z_L}{1 + g_{m1}Z_L + sC_{gs}(R_f + Z_L)}, \tag{2}$$

where R_f is the feedback resistor and Z_L the load impedance. This topology was further improved by mean of a Cascode configuration that has only a small impact on the input impedance, compared to the simple common source transistor. This structure improves the reverse isolation because of the buffer function of the common gate MOSFET. This leads, together with the feedback resistor that performs a negative feedback, to a higher stability.

2.2 Load

In order to minimize the noise of the amplifier resistive loads were avoided: the load comprises a resonating LC-parallel tank. This enables very low supply voltages because of the negligible voltage DC-drop across the on-chip inductor. The high equivalent resistance at the resonance together with the high output resistance of the Cascode allows a considerable voltage gain. Furthermore the LC-load exhibits a bandpass behaviour, which helps to suppress out-of-band interferers. Since the inductor was integrated, simulations were conducted with an Infineon in-house tool, based on the FastHenry/FastCap simulator, in order to take into account all parasitic effects (Kehrer, 2001). An octagonal form was chosen and the inner resistance of the windings was minimized by mean of stacked metal layers, shorted by vias. The capacitance to the bulk was reduced by using the three upper metal layers. In Fig. 2 is depicted the equivalent circuit diagram of the inductor that was used in the simulations.

2.3 Noise

The main source of noise in this circuit is caused by the thermal channel noise of the input transistor. This can be schematized by a current generator between drain and source, which is given by Shaeffer (1997):

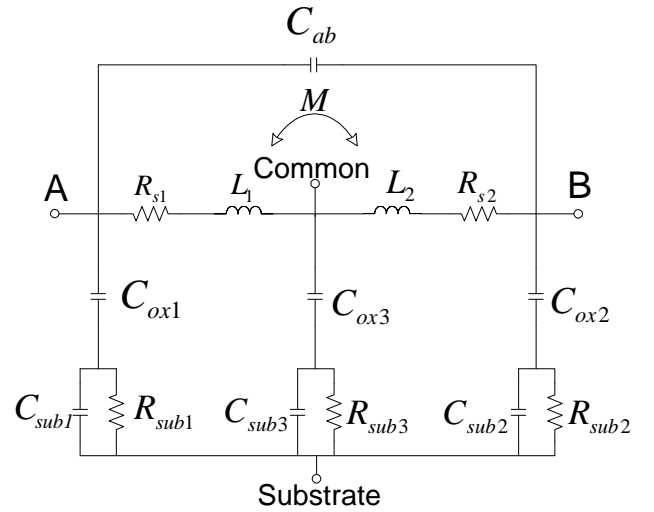$$\overline{i_{nd}^2} = 4kT\gamma g_{d0}\Delta f, \tag{3}$$

Fig. 2. Equivalent curcuit of the integrated inductor.

where K is the Boltzmann's constant, T is the absolute temperature, γ is a bias-dependent factor and g_{d0} is the zero-bias drain conductance of the FET. If we assume $g_{d0} \simeq g_m$ that is the transconductance of the input FET and $\gamma \simeq 2/3$ we obtain:

$$\overline{i_{nd}^2} = \frac{8}{3}kTg_m\Delta f. \tag{4}$$

Since the feedback resistor has a great value (more than 1.5 KΩ) it gives a negligible noise contribution. In addition it does not sensibly modify the overall gain of the amplifier (weak feedback). Therefore we will estimate the noise factor considering the feedback resistor as infinite. Thus the total noise voltage at the output is, considering also the thermal noise of the source resistance R_s:

$$\overline{V_{n,out}^2} = (4KTR_sA_v^2 + \overline{i_{nd}^2}R_p^2)\Delta f, \tag{5}$$

where

$$A_v = g_{m1}R_{OUT}Q_{in} \tag{6}$$

is the approximated voltage gain. Q_{in} and R_{out} are the quality factor of the input mesh when the amplifier is adapted to the source R_s and the output resistance respectively. They are defined as follows:

$$Q_{in} = \frac{1}{2R_s\omega C_{gs}} \tag{7}$$

and

$$R_{OUT} = R_P//R_{CASC}. \tag{8}$$

Hence, the output resistance of the amplifier, neglecting the feedback resistance, is given by the parallel between the output resistance of the Cascode, R_{casc} and the equivalent resistance R_P of the load at the resonance. The first can be
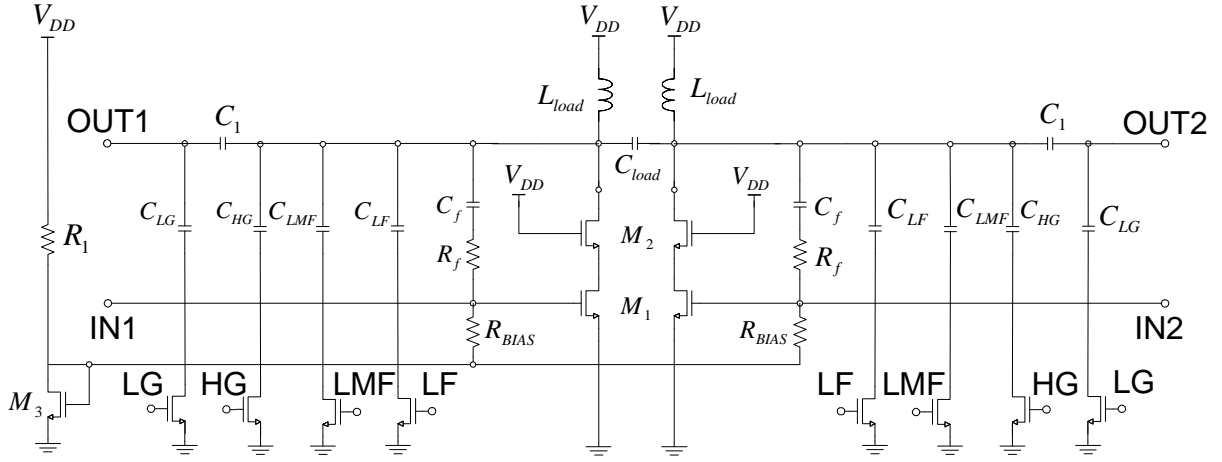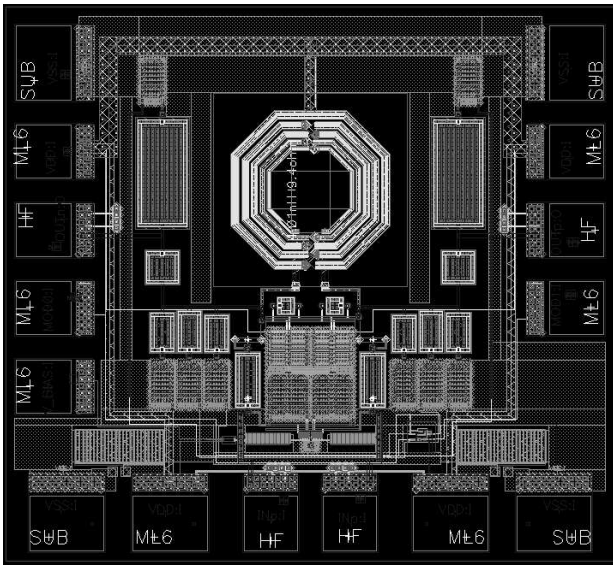
Fig. 3. Complete Schematic.
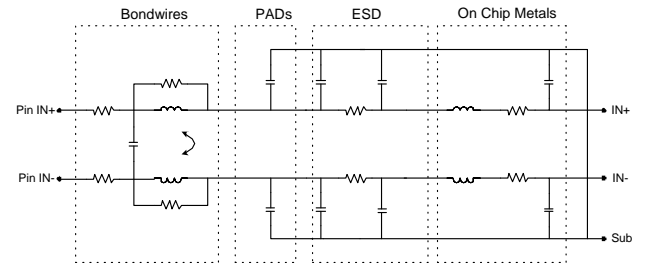

Fig. 4. LNA layout.

Fig. 5. Equivalent circuit of the pads/pins parasitics.

factor. The noise factor is therefore, replacing the value of the output resistance:

$$F = \frac{V_{n,out}^2}{4kT\,R_S A_v^2 \Delta f} = \frac{4kT\,R_s A_v^2 + \frac{8}{3}KT g_{m1} R_{OUT}^2}{4kT\,R_s A_v^2} =$$

$$= 1 + \frac{\frac{8}{3}KT g_{m1} R_{OUT}^2}{4kT\,R_s g_{m1}^2 Q_{in}^2 R_{OUT}^2} = 1 + \frac{2}{3R_s g_{m1} Q_{in}^2} . \quad (12)$$

This result suggests that the noise factor tends to a null value for decreasing Q_{in}, that is for decreasing C_{gs}, thus for smaller input transistors. Otherwise the SPICE model 2 noise simulations show the presence of a minimum noise factor for a precise size of the input MOSFET. This could be explained by mean of the inversion layer resistance:

$$R_{inv} \simeq \frac{1}{5g_m} . \quad (13)$$

The V_{gs} will be now:

$$V_{gs} = Q_{eff} V_{in} , \quad (14)$$

where Q_{eff} is an "effective" Q_{in} that includes the effect of R_{inv} and could be so defined:

$$Q_{eff} = \frac{1}{\omega_0 C_{gs}(2R_s + R_{inv})} . \quad (15)$$

simply obtained by mean of the small signal equivalent circuit. Approximately we have:

$$R_{CASC} \simeq g_{m2} r_{02} r_{01} . \quad (9)$$

Moreover, the load at the resonance exhibits the following parallel resistance:

$$R_p = R_{ser}(Q_{out}^2 + 1) \quad (10)$$

with

$$Q_{out} = \frac{\omega_0 L_{load}}{R_{ser}} , \quad (11)$$

where R_{ser} is the parasitic series resistance of the integrated inductor, L_{load} the inductance of the load and Q_{out} its quality
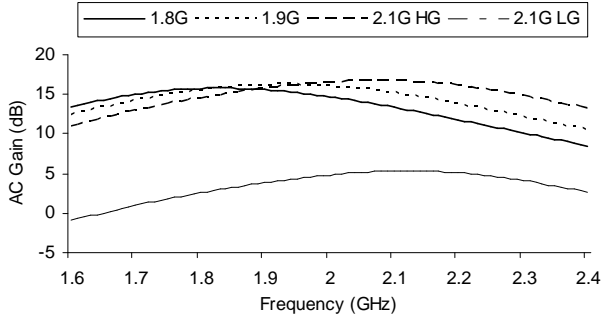
Fig. 6. AC Gain Simulation results.
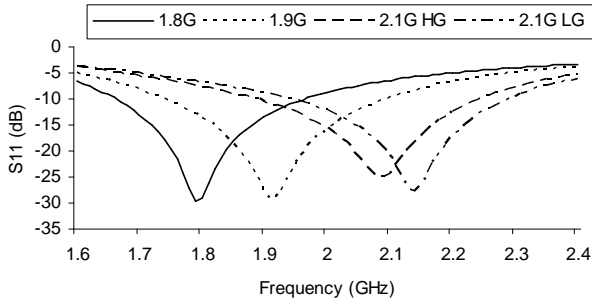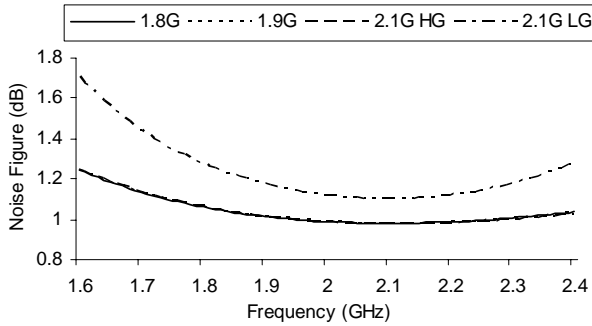

Fig. 7. S_{11} Simulation results.

Fig. 8. Noise Figure simulation results.

This quantity tends to a constant value for W small enough, since C_{gs} is proportional to W and the inversion layer resistance is inversely proportional to the same quantity. The inversion layer resistance can be represented as a resistor in series with C_{gs} whose noise contribution must be taken into account. Replacing Eq. (15) in (12) and adding the thermal noise of R_{inv} we obtain:

$$F = 1 + \frac{R_{inv}}{R_s} + \frac{2}{3 R_s g_{m1} Q_{eff}^2} \,. \tag{16}$$

For $W \rightarrow 0$, the last term in Eq. (16) is inversely proportional to g_{m1} since Q_{eff} remains constant. Moreover the

Table 1. Gain Simulation Results.

MODE	AC Gain	Max Gain Freq.	B_{-1dB} GHz
1.8 GHz High Gain	15.75 dB	1.83 GHz	$1.68 - 1.99$
1.9 GHz High Gain	16.15 dB	1.93 GHz	$1.77 - 2.10$
2.1 GHz High Gain	16.68 dB	2.07 GHz	$1.90 - 2.23$
2.1 GHz Low Gain	5.32 dB	2.12 GHz	$1.95 - 2.28$

Table 2. S_{11} Simulation Results.

MODE	$S_{11,MIN}$	$S_{11,MIN}$ Freq.	$S_{11} < 10$ dB
1.8 GHz HG	-28.92 dB	1.79 GHz	$1.67 - 1.96$ GHz
1.9 GHz HG	-28.00 dB	1.91 GHz	$1.74 - 2.09$ GHz
2.1 GHz HG	-24.28 dB	2.09 GHz	$1.89 - 2.24$ GHz
2.1 GHz LG	-21.27 dB	2.14 GHz	$1.95 - 2.29$ GHz

Table 3. Linearity and Noise Figure Simulation Results.

MODE	IIP_3	iCP_1	NF
1.8 GHz High Gain	-5.54 dBm	-17.76 dBm	1.06 dB
1.9 GHz High Gain	-5.31 dBm	-18.06 dBm	1.01 dB
2.1 GHz High Gain	-5.94 dBm	-18.47 dBm	0.98 dB
2.1 GHz Low Gain	-7.35 dBm	-19.74 dBm	1.10 dB

term in the middle is proportional to R_{inv}. That means that the Noise Factor will begin to increase again for a definite W and implies the presence of a minimum. The input transistor width was chosen in correspondence to this minimum, that lays at about 500 μm.

2.4 Linearity

Once we set the bias currents of the FETs we analyze the linearity of the amplifier in dependence on the width of the input transistors W_{in}. Increasing W_{in} we observe two opposite effects: on the one hand the overdrive voltage $V_{GS} - V_T$ decreases, worsening the linearity since we have a direct proportionality between the input IP3 and the biasing overdrive voltage (Lee, 1998). On the other hand a wider input FET means a decrease of the input Q (7), because of the increasing gate-source capacitance. This implies that V_{gs}, equal to $Q_{in}V_{in}$, decrease as well, so improving the linearity by preventing the amplifier to saturate. It can be shown that in a narrowband architecture, like this LNA, the input $IP3$ is proportional to $1/Q_{in}^2$ (Lee, 1998). It was found that the dependence on the quality factor of the input mesh dominates, indicating a better linearity when using a wider input FET.

2.5 Multi-gain and Multi-frequency Mode

The multi-gain capability is realized by mean of a switchable capacitive divider ($C_1 - C_{LG}$ in Fig. 3). When inserted

the AC output signal is attenuated, thus the gain is reduced of about 10 dB. This solution does not improve the intrinsic linearity of the amplifier; anyway it is convenient, because a reduced amplitude of the output signal indicates an improved linearity of the incoming stage (i.e. mixer). Similarly the multi-frequency function is implemented via switchable capacitors that vary the resonance frequency of the LC-load. Since the equivalent resistance of the resonating load varies in a marginal range and because of its great influence onto the input impedance of the amplifier, this solution is appropriate in order to get a good matching in all operating modes.

3　Layout and Simulation Results

The complete schematic is represented in Fig. 3. A small digital logic circuit was added in order to switch on/off the capacitors thus varying the operating mode that is chosen via two external pins. Figure 4 shows the layout of the circuit, whose area is $0.44\,\mu$m^2, including the pads. Particular attention was paid into reducing the parasitic resistance of the metal interconnections to minimize the noise. ESD-protection consisting in integrated bulk/n-well diodes between input/output and VDD/ground respectively were used and considered in the simulations. Their parasitic capacitance, together with that of the pads and the other parasitics of the bondwires, has a severe impact on the input impedance of the LNA. For this reason their effect was modelled with an equivalent circuit (Fig. 5). To cope with this problem an external compensating network was needed: it consist of an inductor of 10 nH in parallel to the inputs together with two capacitors (2.2 pF) in series. These components' values are compliant with the standard E12 and easily obtainable. The external network used is the same for every operating mode of the LNA. Figures 6, 7 and 8 show the simulated gain, noise figure and input matching in every operating mode. The Gain, S_{11} and Noise Figure results are resumed in Table 1, Table 2 and Table 3 respectively. In Table 3 the linearity simulation results are depicted as well, namely the input IP3 and the input referred Compression Point. The linearity simulations were performed with a two tone test: the first tone at the frequency related to the operating mode, i.e. 1.8, 1.9 and 2.1 GHz, the second at a frequency distance of 10 MHz.

4　Conclusions

An LNA with variable gain and operating frequency band was designed. A cascode topology with feedback resistance was used thanks to its good compromise between noise and stability. The total current consumption is about 9 mA with a supply voltage of 0.8 V for a total of 7.2 mW of dissipated power. The noise was minimized by mean of a high-Q input mesh, obtained with reactive (noiseless) components and maximizing the gain: a 1-dB NF in every high gain mode was obtained. Due to its advantages like the band pass behavior, the low added noise and the high gain at the resonance frequency, the LC resonating load is the most appropriate solution. An important achievement is the good input matching, at every considered frequency range, with the same external adapting network, that allows a sensible cost reduction of the final receiver.

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