Noise Considerations of Integrators for Current Readout Circuits

B. Bechen, A. Kemna, M. Gnade, T. v. d. Boom, and B. Hosticka

Fraunhofer Institute of Microelectronic Circuits and Systems, Duisburg, Germany

Abstract. In this paper the noise analysis of a current integrator is carried out and measures to reduce the overall noise are presented. The effects of various noise sources are investigated and their dependence on the input capacitance and on the gate area of the input transistors of the OTA used for the readout is shown. Both, input capacitance and gate area, should be kept as small as possible. Moreover, the linearity of the integrator is examined. In addition to that, the available application of such sensor readout circuit, which is a CMOS photodetector readout, is introduced. It uses an automatic gain switching, so that the dynamic range is extended.

1 Introduction

For various special applications in industrial measuring techniques sensor readout circuits are required. In the available consideration the current readout, particularly of a CMOS photodetector, is examined. An advantage of CMOS technology is the possibility to integrate sensor readout and photodetector together on a single chip. The pixels, consisting of photodiode and readout electronics, are arranged in an array, which enables an optional random access to each pixel. Before investigating such pixels, a general integrator is investigated in Sects. 2 and 3. As shown in Fig. 1 the integrator is realized with an operational transconductance amplifier (OTA), which has a capacitive feedback. This integrator converts the current of the current source, particularly of the photodiode, into an output voltage. In Sect. 4 a method to reduce the requirements on the OTA is presented.

2 Noise analysis

In the following section the noise behaviour of a feedback integrator as a current-to-voltage converter is investigated (see Fig. 1). The noise equivalent circuit diagram is shown in Fig. 2. Noise sources are grey-shaded. Here $\sqrt{i_{n1}^2}$ represents

Correspondence to: B. Bechen (benjamin.bechen@ims.fraunhofer.de)

the shot noise of the current source, $\sqrt{\overline{u_{n2}^2}}$ in each case the thermal noise of the switches and $\sqrt{\overline{u_{n3}^2}}$ is the input-referred OTA noise.

 $C_{\rm E}$ is the total input capacitance, which is the sum of all capacitances at the OTA input node. It is mainly determined by the gate area capacitance of the OTA input transistors and, of course, by the current source capacitance. The single-ended OTA is modelled by the transconductance $g_{\rm m}$, the output conductance $g_{\rm L}$, and the load capacitance $C_{\rm L}$.

As can be seen, the operation is separated in the two switched capacitor operation phases, i.e. the reset phase and the integration phase.

2.1 Reset phase

During the reset phase the integrator output is short-circuited via the reset switch with its series resistance $R_{S,R}$ to its inverting input. By using transfer functions $H_{e,i}(f)$ from the noise sources to the input node, the noise power can be calculated as

$$P_{e,res,i} = \int_{0}^{\infty} |H_{e,i}(f)|^2 \cdot W_i(f) df$$
 (1)

with i as an index for the different types of noise sources. W_i are the different spectral noise densities, which can be defined as

$$W_{iph}=2 \cdot e \cdot I_{in}$$
 (2)

for the shot noise of the current source,

$$W_{s,th} = 4 \cdot k \cdot T \cdot R_{S,R} \tag{3}$$

for the thermal noise of the reset switch,

$$W_{O,th} = \frac{16}{3} \cdot \frac{k \cdot T}{g_m} \tag{4}$$

for the thermal noise of the OTA and

$$W_{O,1/f} = \frac{2 \cdot K_f}{C_{ox} \cdot f} \tag{5}$$

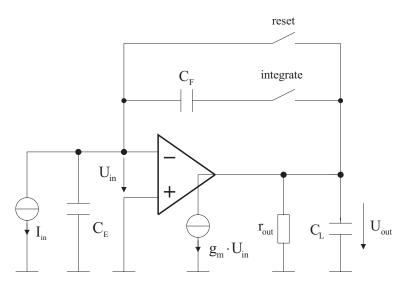


Fig. 1. Principle of the current integrator.

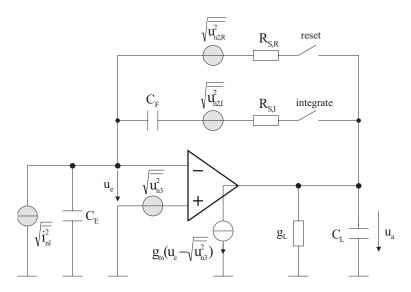


Fig. 2. Noise equivalent circuit diagram of the integrator.

for the 1/f-noise of the OTA. Together with Kirchhoff's rules the noise transfer functions of the single noise contributions can be described as follows:

$$\begin{split} H_{el}(\omega) &= \frac{u_e}{\sqrt{i_{nl}^2}} \\ &\frac{1 + R_{S,R}g_L + R_{S,R}j\omega C_L}{g_m + g_L + j\omega(C_L + C_E) + R_{S,R}j\omega C_E(g_L + j\omega C_L)} \end{split} \tag{6}$$

for the transfer function of the noise current source to the input node,

$$\begin{split} &H_{e2}(\omega) = \frac{u_e}{\sqrt{u_{n2,R}^2}} \\ &= \frac{-g_L - j\omega C_L}{g_m + g_L + R_{S,R} g_L j\omega C_E + j\omega (C_L + C_E) - \omega^2 C_L C_E R_{S,R}} \end{split} \tag{7}$$

for the transfer function of the reset switch noise source to the input node and

$$\begin{split} H_{e3}(\omega) &= \frac{u_e}{\sqrt{u_{n3}^2}} \\ &= \frac{g_m}{g_m + g_L + R_{S,R} g_L j \omega C_E + j \omega (C_L + C_E) - \omega^2 C_L C_E R_{S,R}} \end{split} \tag{8}$$

for the input-referred OTA noise to the input node.

In the following integration phase the input referred noise is transferred to the output by the following equation:

$$P_{a,res,i} = \left(\frac{C_E}{C_F}\right)^2 \cdot P_{e,res,i} . \tag{9}$$

2.2 Integration phase

During the integration phase the integration capacitor C_F is switched into the feedback path by the integration switch with its series resistance $R_{S,I}$. The noise equivalent circuit is still shown in Fig. 2. In difference to the reset phase, the noise is calculated in the integration phase as referred to the output. Similarly, the transfer functions have to be determined:

$$H_{al}(\omega) = \frac{u_a}{\sqrt{\frac{1}{i_{nl}^2}}} = \frac{(g_m + j\omega C_E)(1 + j\omega C_F R_{S,I}) - [j\omega C_F + j\omega C_E(1 + j\omega C_F R_{S,I})]}{(g_L + j\omega C_L)[j\omega C_F + j\omega C_E(1 + j\omega C_F R_{S,I})] + j\omega C_F(g_m + j\omega C_E)}$$
(10)

for the transfer function of the noise current source to the output node,

$$H_{a2}(\omega) = \frac{u_a}{\sqrt{u_{n2.I}^2}} = \frac{g_m C_F + j\omega C_F C_E}{g_L C_E + g_m C_F + g_L C_F + j\omega (C_F C_E R_{S,I} g_L + C_L C_E + C_E C_F + C_L C_F) - \omega^2 C_L C_F C_E R_{S,I}}$$
(11)

for the transfer function of the integration switch noise source to the output node and

$$H_{a3}(\omega) = \frac{u_a}{\sqrt{u_{n3}^2}} = \frac{g_m C_F + g_m C_E + j\omega C_F C_E R_{S,I} g_m}{g_L C_E + g_m C_F + g_L C_F + j\omega (C_F C_E R_{S,I} g_L + C_L C_E + C_E C_F + C_L C_F) - \omega^2 C_L C_F C_E R_{S,I}}$$
(12)

for the input-referred OTA noise to the output node. Thus the noise of the integration phase $P_{a,int}$ and the total noise power can be calculated:

$$P_{tot} = \sum P_i = \sum \left(P_{a,int,i} + \left(\frac{C_E}{C_F} \right)^2 \cdot P_{e,res,i} \right)$$
 (13)

2.3 Results of noise analysis

Although the circuit under investigation is a sampled-data circuit we can still use a continuous-time noise analysis if we take into account that all undersampled noise is aliased. Thus we find all noise in the baseband.

A noise analysis that involves a detailed evaluation of Eqs. (1–13) is quite tedious. In order to simplify the analysis we assume that following approximations hold: $g_m \gg g_L$, $R_{S,R} \cdot g_L \ll 1$, $R_{S,I} \cdot g_L \ll 1$, $\omega \cdot R_{S,R} \cdot C_L \ll 1$ and $\omega \cdot R_{S,I} \cdot C_L \ll 1$. These are valid for high open-loop gain of the OTA and low ON-resistance of the switches, respectively. It is interesting to note that then the signal bandwidth (and, hence, the noise bandwidth) is dictated mainly by the product $g_m/(C_L + C_E)$ in the reset phase and by $g_m/\left[C_E + C_L \cdot (1 + C_E/C_F)\right]$ in the integration phase. Increasing C_E to lower the bandwidth is not recommended, since it introduces a zero in two of the noise transfer functions (see Eqs. (11) and (12)) and, also, it raises the DC gain of the OTA noise transfer function to the

output (see Eq. (12)). Hence the most important measure to reduce the readout noise is to reduce the integrator bandwidth

$$BW = \frac{g_L}{2 \cdot \pi \cdot C_L} \tag{14}$$

by keeping C_L as large as possible. Unfortunately the bandwidth limitation due to C_L affects the slew rate and the available output current of the OTA. This analysis shows that the input capacitance C_E has the most deleterious effect on the noise performance of the integrator. This has been corroborated by simulations, as shown in Fig. 3.

It can be seen that the input capacitance C_E has to be realized as small as possible to minimize the noise. For the available application (photodetector readout), a reduced capacitance of the photodiode is presented in Kemna (2003) by using a dot diode. It must be noted that the dark current also has to be reduced to ensure maximum signal resolution.

In single stage amplifier designs, the OTA performance is mainly determined by the MOS transistors of the input stage (Uhlemann, 1994). According to that, noise powers are plotted in Fig. 4 in dependence of the gate area of the input transistors. An increase in the gate area would reduce the 1/f noise, but the 1/f noise of the OTA contributes only very little to the overall noise. Hence the gate area should be chosen small.

3 Linearity of the integrator

A Laplace transformation of the transfer function of a simple current integrator, yields

$$\frac{U_{\text{out}}(s)}{I_{\text{in}}(s)} = \frac{A_0 \left(1 - \frac{sC_F}{g_{\text{m}}}\right)}{s\{[C_F(A_0 + 1) + C_E] + sr_{\text{out}}(C_L C_E + C_L C_F + C_F C_E)\}} = \frac{A_0 \left(1 - \frac{s}{z}\right)}{\frac{s}{p_1} \left(1 + \frac{s}{p_2}\right)}$$
(15)

with the open loop gain $A_0=g_m \cdot r_{out}$. The abbreviations z, p_1 and p_2 are defined as

$$z = \frac{g_m}{C_F}, \qquad p_1 = \frac{1}{(A_0 + 1) \cdot C_F + C_E}, \qquad p_2 = \frac{(A_0 + 1) \cdot C_F + C_E}{r_{out} \cdot (C_L \cdot C_E + C_L \cdot C_F + C_F \cdot C_E)}$$
 (16)

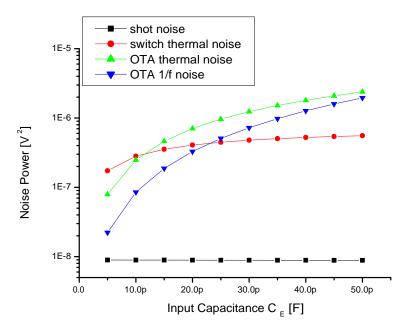


Fig. 3. Noise power of the integrator stage versus the input capacitance.

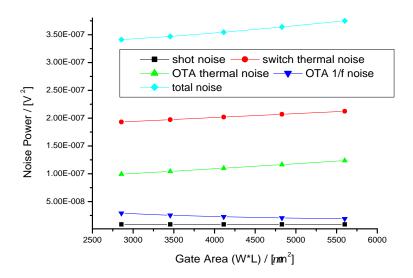


Fig. 4. Noise power of the integrator stage versus gate area of the input transistors.

Transforming it back and assuming the current is a step function, results in an output voltage as follows:

$$u_{out}(t) \hspace{-0.1cm}= \hspace{-0.1cm} I_{in0} \cdot \left\{ A_0 \cdot p_1 \cdot \left[t \hspace{-0.1cm} - \hspace{-0.1cm} \frac{(1 + \frac{p_2}{z})}{p_2} \cdot \left(1 \hspace{-0.1cm} - \hspace{-0.1cm} e^{-p_2 \cdot t} \right) \right] \right\}. \quad (17)$$

After one integration period T, the integral nonlinearity can be calculated as

INL=
$$\frac{\left(1 + \frac{p_2}{z}\right) \cdot \left(1 - e^{-p_2 \cdot T}\right)}{p_2 \cdot T}$$
. (18)

In Fig. 5 the nonlinearity INL is plotted over the integration time T. The limit for a zero integration time results in an INL of 1.

4 An application example

In the available application a photocurrent integrator is investigated, which operates with two automatically selectable gains, in order to relax the requirements on the OTA. To implement an automatic gain control (AGC) an auto zero comparator is used, which controls the two feedback capacitors. The principle is shown in Fig. 6. If the output voltage exceeds the threshold voltage of the comparator, a second capacitor with a 31 times larger capacitance is switched in parallel. Then the integrator has turned from high into low gain configuration, because signal charge is shared between

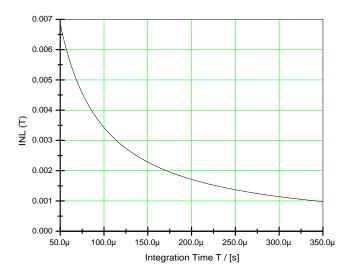


Fig. 5. INL over integration time T.

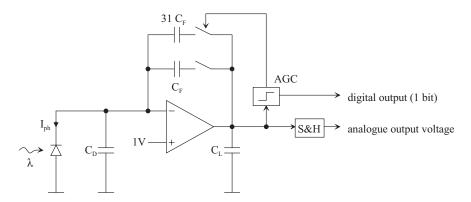


Fig. 6. Pixel readout electronics.

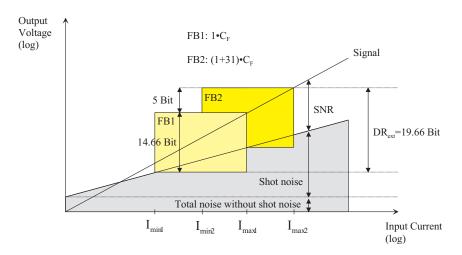


Fig. 7. Dynamic range extension by automatic gain control.

Table 1. Specifications of the photocurrent integrator.

Minimum Signal (theoretical)	99.33 fA	Dynamic Range (theoretical)	19.66 Bit
Minimum Signal (noise determined)	491.83 fA	Dynamic Range (noise determined)	17.35 Bit
Maximum Signal	82.29 nA	Linearity (FB1)	10.33 Bit
Integration Time	$350~\mu \mathrm{s}$	Linearity (FB2)	13.99 Bit

the capacitors correspondingly to their ratio. After a frame period, the signal is held by a sample and hold stage (S&H) and can be read out during the next frame period using a row and column multiplexer circuitry, whereas the used gain is determined by the digital output.

In photocurrent integration, the minimum input signal that can be processed is defined by the input-referred noise, and the maximum output voltage swing defines the maximum output signal. This leads to the conclusion, that noise determines the dynamic range (DR) and the signal-to-noise ratio (SNR). Due to the shot noise, the maximum SNR is signal dependent, and the maximum SNR is not equal to the dynamic range.

A dynamic range extension is possible by using the automatic gain control. This is visualised for some exemplary values in Fig. 7, in which the feedback FB2 has a feedback capacitance 32 times larger than feedback capacitance FB1. The signal and the noise at the output are plotted over the input current. The noise consists of the signal-dependent shot noise and the remaining constant noise. The extension of the dynamic range is determined by the ratio of the feedback capacitors.

The specifications used in this application example are listed in Table 1. Here the specifications concerned to the minimum input photocurrent are distinguished between the theoretical capability of the integrator and the value limited by the noise and the dark current of the photodiode.

5 Summary and conclusion

The principle of a noise analysis of a current integrator has been demonstrated. This noise analysis led to the conclusion, that the input capacitance of the photodiode has to be kept at minimum. Also decreasing the bandwidth is an important measure to reduce noise. These conclusions can be extended to all current readout circuits.

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