Advances in Radio Science, 3, 377–381, 2005
SRef-ID: 1684-9973/ars/2005-3-377

Advances in Radio Science

Challenges of V_{DD} scaling for analog circuits: an amplifier

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Abstract. With the shrinking of the device dimensions, the power supply voltage value is continuously decreasing. Since the threshold voltage value does not decrease as much as the power supply and the drain source saturation voltage becomes an important fraction of the power supply, many amplifier architectures are no more suitable for modern processes. A transconductance amplifier based on current mirrors is analyzed highlighting the main challenges of a low-voltage analog design. Among the many proposed amplifier architectures, a topology based on current mirrors has been chosen as the most promising to operate with low voltages. Simulations with 90 nm CMOS prove the feasibility of circuit operation with satisfactory performance at an operating power supply voltage as low as 0.6 V.

1 Supply Voltage and Threshold Voltage Scaling

Due to the scaling of the device dimensions and of the growth of the higher performance and lower power market, the supply and the threshold voltages of the CMOS circuits are constantly decreasing. The determination of the threshold voltage value is a compromise between the desire of a sufficiently large saturation current that determines the dynamic performance and the need to limitate the subthreshold leakage currents. The power supply is usually set to the smallest value necessary to maintain a sufficient overdrive voltage to meet the desired saturation current. The different technical requirements of the several portions of the semiconductor market lead to several parameter scaling and therefore to different transistor devices in the same technology node. In Fig. 1 the development and the forecast of threshold voltage for device designed for high performance, for low operating power and for low standby power applications are reported (Roadmap, 2003).

2 Moderate Inversion

In recent years, mixed signal circuits, whose analog and digital parts are realized on the same chip sharing the same technology and the same power supply, become usual practice. The supply voltage scaling, largely applied to reduce the power consumption in digital applications, limits the performance of these blocks. However its effects on analog circuits are even stronger, since the smaller difference between the supply and the threshold voltage reduces the available overdrive voltage, leading the transistors in moderate inversion where the design of the analog circuit is a demanding challenge. Moderate inversion is the transition region between the weak and the strong inversion regimes and it is characterized by an overdrive voltage between approximately one and five thermal voltages ($U_T{=}kT/q$) (Cunha, 1998). In this transition zone, the sub-threshold characteristics must smoothly link up with the strong inversion ones. Since the channel is only partially built, MOSFETs exhibit small drain currents per area, therefore large dimensions are necessary to obtain acceptable frequency range. The transconductance to current ratio g_m/I_{DS}, which reaches its maximum in the sub-threshold region, makes moderate inversion device interesting as input stage of amplification stages. A substantial drawback of this operating region is the minimum required drain source voltage V_{DSAT}, which does not scale with the overdrive voltage as in strong inversion, but it reaches a minimum at $4U_T$. A further difficulty for the circuit design is the lack of a simple transistor equation that could allow approximate handmade dimensioning. In Fig. 2 the ratio g_m/I_{DS} and the voltage V_{DSAT} are reported versus the normalized current. I_S is defined as the current flowing in the transistor when the overdrive voltage is equal to one thermal voltage. The moderate inversion region is represented by the dashed area.

3 Current Mirrors

The current mirror is one of the basic and most common structures in IC circuit design. Precision of current mirrors relies on symmetry among its devices and their biasing. These circuits, thanks to their simplicity, are suitable for low power applications, so that current mode circuits are considered a promising approach for low power circuit design. In this paragraph the supply limitations of two current mirror architectures are analyzed.

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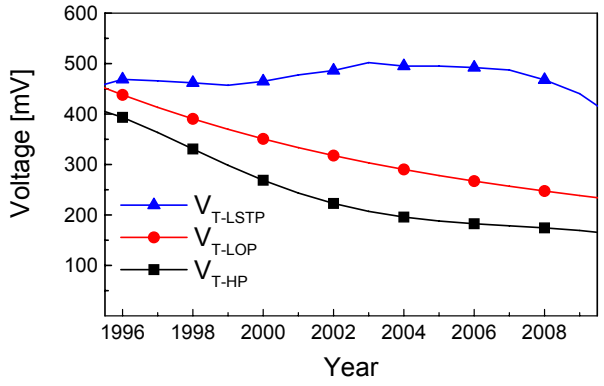

Fig. 1. V_T scaling for the high performance (HP), low operating power (LOP) and low standby power (LSTP) devices.

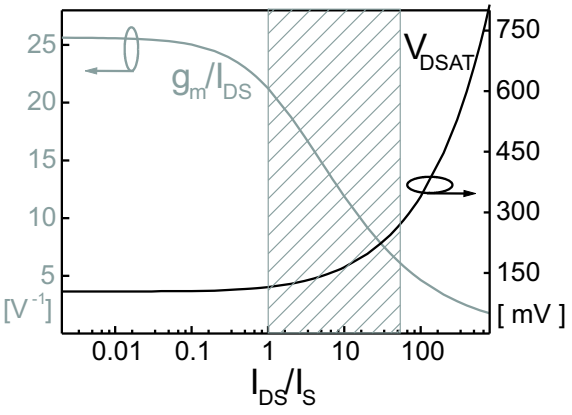

Fig. 2. g_m/I_{DS} ratio and V_{DSAT} vs. the normalized current

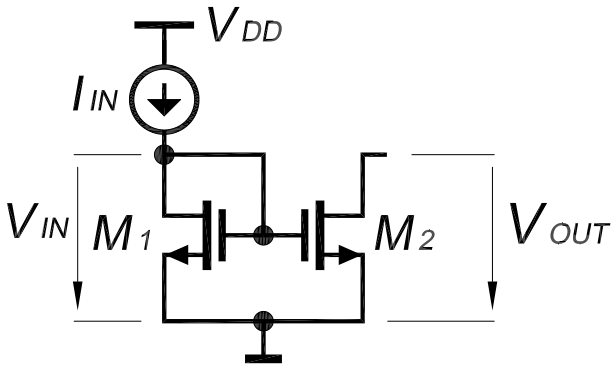

Fig. 3. Simple Current Mirror.

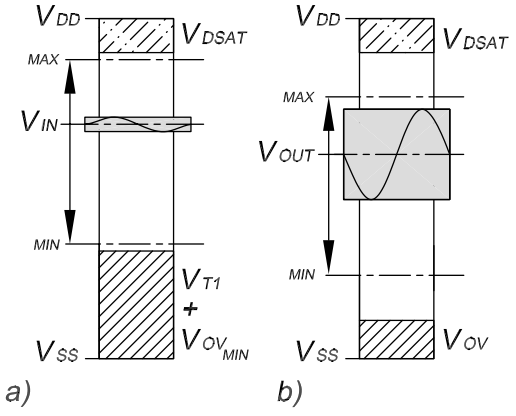

Fig. 4. Allowable input **(a)** and output **(b)** DC Voltages for the Simple Current Mirror.

An ideal current mirror is characterized by a ratio between the output and the input currents that must be independent from the input and the output voltages. This condition can be restated with the following requirements: the current mirror is a current controlled current source with an infinite output resistance and a negligible input resistance.

The simplest current mirror consists of two transistors, M_1 and M_2, whose gates are shorted to the drain of the input device M_1, Fig. 3. Assuming the transistors biased in saturation region, the gate-source voltage of the transistors is:

$$V_{GS} = V_{T1} + V_{OV} = V_{T1} + \sqrt{\frac{2I_1}{\mu C_{ox} W/L}} \qquad (1)$$

The range of the feasible DC voltages at the input and at the output nodes is reported in Fig. 4. The minimum value that the input DC voltage can assume is $V_{SS}+V_{T1}+V_{OV_{MIN}}+V_{in}$, i.e. the minimum gate-source voltage that leads the input transistor in strong inversion plus the amplitude of the input voltage signal. The upper limit of the input DC voltage is given by the amplitude of the voltage signal V_{in} and by the current source I_{IN}, that experiences at least a voltage V_{DSAT} across its terminals when realized with transistor devices. This limit is drawn with dashed lines, since it is given by the external circuit and not by the current mirror itself. The DC output range is indicated with a similar notation. To maintain the output transistor M_2 in saturation, the output voltage, i.e. the drain voltage of M_2, must be larger than its overdrive voltage V_{OV}. Therefore the DC output voltage must be above this limit plus the amplitude of the output signal. The upper limit for the DC output voltage is set by the external circuit. Besides the limited input and the output voltage ranges where the current ratio is characterized by a constant value, this simple current mirror presents two more nonidealities: a no-zero input resistance, $1/g_{m1}$, and a finite output resistance, r_{DS2}.

If the input node of a current mirror requires a low DC voltage, it can be disconnected from the gate of the input transistor by means of an additional MOSFET, M_3, in the circuit reported in Fig. 5 (Peluso, 1998). This modified circuit presents two possible input nodes: *IN1* at the gate of M_1 and *IN2* at its drain. In Fig. 6, the range of the DC voltages at the inputs and at the output are reported. The lower limit of the DC voltage range of the input *IN1* is the maximum between the sum of the drain-source voltages of the transistors M_1 and M_3 and the gate-source voltage of the transistor M_1. If the transistor M_1 operates in saturation regime, its overdrive voltage is equal to its minimum drain-source voltage,

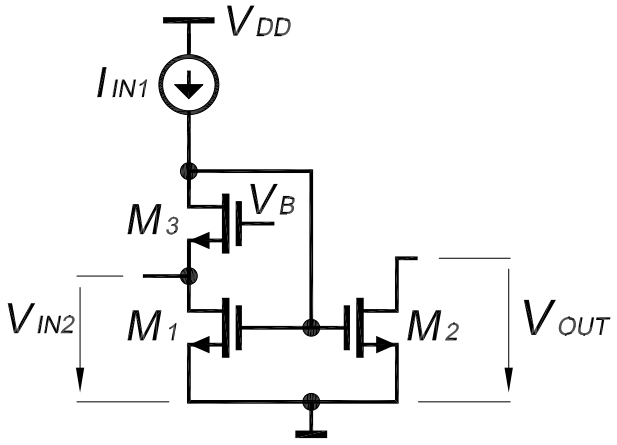

Fig. 5. Low Voltage Current Mirror.

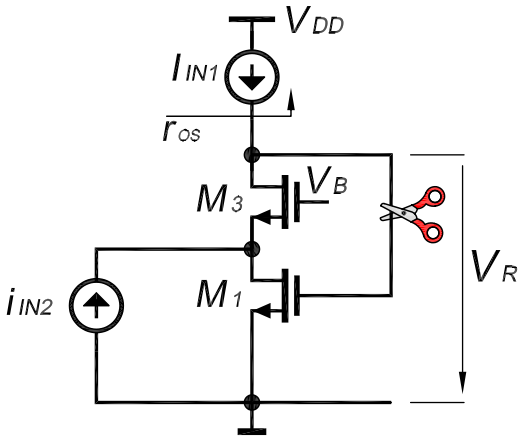

Fig. 7. Cutting for the loop gain computation.

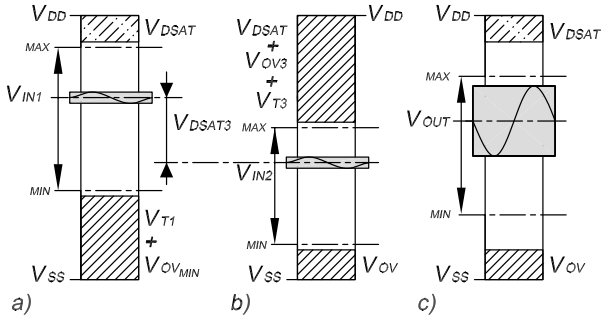

Fig. 6. Allowable DC Voltages for Low Voltage Current Mirror at the inputs IN1 **(a)**, IN2 **(b)** and at the output **(c)**.

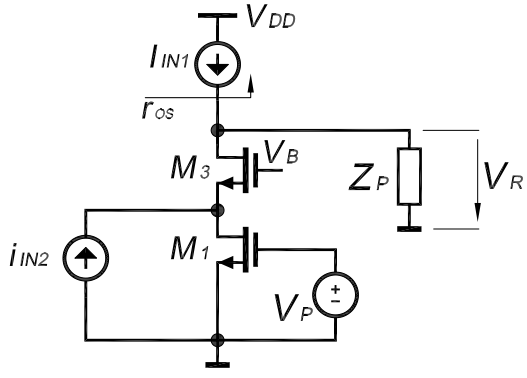

Fig. 8. Equivalent Circuit after cutting for the loop gain computation.

therefore, under the assumption that the threshold voltage V_{T1} of the transistor M_1 is larger than the minimum drain-source voltage of the MOSFET M_3, the DC voltage range of the input *IN1* is identical to the simple current mirror one. The minimum DC voltage at the input *IN2* is determined by the saturation condition of transistor M_1, i.e. it is equal to the overdrive voltage V_{OV}, while its upper border is given by the requirements on transistor M_3. In Fig. 6 is reported the case where V_B, the gate voltage of transistor M_3, is one V_{DSAT} lower than the power supply. A further condition ties together the choice of the DC voltages of the inputs: their voltage difference must be larger than the minimum drain-source voltage of transistor M_3. The minimum output voltage and the output resistance of this circuit are equal to the results derived for the simple current mirror.

In this circuit a shunt-shunt feedback loop can be identified. The small signal input current source i_{IN2} is connected to the source of the transistor M_3, a common gate stage, that amplifies at its drain any modification of the input voltage, v_{in2}. Since M_3 drain is also the gate of the transistor M_1, the amplified voltage signal causes a current of the transistor M_1, that subtracted to the input signal, forces the voltage at the input node to remain constant. If the feedback loop gain is sufficiently large, the error current i_ε flowing through M_3 is negligible. To compute the feedback gain loop, a cut is made at the gate of the transistor M_1 to divide the the feed-forward and the feedback networks, Fig. 7, and its equivalent circuit is built, Fig. 8. The impedance Z_P has the same value of the the impedance between the node V_R and ground in the original network. The biasing of the MOSFET M_1 is provided by a voltage source V_P, whose value is equal to V_R of the original network. With this cut, the feed-forward and the feedback networks are separated and unidirectional (Pellegrini, 1972), until high frequencies where the circuit functionality is mostly determined by the parasitic capacitances of the transistors.

The feed-forward transfer function, R_{FF}, is calculated as the ratio between the small signal output voltage v_r and the small signal input current i_{in2}, when the the feedback path is disconnected, i.e. when the small signal current source v_p is null, Fig. 9. The feedback conductance G_{FB} is calculated as the ratio between the small signal feedback current i_F flowing in the transistor M_1 and the voltage v_p.

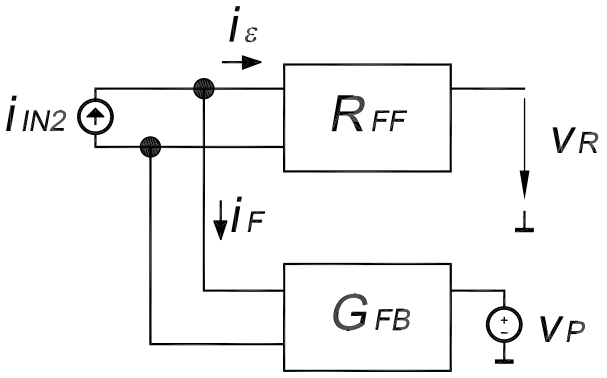

Fig. 9. Model of the shunt-shunt feedback system.

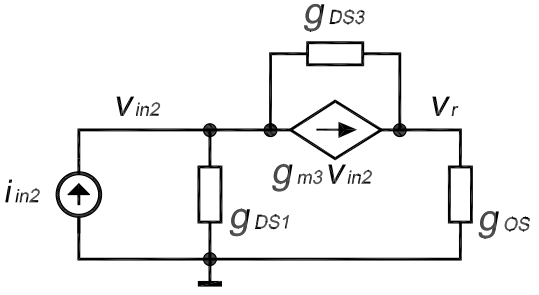

Fig. 10. Small Signal Equivalent Circuit for R_{FF} calculation.

The small signal equivalent circuit for the computation of the feed-forward gain is reported in Fig. 10. Since the voltage source v_p is turn off, the voltage controlled current source $g_{m1}v_{gs1}$ is null.

From the equations of the nodes:

$$\begin{cases} i_{in2} = g_{DS1}\, v_{in2} + g_{m3}\, v_{in2} + g_{DS3}\, (v_{in2} - v_r) \\ i_{in2} = g_{DS1}\, v_{in2} + g_{OS}\, v_r \end{cases} \tag{2}$$

where g_{DS1} and g_{DS3} are the conductance values of M_1 and M_3 respectively, g_{OS} is the output resistance of the current source I_{IN1}, while g_{m3} is the transconductance value of the transistor M_3. The input resistance $R_{in_{FF}}$ and the gain R_{FF} of the feed-forward block in open loop are:

$$\begin{cases} R_{in_{FF}} = \left.\dfrac{v_{in2}}{i_{in2}}\right|_{v_p=0} = \dfrac{g_{DS3}+g_{OS}}{(g_{DS1}+g_{DS3}+g_{m3})g_{OS}+g_{DS1}g_{DS3}} \simeq \dfrac{g_{DS3}+g_{OS}}{g_{m3}\, g_{OS}} \\ R_{FF} = \left.\dfrac{v_r}{i_{in2}}\right|_{v_p=0} = \dfrac{g_{m3}+g_{DS3}}{(g_{DS1}+g_{DS3}+g_{m3})g_{OS}+g_{DS1}g_{DS3}} \simeq \dfrac{1}{g_{OS}} \end{cases} \tag{3}$$

Similarly, the gain of the feedback network is calculated when the input small signal current i_{in2} is null, resulting into:

$$G_{FB} = \left.\frac{i_F}{v_p}\right|_{i_{in2}=0} = g_{m1} \tag{4}$$

The feedback loop gain is therefore:

$$R_{FF}G_{FB} = \frac{(g_{m3}+g_{DS3})g_{m1}}{(g_{DS1}+g_{DS3}+g_{m3})g_{OS}+g_{DS1}g_{DS3}} \simeq \frac{g_{m1}}{g_{OS}} \tag{5}$$

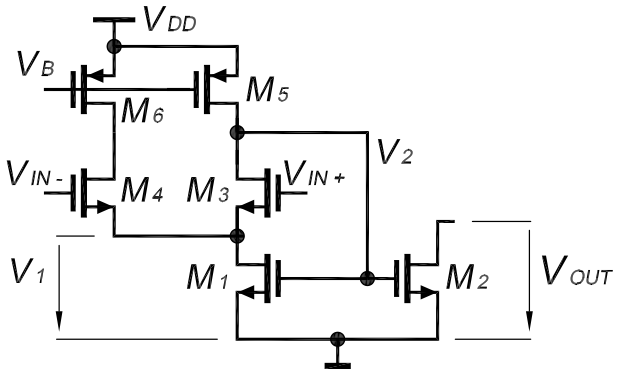

Fig. 11. Differential Input Pair.

Due to the current feedback at the input, the resistance seen by the input source I_{IN2} is equal to the input resistance $R_{in_{FF}}$ determined in open loop reduced by the feedback factor $1+R_{FF}G_{FB}$:

$$R_{IN2} = \frac{v_{in2}}{i_{in2}} = \frac{R_{in_{FF}}}{1 + R_{FF}G_{FB}} = \\ = \frac{g_{DS3}+g_{OS}}{(g_{DS1}+g_{DS3}+g_{m3})g_{OS}+g_{DS1}g_{DS3}+(g_{m3}+g_{DS3})g_{m1}} \\ \simeq \frac{g_{DS3}+g_{OS}}{g_{m1}g_{m3}} \tag{6}$$

That is, the input resistance has been reduced of a factor $g_{m3}/(g_{DS3}+g_{OS})$ with respect to a simple current mirror, tending to the ideal zero value of the input resistance of a current mirror. The transfer function of this circuit, v_r/i_{in2} is given by:

$$\frac{v_r}{i_{in2}} = \frac{R_{FF}}{1 + R_{FF}G_{FB}} = \\ \frac{g_{m3}+g_{DS3}}{g_{m3}(g_{m1}+g_{OS})+g_{m1}g_{DS3}+(g_{DS1}+g_{DS3})g_{OS}+g_{DS1}g_{DS3}} \\ \simeq \frac{1}{g_{m1}} \tag{7}$$

For the small signal, with similar considerations at the input I_{IN1}, when the feedback loop is sufficiently large, the output current of this low voltage current mirror, i.e. the current through the transistor M_2, can be proved equal to the sum of the input currents, that is:

$$i_{out} = i_2 = g_{m1}v_r \simeq g_{m1}\left(\frac{i_{in1}+i_{in2}}{g_{m1}}\right) \tag{8}$$

4 Fully Differential Amplifier

Figure 11 shows a differential input stage based on the low voltage current mirror. The input differential signal v_{in} is applied between the gate of the MOSFETs M_3 and M_4 which constitute the differential pair. The current sources M_5 and M_6 are biased by a constant voltage V_B. In spite of its asymmetry, this circuit operates as a differential stage, due to the

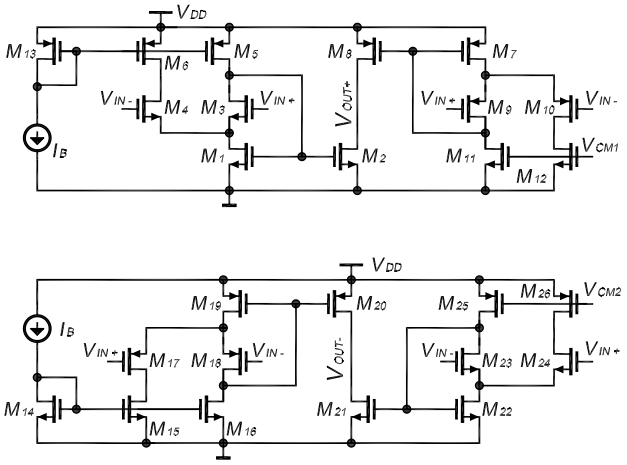

Fig. 12. Fully Differential OTA.

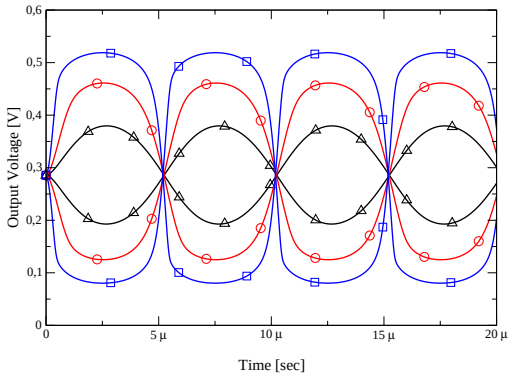

Fig. 13. Output Voltages for 3 input amplitudes.

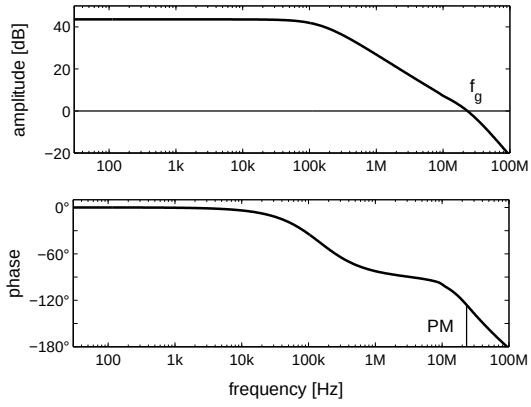

Fig. 14. Bode Diagram of the circuit.

feedback loop realized by the transistor M_3 that forces the voltage V_1 to follow the positive input voltage, since the current flowing into the transistor M_3 and therefore its gate source voltage must remain constant. Therefore the MOSFET M_4 experiences a gate source voltage signal equal to the entire differential input, and its small signal drain source current is proportional to the input voltage $i_{ds4}{=}g_{m4}v_{in}$. This current is equivalent to the current source I_{IN2} studied in the previous section, it flows into the transistor M_1 and it is mirrored at the output.

A fully differential transconductance amplifier based on the low voltage input differential stage is shown in Fig. 12. Fully differential structures are preferred to single ended amplifiers, although they require a larger area, since they present a larger immunity to power supply and input noise, they cancel the even harmonic components of the distortion and they are more robust to parameter fluctuations. This amplifier architecture has been realized without cascode stages, since these structures become critical for low supply voltages. The circuit is a one-stage amplifier driving a capacitive load. The common mode voltage at the input and at the output nodes is set to analog ground, $V_{DD}/2$. The inverter output stage operates in class AB, generating rail-to-rail output voltages without requiring a large power consumption in the bias point Fig. 13. The circuit has two common mode circuits, that regulate independently the two amplification blocks, so that the amplifier can independently compensate for variations of the pMOSFET and of the nMOSFET input differential pair introduced by parameter fluctuations and for variation of the input common mode voltage. The circuit, biased with a single power supply voltage of 0.6 V, is designed and simulated using a 90 nm standard CMOS process. A low frequency amplification of 44 dB and unity gain bandwidth f_g above 23 MHz for a capacitive load of 1.6 pF are obtained, Fig. 14. The phase and the gain margin are 55° and 25 dB, respectively. The power consumption of the circuit is 32 μW.

5 Conclusion

In this paper the main limits of some analog circuits for very low voltage applications are analyzed and an alternative current mirror is closely studied. Based on this basic block, a low-voltage low-power fully differential amplifier with rail-to-rail outputs operating with 0.6 V is presented. Simulated in a 90nm standard CMOS gives a low frequency gain 44 dB and a unity gain bandwidth is 23 MHz.

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