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A Contribution to Reconfigurable Analog Electronics by a Digitally Programmable Sensor Signal Amplifier

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Abstract. In particular, primary sensor electronics are prone to deviations and degradation in its performance due to environmental influences and manufacturing conditions. In order to restore its functionality, calibration or trimming techniques are usually employed. More recent, programmable or reconfigurable approaches from the field of evolutionary electronics offer great source of inspiration through their unique properties of fault-tolerance and self-repair. In our approach, we try to include efficiently, the available knowledge of recent reconfigurable devices into the otherwise attractive concept. In our approach, a flexible FPTA architecture is developed meeting the requirement of sensor signal amplifier in particular for time continuous signal processing. The developed approach is verified and implemented in 0.35 μm CMOS technology.

1 Introduction

Primary sensor electronics are susceptible to drifts due to changing environmental influences and manufacturing conditions like aging, thermal drifts, etching rate, material defects. These effects are capable of causing considerable variations in the functionality of the analog corresponding circuits, as they have rich set of dynamics than the digital counterpart. Recent measures to restore the functionality are performed through several ways like careful matched layout design, calibration or trimming at manufacturing time are mandatory. Normally these approaches are slow with respect to deployment time, costly, static and have to be performed repeatedly when done dynamically. Especially *on the fly calibration* capability is desirable for sensor systems. More recent improved approaches (Analog Devices, 2004) extend these established procedures to compensation techniques during the actual operating phase (Frühauf et al., 2002). Some recent approaches and products developed and made available for dynamic self-calibration of analog systems/components are ALD2724x (EPAD) and AD8555 (DigiTrim) amplifiers. The ALD2724x are developed by Analog Linear Devices Inc. in which trimming is done by EEPROM with finite number of correction cycles. Whereas in AD8555, trimming is done by DAC with volatile memory/switches through infinite correction cycles. The so far discussed programmable analog devices are more concerned with the calibration point of view. Other available reconfigurable analog devices are Zetex TRAC, Cypress PSoC, Lattice ispPAC30, Anadigm Vortex, IMTEK G_mC-Filters, and KIP FPTA. These devices differ from each other based on their granularity. Most commercial versions are based on building block level (course grained). These reconfigurable analog devices have strong relation to evolvable hardware. Much more extensive concepts for practical engineering application are provided by the quite recent field of evolutionary electronics (Zebulum et al., 2002), where circuits are bred by appropriate learning and optimization approach, commonly affiliated to the field of evolutionary computation. In particular, programmable, flexible special purpose hardware can serve as the target or implementation platform for such analog or mixed-signal circuits. A collection of such approaches are denoted as Field-Programmable-Transistor-Arrays (FPTA). The general approach bases on homogeneous transistor array, where appropriate circuits are bred literally according to prescribed specification (Zebulum et al., 2002; Langeheine et al., 2003). In spite of interesting results, this approach has several drawbacks, like the circuit creation by evolutionary computation always starts from scratch or from primal soup which can lead to peculiar solution. Secondly, the use of homogeneous transistor arrays demands excessive switching resources. The use of optimization algorithms also wastes the existing knowledge of the experienced designers. These drawbacks form the basis of our new approach of reconfigurable analog electronics in particular to sensor signal amplifiers which are configured digitally. In this paper, we will report on the general concept of reconfigurable operational amplifier, implementation of OPA, simulation results and finally on the status of the physical chip implementation and envisioned applications.

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2 Concept of Reconfigurable OPA

Our approach starts from medium granularity, and combines the concepts presented in the previous section to obtain

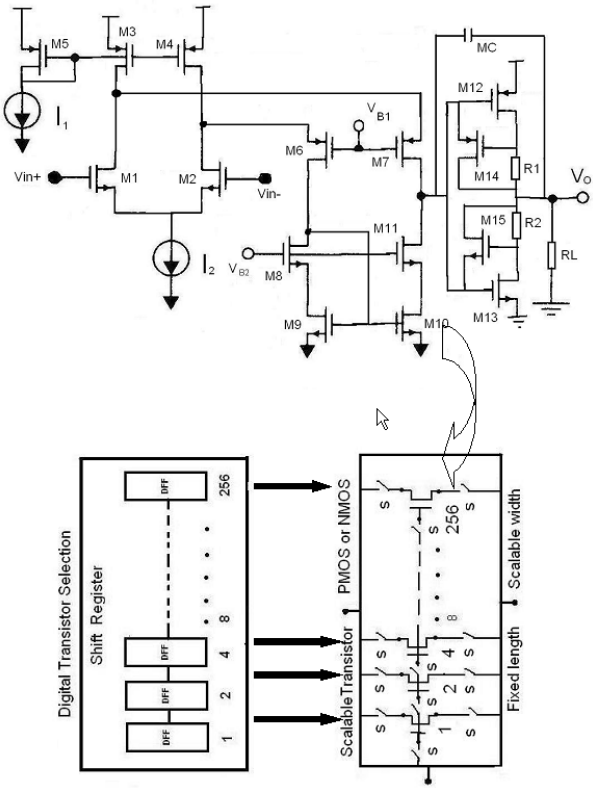

Fig. 1. Folded-cascode-operational amplifier and the replacement scheme of ordinary by scalable transistors.

digitally configurable sensor electronics and with regard to its performance, be continuously self calibrating during the course of its operation. Current FPTA's are homogeneous transistor arrays. The arrays all together provide transistors with variety of lengths and widths. These arrays can be interconnected using large number of switches to form a novel circuitry. After investigation of the current FPTA, we focused our work on the design of sensor signal amplifier with medium granular structure of the FPTA thereby making the transistor array heterogeneous. This is achievable through fixing the length of the transistor in the operational amplifier circuit design to a suitable unit length. The appropriate length is determined through simulations and the choice was conservative. Furthermore, transistor sizing can efficiently be done from the inspiration taken from A/D-D/A converters by which the elementary transistors in the heterogeneous array are sized by the powers of two. These two simple design approaches reduce the number of required switches and thus, the parameters of the design algorithm. Our approach also introduces hierarchy switches (transistor/topology/array). The low level switches interconnect the elementary transistors to form dynamically scalable transistors. The medium level switches define the overall amplifier topology, e.g., Miller-, folded-cascode-OPA, formed basically by interconnecting the available scalable transistors. Finally, the top level switches configure single or multiple amplifier blocks to form complex circuits like the

Table 1. Some feasible aspect ratios for the FC-OPA design by ordinary and scalable transistors.

Name	W=1 μ	W=2 μ	W=4 μ	W=8 μ	W=16 μ
M1	1	2	4	8	16
M2	1	2	4	8	16
M3	32	64	64	64	128
M4	32	64	64	64	128
M5	128	128	128	128	128
M6	32	64	32	64	128
M7	32	64	32	64	128
M8	8	64	16	8	32
M9	8	64	16	8	32
M10	8	64	16	8	32
M11	8	64	16	8	32
M12	128	128	128	128	128
M13	64	64	64	64	64
M14	16	16	16	16	16
M15	16	16	16	16	16
I1μA	100	100	100	100	100
I2μA	100	100	100	100	100
R1, R2	50	50	50	50	50
MC	1p	1p	1p	1p	1p
RL	1K	1K	1K	1K	1K

instrumentation amplifiers. This hierarchical switching approach allows reduction in the use of switching resources. In our approach a simple transmission gate is used. The appropriate switch dimensions are determined based on the parameters like ON-resistance, parasitic capacitance, noise and so on in order to avoid considerable changes in the circuit performance. The appropriate switch dimension so determined will be reported in the following sections. The switching patterns are incorporated into the reconfigurable usually through

Table 2. Some feasible aspect ratio for the FC-OPA design with standard and scalable transistors.

Name	W=32 µ	W=64 µ	W=128 µ	W=256 µ
M1	32	64	128	256
M2	32	64	128	256
M3	256	128	256	256
M4	256	128	256	256
M5	256	256	256	256
M6	256	128	128	128
M7	256	128	128	128
M8	32	64	64	64
M9	32	64	64	64
M10	32	64	64	64
M11	32	64	64	64
M12	128	128	128	256
M13	64	64	64	64
M14	16	16	16	16
M15	16	16	16	16
I1µA	100	100	100	100
I2µA	100	100	100	100
R1,R2	50	50	50	50
MC	1p	1p	1p	1p
RL	1K	1K	1K	1K

random access address options. However, with regard to the rather low update time constraints in the envisioned application fields and the tight cost constraints on electronic discrete components, a serial approach based on a shift register will be preferred in the next steps of our work. The

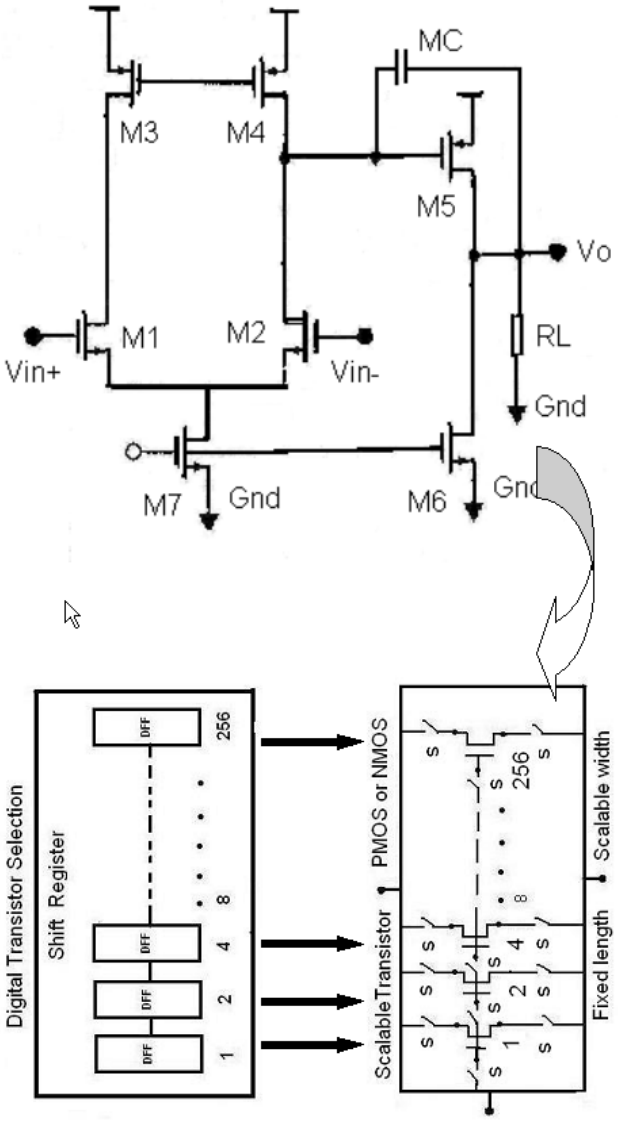

Fig. 2. Miller operational amplifier and the replacement scheme of ordinary by scalable transistors.

described concepts offer the baseline for application of various algorithms serving for self-calibration, automatic and manual configuration of the amplifier unit.

3 Implementation of Reconfigurable OPA

The pursued concepts in the previous sections are first implemented for a sensor signal operational amplifier with folded-cascode topology.

Figure 1 shows the schematic of the amplifier implementation employing standard transistors of the chosen technology. For this reference model simulations were carried out to find a suiting length parameter as well as the aspect ratios of all the transistors used in building the FC-OPA. Further, a feasible range of the powers of two for the aspired scalable

Table 3. Simulation results obtained for the folded-cascode reference model amplifier with standard transistors and aspect ratio according to Tables 1/2.

Different Width in µ	Gain in dB	GBW in MHZ	PM in Deg
W= 2	95	15	78
W= 4	100	12	75
W= 8	103	35	62
W= 16	101	21	51
W= 32	95	32	60
W= 64	110	13	60
W= 128	100	39	51
W= 256	101	40	50

Table 4. Simulation results obtained for the folded-cascode reference model amplifier with scalable transistors and aspect ratio according to Tables 1/2.

Different Width in µ	Gain in dB	GBW in MHZ	PM in Deg
W= 2	90	25	80
W= 4	95	28	70
W= 8	101	25	50
W= 16	115	30	50
W= 32	110	15	50
W= 64	110	23	55
W= 128	103	18	50
W= 256	105	17	40

transistors are determined. Finally, the effect of switch dimensioning are also investigated and fixed.

The design was carried out employing the Cadence DFW II obtained through EUROPRACTICE and Austriamicrosystems HitKit for the chosen 0.35 μm CMOS technology. Tables 1 and 2 show the achieved results for aspect ratio investigation suitable for the reference model. In order to describe the feasibility of our approach, operational amplifier with Miller topology is also constructed both with standard and scalable transistors as shown in Fig. 2 and the corresponding aspect ratio is shown in Table 5.

For both the topologies a fixed transistor length of 2 μm is used as a conservative choice. In future designs substantial length reduction seems feasible.

As the first step of our work on the schematic level, scalable transistor building blocks for NMOS and PMOS transistors were designed. The elementary transistors and the connecting switches constitutes the scalable transistors.

Table 5. Single aspect ratio for Miller-OPA design with both standard and scalable transistors.

Name	M1	M2	M3	M4	M5	M6	M7
W in µ	16	16	128	128	128	256	256

Table 6. Simulation results obtained for the Miller reference model amplifier and aspect ratio according to Table 5.

Differential Pair in µ	Miller-OPA (standard transistors)			Miller-OPA (scalable transistors)		
	Gain in dB	GBW in MHZ	PM in Deg	Gain in dB	GBW in MHZ	PM in Deg
W=16	69	22	55	79	25	56

Ranging from the minimum width to the maximum aspect ratios, a total of 9 stages can be selected. In addition, the minimum sized transistors are duplicated three times so as to reduce the influence caused due to minimum dimensions.To avoid undesired capacitive load, all three pins of the unit transistors are connected to switches, assuming, that for transistors, bulk is set to a common potential. In our work, a simple transmission gate of the dimension 8/0.35 μm is used. A total of 12 switch control lines are required for each scalable transistor (ST). The schematic of the reference model are modified by replacing the standard transistors with ST, as indicated in the lower part of Figs. 1 and 2. The switching signals for each ST in the experiment are set by constant voltages for ON and OFF levels. This allows efficient analog simulations without the burden of simulating the digital part.

Simulation results of the reconfigurable amplifier cell with ST were close to the reference model amplifier with standard transistors to confirm the feasibility of the chosen approach. Table 4 gives the simulation results of the OPA with ST. This can be compared to those obtained by the reference model standard amplifier design in Table 3. In a similar fashion, simulations are performed and results are compared for the operational amplifier with Miller topology. Table 5 gives the dimensions of the transistors used in building the Miller-OPA. Unlike the FC-OPA, Miller-OPA are constructed for a particular aspect ratio. Table 6 gives the simulation results comparison for Miller operational amplifier for both with standard and with scalable transistors.The graphical comparison results for both the reference models, namely, folded-cascode and Miller operational amplifier topology

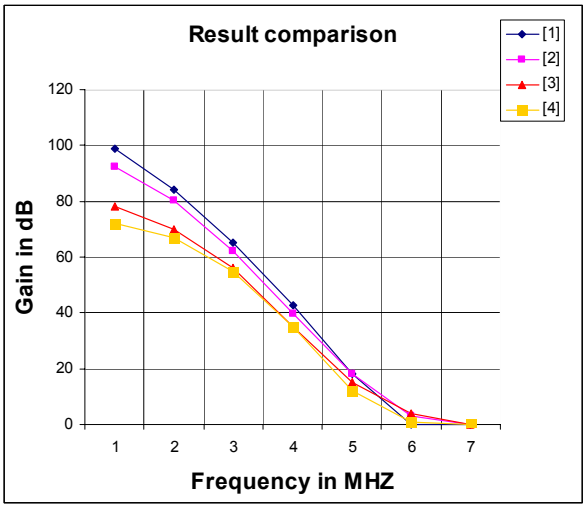

Fig. 3. Gain comparison for both the reference model amplifiers with standard and scalable transistors. ([1] FC-OPA with standard transistors, [2] FC-OPA with scalable transistors, [3] Miller-OPA with scalable transistors, and [4] Miller-OPA with standard transistors.)

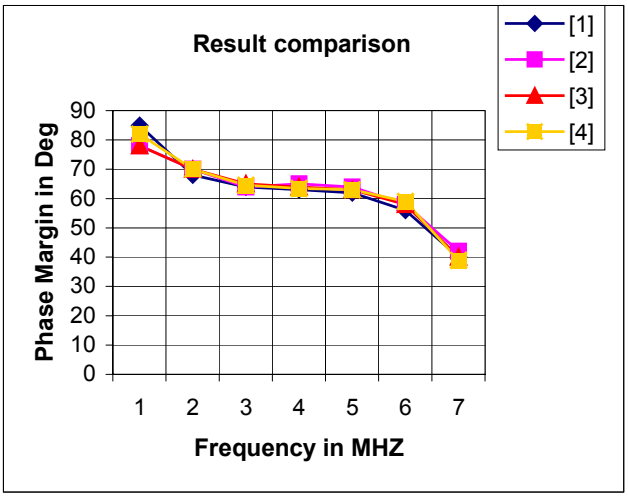

Fig. 4. Phase margin comparison for both the reference model amplifiers with standard and scalable transistors.

with standard and scalable transistors are shown in Figs. 3 and 4 according to Tables 3, 4, and 6.

Based on the promising circuit level simulations, the work can be proceeded further in two different direction. First, the physical realization of the reconfigurable operational amplifier to emerge as a test chip. Secondly, more flexible and complex architecture can be pursued. Flexible reconfigurable amplifier implementations are made feasible by the introduction of the topology switch levels, tailored to the need of the application with optimum effort and power consumption trade off. Furthermore, the concepts of scalable transistors can be used also for passive elements to form fields of resistors and capacitors. Note that the compensation capacitance used for both reference models are separate standard capacitors.

4 Physical Realization of OPA

With respect to practical applications and acceptance of the introduced concept, a typical 8 pin dual-in-line single operational amplifier package is preferred.

In our work, we define a digital interface for the requirement of programming, calibrations or for mixtrinsic evolution purposes. In addition to the normal pins of the OPA, a *serial_In* (D) pin to feed the shift register, a *clock* (CLK) pin, and an *Enable* (EN) pin are required. The enabling signals make sure that the switches do not interact with the circuit operation when turned off until a valid switch pattern are feed into the circuit. Figure 5 shows the pin arrangement for the 8 pin package.

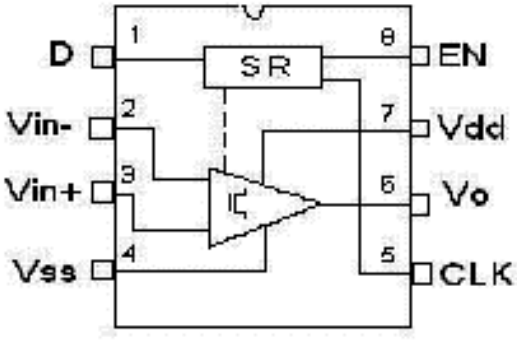

Fig. 5. Aspired chip interface and 8 pin DIL-package.

The shift register along with the additional protection logic were implemented as full custom cells. A general separation between the digital and analog sections is not necessary, since the digital activity is well separated from the operation phase of the analog section. By offering redundancy on the ST level, concepts of self-repair and fault tolerance are addressed. The flexibility of self-repair and fault tolerance options are increased by providing large number of ST's and switches on the topology levels. The basic ST's are realized with 12 stages of unit transistors, equivalent stages of shift registers, switches and protection logics. The chip can serve as a single instance/single amplifier or multiple instances/multiple single amplifiers as in the case of instrumentation amplifier thereby constructing a reconfigurable instrumentation amplifier.

The later one are constructed not only by using scalable transistors, but also with the fields of resistors and capacitors designed by extending the concepts of ST to passive elements. This facilitates the programmability in the compensation and feedback circuitries and is paving the

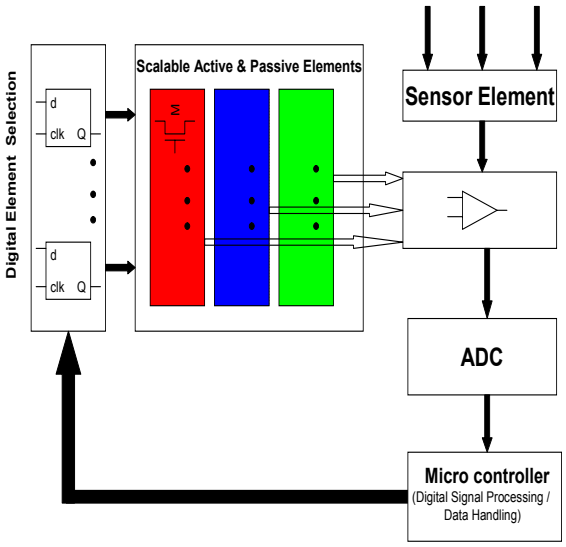

Fig. 6. General architecture of sensor systems built with scalable active and passive devices.

way to build complex circuits like filters and ADC's. Figure 6 shows the architecture of a general purpose sensor system built with scalable active and passive devices. The loop shown in Fig. 5 implies the feasibility of *on the fly* calibration much larger numbers. The increased fault-tolerance and self-healing capability, continuous auto-calibration *on the fly*, trade-off and optimization of parameters like power, gain, and slew-rate, reduced switch counts makes our approach to compensate for the slight larger manufacturing cost due to increased die area.

5 Conclusion

In this paper, we have provided a contribution to reconfigurable analog electronics to meet the need for auto calibration or trimming measures in particular for time continuous signal processing. Fault-tolerance in analog circuits in particular to sensor systems through bio-inspired approach is achieved. The incentive of our approach comes from the inspiration of evolutionary computation and the recent development in measurement instrumentation. The proposed chip will allow digital programming and calibration by algorithms ranging from simple algorithm to evolutionary computation. The costly trimming procedures are reduced by our approach and continuous on the fly calibration will be feasible.

In future work, the complete described concept will be subject to implementation. The implementation will be verified for parasitic influences by post layout simulations. Assessment of general frequency limitations will also be conducted. Further, adaptation algorithms for reconfiguring our circuit will be studied. As a long term perspective, adaptation could be extended including the sensors in the optimization loop (*sensor-in-the-loop-learning*). The adaptive amplifier circuits can help in compensating the drifts.

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