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WCDMA outphasing power amplifier with a software defined transmitter/receiver architecture for determination of the predistortion function

W. Gerhard and R. Knöchel

Microwave Group, University of Kiel, Kiel, 24143, Germany

Abstract. A flexible and easily configurable software defined transmitter/receiver (TX/RX) architecture is described, which allows the determination of the distorted complex transfer characteristics of a 3 port nonlinear outphasing power amplifier (PA) for application in a WCDMA base station. The TX/RX architecture is capable of generating high precision single sideband signals (SSB) using a DSP algorithm, which is almost insensitive to measurement errors and to the frequency response of the output measurement channel. Based on this an inverse predistortion function for a necessary linearization is calculated and implemented into a FPGA (field programmable gate array) through look-up-tables (LUT). The common base band and the differential phase angles are predistorted, resulting in a linearization of the PA.

1 Introduction

The modulation techniques used in WCDMA systems (3GPP TS 25.213 V5.2.0, 2002–09) result in signals with significant simultaneous amplitude (AM) and phase modulation (PM). This poses strong linearity requirements on the PA, which can only be fulfilled under power back off with reduced efficiency. Linearity is traded with efficiency. The thus arising problem may be solved with outphasing amplifiers. That concept was initially introduced by Chireix (1935) and later extended to the LINC (LInear Amplification using nonlinear Components) technique by Cox (1974). The AM/PM-signal is transformed into two constant amplitude counter-rotating solely phase modulated signals commonly carrying the original PM and, in their differential phase, the AM information. The signal separation can be achieved with a fast digital hardware signal processor which requires a wide bandwidth (Gerhard and Knöchel, 2005). The resulting constant envelope signals can be amplified with saturated PAs (class B, C, F) having high efficiencies. By coupling the two PA stages through a purely reactive Chireix output circuit the AM part of the signal can be reconstructed with high efficiency. Due to the direct connection each PA is effectively loaded by a complex impedance which depends on the differential phase modulation. In practice, however, the PAs do not operate in full saturation. They thus do not behave as ideal voltage sources, as it is commonly assumed (Raab, 1985). Due to that reason and because of the properties of the utilized non-ideal transistors, the transfer characteristics of the outphasing PA system will not operate as originally intended but will be distorted. These distortions have to be first determined and then removed by applying a predistortion to the phase modulation in the digital base band. This paper describes a PA applying such a linearization technique. A RX measurement system is required to detect the complex distortion of the output signal. The associated receiver architecture employs a simple vector signal analyzer (VSA) with a 3 stage heterodyne conversion. The last two conversion stages are implemented using a complex Weaver-architecture (Razavi, 1998). The bandwidth is about 50 MHz with a signal to noise ratio (SNR) of better than 70 dB. The architecture admits the generation and adjustment of the required SSB measurement signals with high precision using a robust and insensitive DSP algorithm. After the determination of the complex PA distortions an inverse predistortion function is derived, which predistorts both the differential and the common phase modulation in the digital base band domain, yielding a linearization of the outphasing PA. The signal processing for the determination of the predistortion function is realized on a Host-PC using Matlab. A real-time predistortion of the base band signals is implemented using two LUTs on a fast FPGA which are addressed with the calculated predistortion function.

Correspondence to: W. Gerhard (wg@tf.uni-kiel.de)

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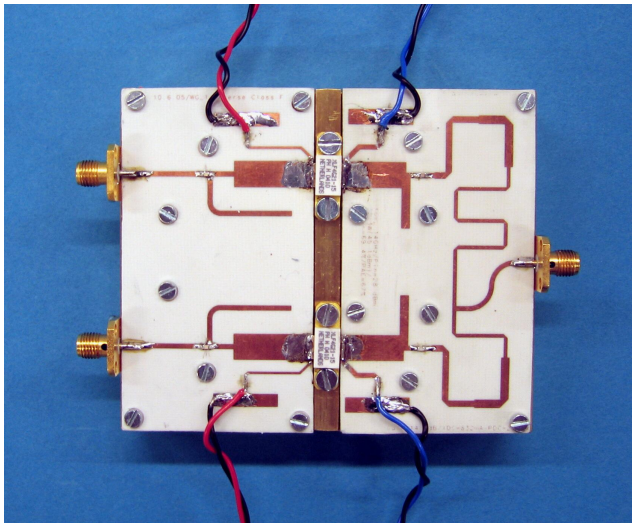

Fig. 1. Implementation of the 24 W outphasing PA.

2 Outphasing PA

Figure 1 shows the practical implementation of a three port 24 W outphasing PA with a direct reactive output coupling of the two transistors. The power transistors used in this design are 15 W Silicon LDMOS (XLF4G21-15) from Philips Semiconductors, Nijmegen, The Netherlands. A nonlinear simulation model for ADS (agilent, USA) and a separate S-parameter file describing the package parasitics were available. Using load pull simulations the optimum load impedance was found for an operating DC drain voltage of 28V. The gate was set to the pinch-off voltage of 2.6 V. The output networks are designed to operate each transistor in an inverse class F mode, which improves the simulated peak drain efficiency from 57% (class B) to 70%. Measurements on a single transistor delivered a drain efficiency of 65% and an output power of about 15 W with a driving power of 28 dBm (Gain = 13.8 dB) at 2.14 GHz. Based on the design and measurement results of a single transistor the direct reactive output coupling between the two transistors was designed. It employs a balun transformation stage, which transforms the complex output impedances (at the "resistive" load), depending on the differential phase, to those at the intrinsic drain ports of the transistors. The resulting impedances as seen by the amplifiers are shown in Fig. 2 as function of the differential phase.

At a differential phase of 45 degrees the two markers indicate inductive and capacitive load conditions. A maximum rf-power of 24 W (43.8 dBm) at 2.14 GHz was measured (-1 dB less than expected) with a corresponding gain of 12.8 dB. A peak drain efficiency of 61% was found, which is only 4% less than the expected value of 65% (single transistor). All circuits were built up using RO4003 20 mil substrate.

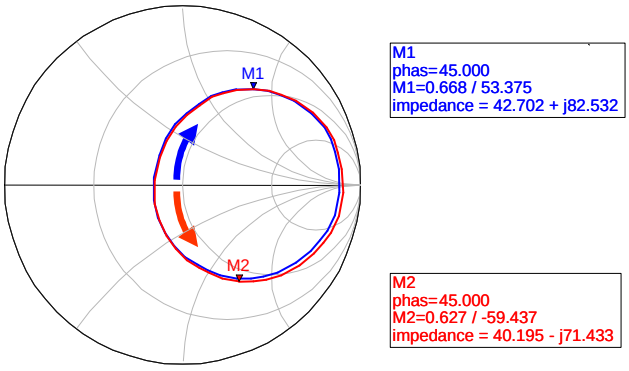

Fig. 2. Impedances at the transistors as function of the differential phase.

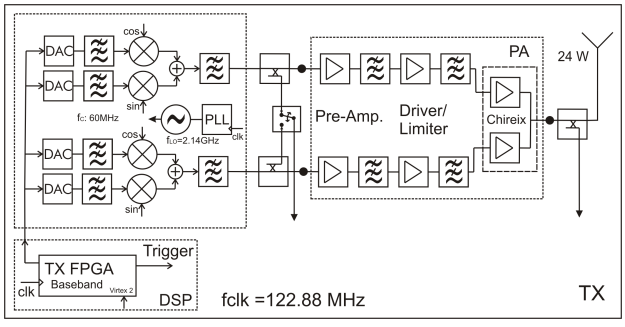

Fig. 3. Schematic of the transmitter topology.

3 Transmitter

3.1 Overview

Figure 3 shows the schematic of the transmitter. The calculation of the differential phase modulation and the generation of the SSB signals are carried out in the digital base band domain. The mathematical algorithms are implemented on a fast digital hardware. A Virtex-II FPGA from Xilinx (Virtex-II, 2001) operating with a sampling frequency of 32 times the UMTS chip rate of 3.84 Mchips/s (122.88 MHz) is used. Four base band channels are digital-analogue converted and then up converted to the rf domain using a direct conversion architecture with two active I/Q mixers. The I/Q mixers hence form a quadrature amplitude modulation circuit which is capable of generating the required PM and SSB signals. The signals are subsequently amplified in multi stages to achieve a sufficient driving power for the main PA of 28 dBm. Three points, as indicated in Fig. 3, denote the complete three port amplifier chain, which forms the nonlinear outphasing amplifier, the distortions of which have to be determined and removed by the linearization.

The three indicated terminals of the amplifier are accessible for the measurement receiver by directional couplers and by switches for performing measurements.

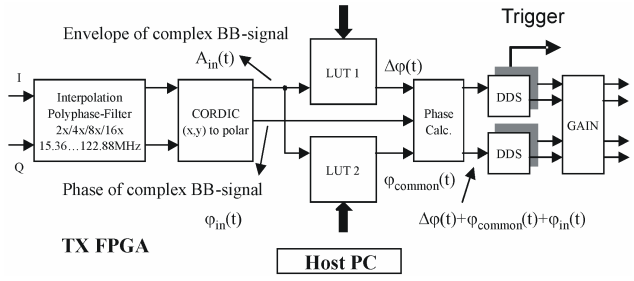

Fig. 4. DSP hardware implementation on the TX FPGA.

3.2 Base band implementation

The hardware implementation of the digital signal processor on the TX-FPA is shown in Fig. 4. Two pseudo noise bit sources, I and Q, with a chip rate of 3.84 Mchips/s are implemented. They are pulse shaped with 2 × oversampling (7.68 MHz) and then interpolated 16 × to a sampling frequency of 122.88 MHz employing efficient polyphase filters. With a special CORDIC algorithm the I/Q signals are transformed from their cartesian into the polar representation.

Thus the envelope and the instantaneous phase information of the base band signal are determined. LUT1 is used to transform the envelope to the corresponding differential phase modulation. Without applying a signal predistortion an arcos() function would be stored and LUT2 would not be required. In order to linearize the PA transfer characteristics LUT2 becomes necessary for applying predistortion to the common phase (instantaneous base band phase). The LUTs are implemented with a 16 × 16 bit resolution, which yields a very high and precise resolution. Four Direct Digital Synthesizers (DDS) are implemented. They serve different tasks:

1. In the TX mode the DDSs separate the phase modulation into the real and the imaginary part, cos(), sin(). Together with the rf QAM up conversion architecture phase modulated constant envelope signals are generated.

2. The DDSs are used as frequency generators to generate SSB test signals for measuring the PA distortions after the phase modulation of the DDSs is switched off. Each channel can be adjusted in frequency, amplitude (gain block) and phase with very high precision and SSB suppression.

3. The DDSs produce a trigger-signal, after they are started well defined at a zero phase, which is used at the RX side for defined phase measurements and synchronous repetition of measurements to average the signals, which reduces the measurement errors defined by noise fluctuations.

With the use of active I/Q mixers a high LO suppression of -60 dB can be obtained. The signal to noise ratio (SNR)

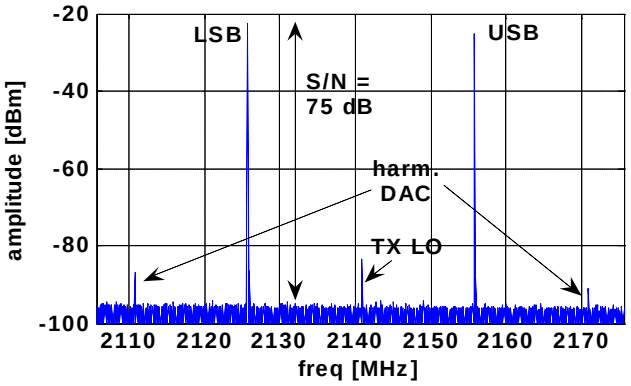

Fig. 5. TX-DSB-spectrum at 2.14 GHz with a base band frequency of 15 MHz. Phase noise: 1 KHz offset: -95 dBc, rms-phase: 0.65°.

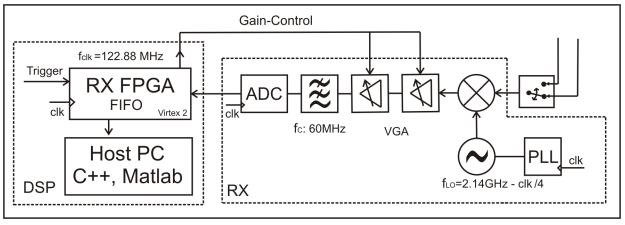

Fig. 6. Hardware implementation of the wideband measurement receiver.

is better than 75 dB and distortions like harmonics and intermodulation distortions are suppressed better than 65 dB. The designed low phase noise PLL has an rms phase noise of about 0.65°. Figure 5 shows the double side band (DSB) spectrum plot of one rf branch.

4 Measurement receiver

4.1 RX Architecture

The schematic of the RX system is shown in Fig. 6. The rf front end of the measurement receiver is designed as a "near zero IF" conversion stage, i.e. a single heterodyne conversion with a low 1. IF. The rf signal is down converted to an IF of 30.72 MHz, which is clk/4. This is done by a second PLL, which is coupled to the same reference clock of 122.88 MHz. This allows synchronous operation of all building blocks of the TX/RX system. The theoretical bandwidth of the receiver is clk/2, i.e. about 60 MHz. The disadvantage of this RX architecture is the image reject problem, which becomes important if the overall outphasing PA initially is not calibrated. In this situation the PA output spectrum needs a huge frequency bandwidth and an aliasing problem occurs. It will be shown later how this problem can be alleviated.

The first IF is amplified twice by voltage controlled gain amplifiers (VGA) with high linearity. It is sampled by an

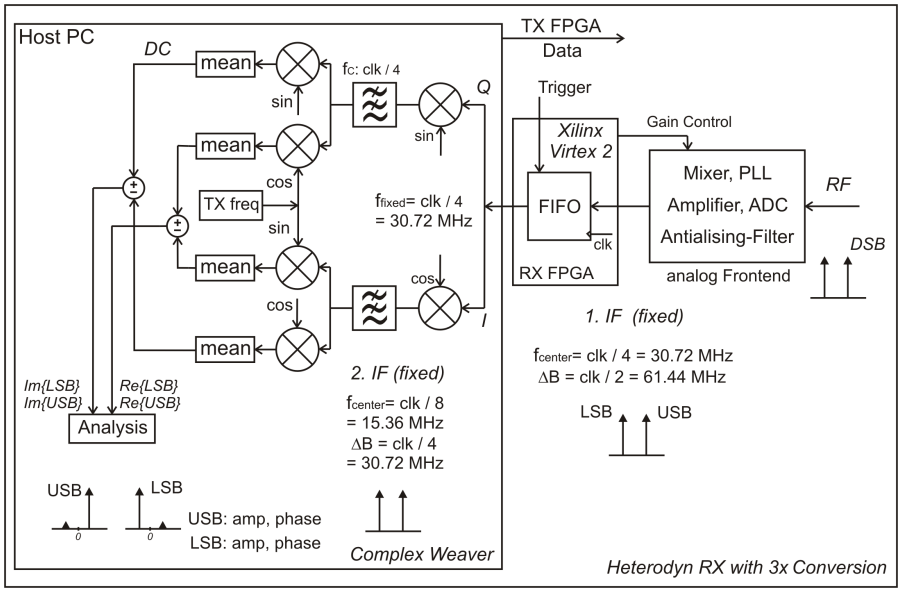

Fig. 7. VSA architecture (Heterodyne) with 3 stage conversion, phase measurement with a Trigger signal.

ADC, operating on the system clock. The samples are stored into a FIFO (RX-FPGA) and the further data processing is realized on a Host-PC. To constantly obtain an optimum dynamic range of the ADC the two VGAs are controlled by the RX-FPGA. To reduce the hardware complexity the receiver is designed as a single channel receiver, without an additional reference channel, which is usually implemented if precise phase measurements are required (as vector network analyzer technique). In the present case the phase measurement is based on the concept of a "digital sampling oscilloscope", where a trigger signal generated by the TX-DDS is used. The disadvantage of this selected architecture is the phase noise of the RX-PLL, which determines the measurement uncertainty. Therefore the PLL requires very low phase noise and averaging in time domain (number of samples) in order to obtain a sufficiently low phase measurement uncertainty.

4.2 Base band architecture/algorithm

The base band algorithm of the receiver with the rf front end is shown in Fig. 7. To determine the SSB suppression of the transmitter a Weaver architecture is selected. This kind of signal processing results in separated complex lower and upper sideband information (amplitude, phase) over a bandwidth of more than 50 MHz.

The fixed digital mixing frequency for the second down conversion is clk/4 (30.72 MHz). The mixing operation can be realized with an efficient multiplexer instead of performing a multiplication operation. Behind the mixing stage an efficient half band filter (fc = clk/4) is implemented, which removes mixing images. The third frequency translation is a homodyne down conversion. The required mixing frequency is exactly known from the TX-DDS and a carrier recovery loop is not required. After the last frequency down conversion the average over all RX-samples is performed. The average operation corresponds to a low pass filtering, which improves the measurement uncertainty due to rejecting of the AC components, like phase noise and remaining mixing signal components. Furthermore the implementation of a frequency adaptive low pass filter after the third mixing stage is circumvented.

4.3 RX-performance

For the TX and RX the PLLs were designed with a fixed frequency and coupled to the same system clock reference. The phase noise at 1 KHz offset was measured as -95 dBc at a carrier frequency of 2.14 GHz. This corresponds to a rms phase deviation of 0.65°. The peak-peak phase uncertainty can be approximated with a Gaussian noise distribution, which gives a phase uncertainty of about 4.5° ($7 \times 0.65°$) for one measurement sample. Figures 8 and 9 plot the measured maximum amplitude and phase uncertainties as functions of the number of samples used for the averaging operation. It can be deduced, that by increasing of the number of samples both uncertainties will tend to approach a value of zero, as expected. Practically 8192–16384 samples are used. This results in a satisfying amplitude and phase measurement uncertainty. Therefore the RX-FIFO depth requirements can be defined to have a size of about 16384 samples using a 14 bit amplitude resolution (14 bit ADC).

Figure 10 plots the investigation of nonlinear properties of the wideband receiver with a 2 tone test signal, measured in the digital domain. The key parameter like IMD3, S/N and harmonics can be deduced. The nonlinear performance data are summarized in Table 1. The amplitude/phase frequency

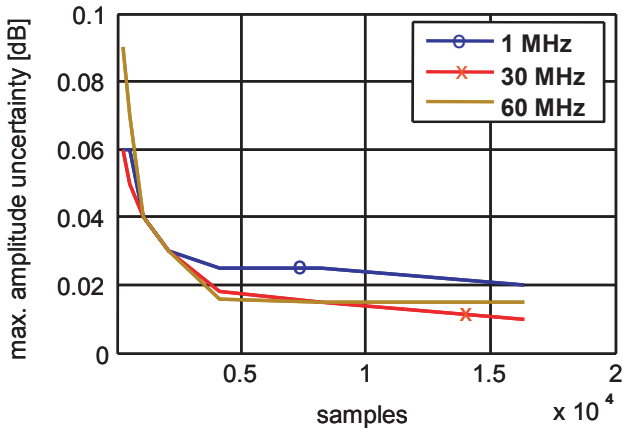

Fig. 8. Amplitude uncertainty vs. number of samples.

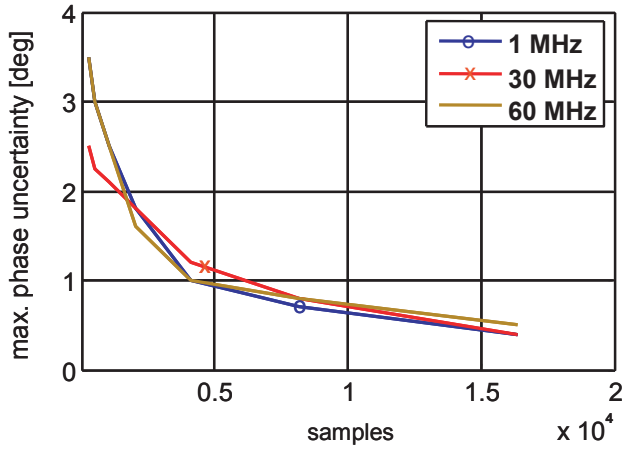

Fig. 9. Phase uncertainty vs. number of samples.

Table 1.

P_{in} for ADC drive, power control loop	-16 ...	-32 dBm
1 dB bandwidth	>	50 MHz
signal / harmonics, 2. order	>	65 dB
signal / harmonics, 3. order	>	65 dB
signal / IM3, spurious	>	65 dB
signal / noise	>	70 dB
within of 60 dB signal dynamic: ampl. uncertainty, pk-pk	<	0.5 dB
phase uncertainty, pk-pk	<	1°

response of the receiver can be corrected with an equalization algorithm. The amplitude frequency response is measured and modelled by means of an FIR filter. Then an inverse function, again a FIR filter, can be implemented equal-

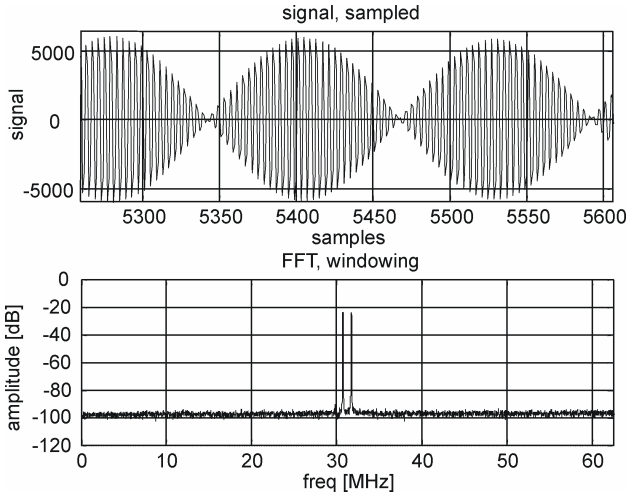

Fig. 10. RX 2 tone performance, time domain and frequency spectrum representation.

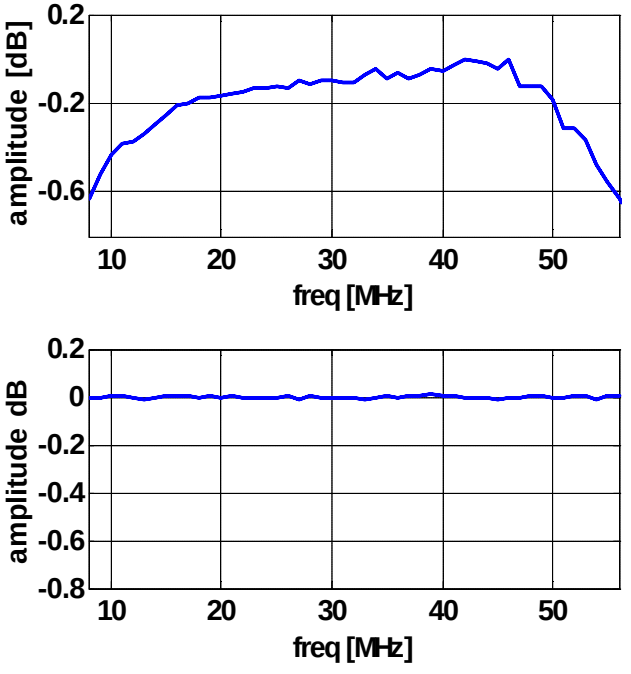

Fig. 11. Amplitude-frequency response of the RX VSA before and after channel equalization.

izing the amplitude frequency response. The FIR filter has the advantage of having absolute stability and a linear phase response, but the required order of the filter can increase dramatically. Furthermore the equalization accuracy is limited. Figure 11 shows the amplitude frequency response before and after equalization over a bandwidth of about 50 MHz. In addition group delay distortions mainly introduced by analogue filters can be compensated with all-pass networks.

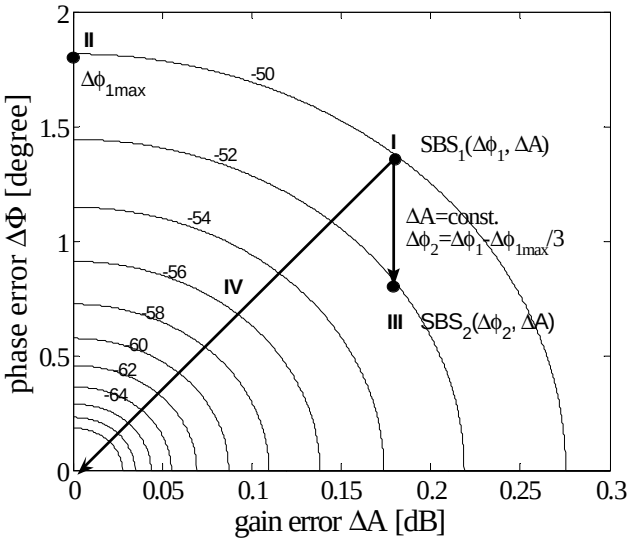

Fig. 12. SBS algorithm with amplitude- and phase dependency.

5 TX single-sideband-suppression (SBS) algorithm

5.1 General

Due to the amplitude/phase frequency response of the directional couplers as well as the subsequent circuitry (e.g. switches) the measurement signal will be falsified. A precise adjustment of the SSB signals will not be possible. It is, however, possible to determine complex values for readjustment of the SSB signal by applying an analytical approach, which requires the measurement of the SSB suppression (SBS) only. Then the amplitude and phase balance can be obtained by adjusting the TX-DDS. With this algorithmic approach the SBS virtually obtains independency of the complex frequency response of the measurement circuit and measurement accuracy. The measurement error, which may be expressed through a possible amplitude deviation between the two SSB signals (LSB, USB) at their two frequencies, defines the maximum possible adjustment uncertainty. As an example, if an amplitude deviation (introduced by the measurement circuit) between the LSB and USB signal of 3 dB occurs and the algorithm tries to adjust the SBS to be -70 dB, then the SBS can only achieve -67 dB as a worst case, that is 3 dB less than the target value. This 3 dB is already a quite large variance in the amplitude frequency response of practical circuits, but the impact of this variance to the resulting SBS is quite small. Furthermore this algorithm does not depend upon the phase/frequency response. Knowledge of the phases of the LSB and USB signals is also not required. As a consequence the technical requirements to be put on the coupling circuitry of the measurement circuit can be advantageously reduced.

5.2 SBS-algorithm

The algorithm is demonstrated in Fig. 12 with some simplification. It can be observed, that e.g. -60 dB SBS requires the amplitude error to be less than 0.1 dB and the phase error to be less than 0.6°. The idea behind the SSB algorithm is to determine the absolute complex operating point first. This corresponds to the actual SBS (I). This is achieved by applying a well defined operating point deviation through adjustment of the TX-DDS. To succeed, two scalar measurements of the SBS (I, III) and a well defined phase adjustment at the TX-DDS (III) are required. Four solution quadrants exist. As a first step the channel having the lower power will be detected. This results in a simplification to two solution quadrants on the right side. The initial SBS (I) is measured. Then a well defined change of the phase in one channel via TX-DDS is applied. To estimate the phase step the corresponding maximum phase error $\Delta\phi_{1max}$ (II) is calculated from:

$$\Delta\phi_{1\,\max} = \arccos\left(\frac{SBS\cdot\left(1+\Delta\mathrm{A}^2\right)-\Delta\mathrm{A}^2-1}{2\cdot\Delta\mathrm{A}\cdot(1+SBS)}\right) \qquad (1)$$

with $\Delta\mathrm{A} = 1$.

A phase change by the well defined value of $\Delta\phi_{1max}/3$ is now applied to of one of the TX-DDSs and a second measurement of the SBS (III) is carried out. The phase step is empirically adjusted to 1/3, but can be chosen freely. From the two SBS measurements two equations with two unknowns can be derived

$$SBS_{1,2} = \frac{1+2\Delta\mathrm{A}\cos\left(\Delta\phi_{1,2}\right)+\Delta\mathrm{A}^2}{1-2\Delta\mathrm{A}\cos\left(\Delta\phi_{1,2}\right)+\Delta\mathrm{A}^2}. \qquad (2)$$

From Eq. (2) a bi-quadratic polynomial equation is obtained

$$\Delta\mathrm{A}^4 + q\,\Delta\mathrm{A}^2 + 1 = 0, \qquad (3)$$

which delivers two positive solutions for ΔA (negative values for ΔA are not meaningful). The two solutions are reciprocal to eachother. The one, which is less than 1, is kept, because the solution quadrant is known.

The following equation has to be solved

$$\Delta\mathrm{A} = \sqrt{-1+\frac{2T^2R^2\sin^2(\Delta\phi_s)}{R^2+S^2T^2-2RST\cos(\Delta\phi_s)} - \sqrt{\left(1-\frac{2T^2R^2\sin^2(\Delta\phi_s)}{(R^2+S^2T^2-2RST\cos(\Delta\phi_s))}\right)-1}}$$

with

$$R = (1+SBS_2)\,, \qquad S = (SBS_2-1)\,,$$
$$T = \frac{SBS_1+1}{SBS_1-1}, \qquad \Delta\phi_s = \frac{\Delta\phi_{1\,\max}}{3} \qquad (4)$$

The channel having the higher power will now be multiplied with the solved ΔA. The corresponding phase $\Delta\phi_1$ can be determined from Eq. (5):

$$\Delta\phi_1 = \arccos\left(\frac{\left(\Delta\mathrm{A}^2+1\right)(SBS_2-1)}{2\mathrm{A}\,(1+SBS_2)}\right) - \Delta\phi_s \quad . \qquad (5)$$

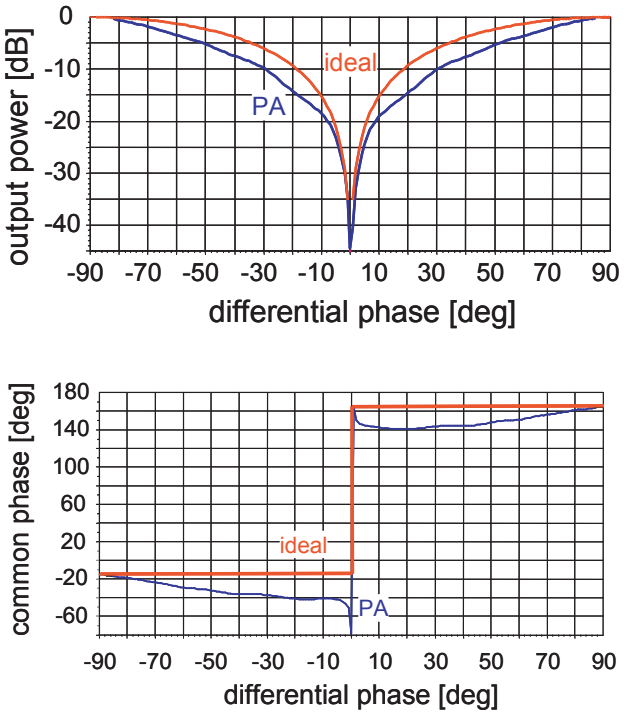

Fig. 13. Simulated distortions of the outphasing PA at 2.14 GHz, **(a)** output power, **(b)** output common phase vs. differential phase.

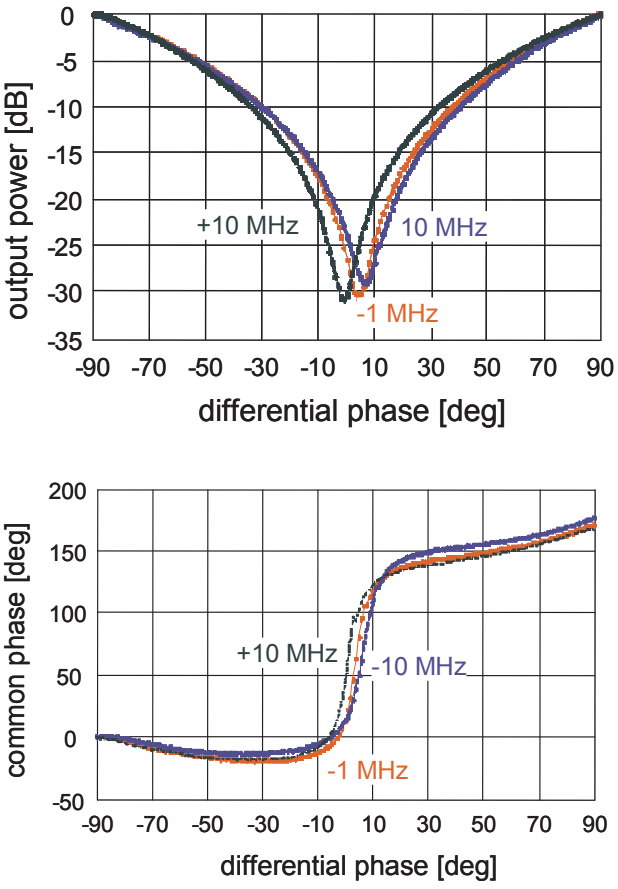

Fig. 14. Distortions of the outphasing PA at 2.14 GHz, **(a)** output power, **(b)** output common phase vs. differential phase and frequency offset.

Finally the phase of one channel can be corrected with the TX-DDS and the SBS becomes perfectly adjusted (IV).

Due to measurement and calculation inaccuracies the algorithm has to be repeated iteratively. If a SBS < -70 dB is achieved the iteration loop is stopped. Usually only a few iteration cycles are necessary.

6 PA distortion and predistortion

6.1 PA transfer characteristics

Figure 13 shows a simulation plot of the output power behaviour and the common phase distortions of the outphasing PA as functions of the differential phase (simulations with ADS, agilent). The output power drops down more rapidly than expected and the common phase does not stay constant, which is caused by the directive output coupling of the power transistors and their behaviour as real voltage sources in saturation. It also can be deduced, that two possible solution areas exist to the left and right to the location of the zero. This is interesting, because the transfer characteristics as well as the related PA efficiencies are not symmetric. Hence characteristic which suits best (left or right) should finally be chosen with respect to the predistortion algorithm. The presence of a signal distortion can already deduced from the simulation results. Therefore the evaluation of the PA transfer characteristics is necessary. It was and should be determined through practical in-circuit measurements. During the practical measurements the SSB signals were generated first and adjusted. Then the differential phase between the 2 SSB carriers was swept and the output power and common phase were measured. Figure 14 plots the measured characteristics. The frequency offset was also varied.

Furthermore, for defining the starting point of a predistortion, a reference point has to be devised as the absolute differential phase angle for maximum or minimum power. In Figs. 13 and 14 the derived characteristics are already normalized to this point and represent relative curves. The practical measurements were performed with an angle resolution of 1°. From the measured amplitude curve the zero depth can be deduced. It is approximately -30 dB, which is good practical value. A perfect vector cancellation and a perfect zero can not be obtained due to asymmetries of the practical PAs. If the measured data are compared with the simulated data, a quite fair agreement between both can be deduced. The differential phase for the -10 dB output power back off can be determined as -30° for both cases. The output phase versus differential phase is decreasing on the left and increasing

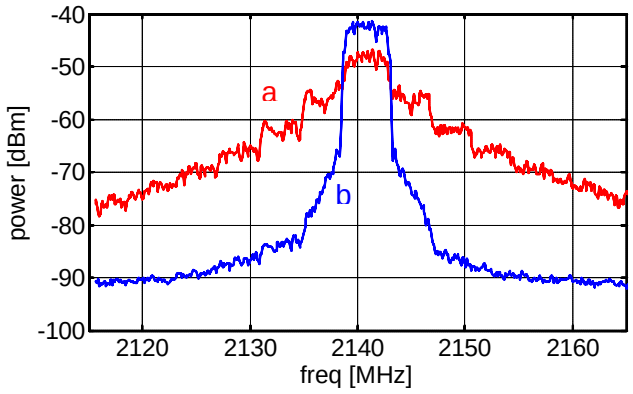

Fig. 15. Effect of phase calibration, PA output spectrum **(a)** without a phase calibration, **(b)** phases of the branches are adjusted.

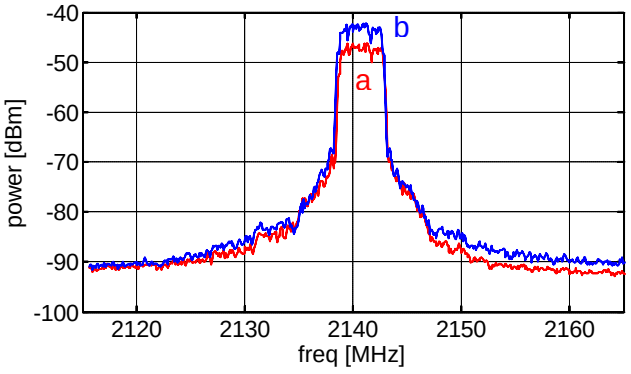

Fig. 16. Effect of "phase only" predistortion, PA output spectrum **(a)** without predistortion, **(b)** with predistortion.

on the right (Fig. 14b). The measured 180° phase jump is not distinct (Compare fig. 13b). This behaviour can be explained by the non perfect amplitude zero, which is -30 dB.

Additionally it can be seen, that the PA transfer characteristics are frequency dependent.

6.2 "Phase Only"- predistortion - algorithm

The derived static PA transfer characteristics as functions of the input differential phase have to be compensated with a predistortion algorithm. The mathematical representation of a so called "phase only"-predistortion algorithm is shown in Eq. (6).

$$
\begin{aligned}
&A_{out} = f_1(\Delta\varphi);\ \varphi_{out} = f_2(\Delta\varphi)\\
&A_{out}(t) = f_1(\Delta\varphi(t)) = Gain \cdot A_{in}(t)\\
&\Delta\varphi(t) = f_1^{inv}(A_{in}(t))\\
&\varphi_{common}(t) = -\varphi_{out}(t) + \varphi_{in}(t) = -f_2(\Delta\varphi(t))\\
&\varphi_{common}(t) = -f_2(f_1^{inv}(A_{in}(t))) + \varphi_{in}(t) \qquad (6)
\end{aligned}
$$

From the measured output power curve a new corresponding input differential phase can be derived with the inverse function

$$\Delta\varphi(t) = f_1^{inv}(A_{in}(t)) \qquad (7)$$

With the newly determined differential phase the common phase distortion can be deduced and compensated. The PA characteristics are present as a LUT. To determine the inverse function the columns of the LUT have to be interchanged. Missing LUT points have to be interpolated. The two newly derived LUTs addressing the predistortion on the differential phase and on the common phase are implemented into the TX base band FPGA (see Sect. 3.2).

6.3 "Phase Only"- predistortion - measurement results

As a dynamic test signal a single WCDMA channel with a pseudo-noise QPSK signal and a peak to average ratio (PAR) of about 5 dB was used. If the outphasing PA is driven without any calibration/predistortion the output spectrum will not restore the single WCDMA channel by having the shape of the input signal, but the broadband phase modulation of the input constant envelope signal will appear at the PA output. This effect can be seen in Fig. 15a. A huge bandwidth is required (defined by the TX). Even with the developed RX architecture with a bandwidth of about 50 MHz a correct measurement without aliasing would not be possible, as mentioned earlier. A large receiver bandwidth is necessary to characterize dynamic PA distortions for single and multicarrier signals, the treatment of which is not in the scope of this paper. However if the TX branches (IQ-mixers, 2 outphasing channels) are adjusted (calibrated) by only using the phase offset a predominant restoration of the channel can be observed (Fig. 15b), accompanied by a reduction of the bandwidth of the signal. But the signal is still blurred due to the distortions arising from the outphasing transfer characteristics. Also the measured output power is too small. It is interesting to see, that the WCDMA channel is clearly restored, taking the distorted PA transfer characteristics into account.

In a next step a static predistortion was investigated. The result is shown in Fig. 16. It can be recognized, that the output power is increased by about 4 dB. This can be explained by the predistortion of the amplitude characteristic. The PAR of the signal is about 5 dB with a sharp power distribution at a power back off of -5 dB. The power increase is just the difference between the ideal and real PA curves at a back off power of -5 dB. This can be evaluated from Fig. 13a. The "back off"-operating point of -5 dB on the ideal (assumed) curve can be found at a differential phase of about -35°. The corresponding real PA behaviour for this differential phase is about 4 dB less (-9 dB), which explains the lower measured power of the channel at the beginning, without predistortion. The full expected output power of the channel could be obtained with the effect of amplitude predistortion.

However, the related linearity improvement is comparatively small. It is assumed, that due to the frequency depen-

dence of the PA distortions and the wide bandwidth requirement of the outphasing approach a perfect vector cancellation can not be obtained with a static (one frequency) distortion characterisation. Therefore dynamic techniques, considering the whole outphasing bandwidth has to be developed and applied, which is in the scope for further research.

7 Conclusion

A powerful, configurable, software defined transmitter/ receiver architecture is proposed for application with PAs using the outphasing concept. Such an approach is interesting, because it has the potential of facilitating the trade off between linearity and efficiency of PAs in WCDMA base stations. A complex TX/RX system is necessary for providing the differential phase modulation in order to drive the outphasing 3 port PA, to determine the system distortions and to apply a calibration and a predistortion algorithm. An almost error-insensitive and efficient DSP algorithm is described, which enables the generation of precise SSB signals. SSB signals (CW) are used for measuring the distorted complex transfer characteristics. The proposed vector receiver architecture offers a simple solution having a large bandwidth. Phase measurements are performed with a Trigger signal generation of the TX-DDS and an averaging operation to reduce measurement uncertainties. The measured complex transfer characteristics are confirming the simulation results. A predistortion algorithm based on the static distortion characterisation was derived and implemented into a TX-FPGA. Further subject of research will be the development and application of dynamic (broadband) distortion characterisation for further linearity improvement.

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