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LNA for Low-Power, Low Data Rate PAN Applications

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Abstract. In this paper a common-gate LNA is presented, which is used in a low-power IEEE 802.15.4 receiver with severer requirements on the current consumption. The LNA is designed in a 0.25 μm CMOS technology and consumes only 831 µA. The LNA achieves a voltage gain of 12.89 dB, a NF of 4.86 dB, and an IIP3 of -6.0 dBm.

1 Introduction

There are a variety of wireless communication systems, which can be distinguished in terms of their system features. The new IEEE 802.15.4 standard - ZigBee (Zig) is intended for communication systems with low data rates, allowing reduced protocols and short duty cycles. Therefore, it is especially qualified for wireless senor networks. In comparison to other systems like UMTS, GSM or GPS, ZigBee has a smaller RF-bandwidth and is intended for a communication range up to 100 m. In contrast, other systems have a higher RF-bandwidth and a communication range of a few kilometers up to a distance from satellite to earth.

The system requirements in terms of linearity (3rd order intercept point - IIP3) and noise (noise figure - NF) must be determined. According to the complexity of a wireless system, this should be done by a proper system simulation (Stücke et al., 2005). Based on the system simulation, it can be shown that the linearity and noise figure requirements are much lower than for other communications systems. For these relaxed requirements, a battery lifetime of up to two years becomes feasible for a IEEE 802.15.4 receiver, whereas for GSM or UMTS it is difficult to achieve larger battery lifetime than one week.

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2 LNA architecture

There are two basic topologies for LNA (Lee, 2004; Razavi, 1998), either common-source (CS) or common-gate (CG) configurations. The CS-LNA, depicted in Fig. 1(a), provides the 50 Ω input impedance Z_{in} by inductive degeneration. The input impedance are tuned to the desired carrier frequency f_0 and can be determined as

$$Z_{in} = \frac{g_m \cdot L_s}{C_{gs}} = \omega_T \cdot L_s = 2\pi \cdot f_T \cdot L_s \ , \tag{1}$$

where f_T is the transit frequency, L_s the source inductor, g_m the transconductance and C_{gs} the gate source capacitance of the MOSFET. The inductor at the drain terminal resonates with the parasitic capacitances of the MOSFET and the inductor itself and the input capacitor of the following circuit (mixer) at the desired carrier frequency f_0. The resulting equivalent resistance R_P of the resonance circuit can be determined for this frequency. Hence, the voltage gain G_V can be expressed as

$$G_V = \left| \frac{v_{out}}{v_{in}} \right| \approx \frac{R_P}{R_s} \cdot \frac{\omega_T}{\omega_0} \ , \tag{2}$$

where R_s is the source impedance (normally 50 Ω). Since f_T is proportional to the bias current, a decrease in bias current will result in a decrease in gain. To tune the Z_{in} to 50 Ω L_s must be adjusted.

In contrast, the voltage gain of the CG-LNA (depicted in Fig. 1(b)) becomes

$$G_V = \left| \frac{v_{out}}{v_{in}} \right| = g_{ms} \cdot R_P \tag{3}$$

and the input impedance is approximately equal to

$$Z_{in} \approx \frac{1}{g_{ms}} \ , \tag{4}$$

where g_{ms} denotes the drain-source transconductance of the MOSFET as proposed in Enz et al. (1995). A decrease in bias

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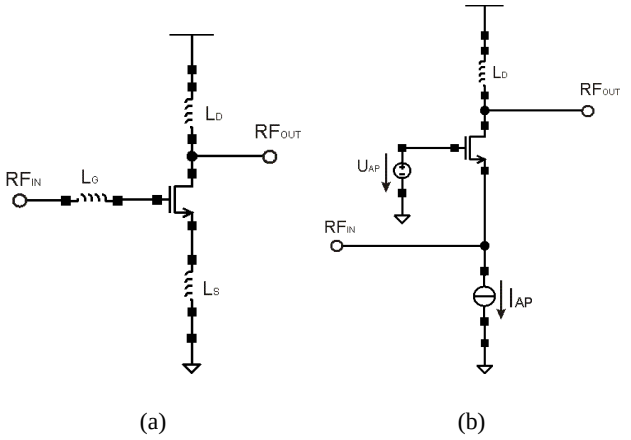

Fig. 1. Principle LNA architectures: **(a)** common-source LNA and **(b)** common-gate LNA.

current also results in a decrease in G_V, but in an increase in the Z_{in}. Therefore, an appropriate bias current must be chosen.

As defined in Shaeffer and Lee (1997), the noise factor F_{CS} of the CS-LNA can be calculated from

$$F_{CS} \approx 1 + \frac{\gamma}{\alpha} \cdot \frac{1}{Q_{in}} \cdot \Psi_{CS} \cdot \frac{\omega_0}{\omega_T} , \quad (5)$$

where γ is the drain noise factor of the MOSFET and Ψ_{CS} describe the portion of the induced gate noise. The other terms are $Q_{in} = 1/\omega_0 C_{gs} R_s$ and $\alpha = g_m/g_{d0}$, with g_{d0} is the zero-bias drain conductance.

In contrast, the noise factor of the CG-LNA can be determined as (Shaeffer and Lee, 1997)

$$F_{CG} \approx 1 + \frac{\gamma}{\alpha} . \quad (6)$$

The noise figure of the CS-LNA is bias-dependent, since it is a function of the bias-dependent f_T as shown by Eq. (5). According Eq. (6), the noise figure of the CG-LNA is bias independent in a first order approximation. Thus, the noise factor (F_{CS}) of the CS-LNA is a linear function of the ratio f_0/f_T, while it is constant with respect to it for the CG-LNA (Allstot et al., 2004). For large values of this ratio, the CG-LNA outperforms the CS-LNA in terms of the noise figure. However, for low bias currents, the f_T becomes low and, hence, the ratio f_0/f_T becomes large. Therefore, the CG-LNA is more suitable for relaxed noise figure requirements but tough demands for low current consumption. But in practice the behavior is more complicated.

3 Operating point of the CG-LNA

3.1 Operation of the MOSFET in moderate inversion

The different modes of operation of the MOSFET in saturation can be defined according to the EKV-model (Enz et al., 1995) as weak, moderate and strong inversion. The mode of operation can be expressed in terms of the inversion coefficient i_f which is the ratio of drain current I_D to specific current I_S in saturation. For $i_f < 0.1$ the MOSFET operates in weak inversion, for $0.1 \leq i_f \leq 10$ in moderate inversion and for $i_f > 10$ in strong inversion as shown in Fig. 2.

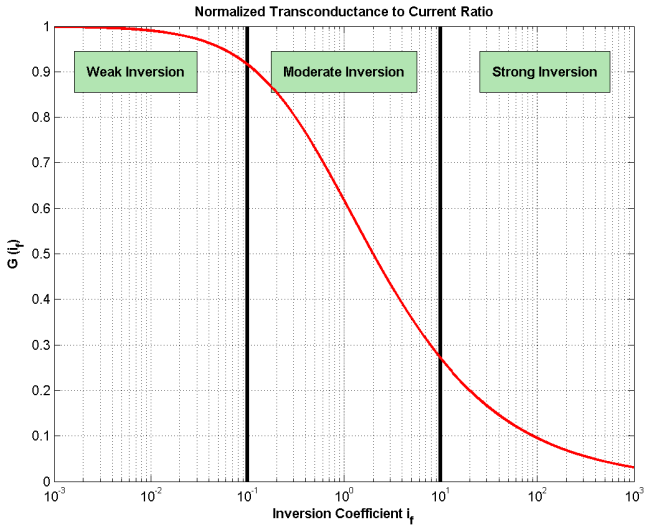

Fig. 2. Normalized transconductance to drain current ratio.

The ratio of source transconductance g_{ms} to drain current I_D is called tranconductance efficiency. In weak inversion this ratio is as large as for bipolar devices, whereas it is low in strong inversion. The transition between both is in the moderate inversion and is described by the normalized transconductance to drain current ratio (depicted in Fig. 2) in accordance to Enz and Cheng (2000)

$$G\left(i_f\right) = \frac{2}{1 + \sqrt{4 \cdot i_f + 1}} . \quad (7)$$

Moving the operating point from strong inversion to moderate inversion has the advantages of higher tranconductance efficiency and lower electrical fields inside the MOSFET (Enz and Cheng, 2000). Due to this, no velocity saturation effect as well as no hot electron effects arises and, hence, lower excess noise is obtained. The disadvantage is the higher nonlinearity due to the exponential behavior of drain current in weak inversion.

3.2 Selection of the operating point and biasing

As discussed in Sect. 3.1 it is advantageous to bias the LNA in moderate inversion. Furthermore, the input impedance of the CG-LNA must be equal to 50 Ω and can be calculated from

$$Z_{in} = \frac{1}{g_{ms} + sC_{gs}} . \quad (8)$$

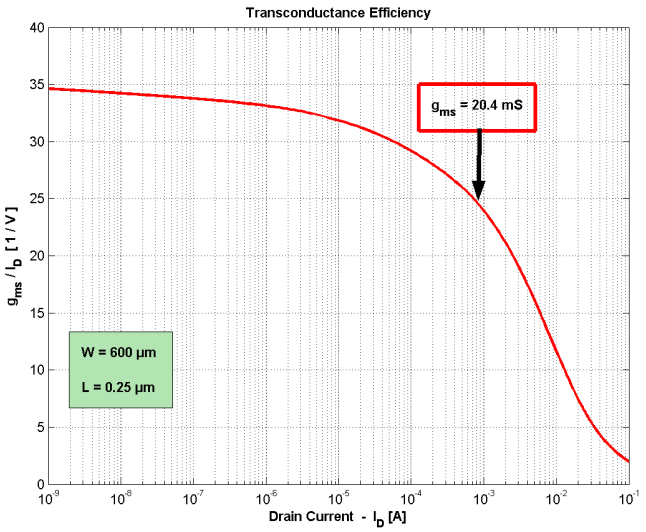

Fig. 3. Transconductance efficiency.

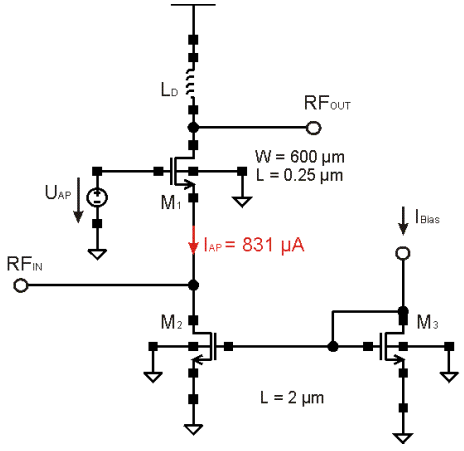

Fig. 4. Schematic CG-LNA.

The imaginary part (ωC_{gs}) of the denominator must be sufficiently low compared to the real part (g_{ms}). Consequently, $g_{ms} \approx 20\,\mathrm{mS}$ must be chosen in a first order approximation. Note, that in practical designs g_{ms} deviates from 20 mS, since bondwire and pad parasitics cause a small impedance change.

A circuit simulation can determine the most suitable transistor size. Fig. 3 depicts the cadence simulation result of a MOSFET with $W = 600\,\mu\mathrm{m}$ and $L = 0.25\,\mu\mathrm{m}$. A bias current of 831 µA allows a transconductance of 20.4 mS. Furthermore, this operating point is located in the moderate inversion region.

The schematic of the CG-LNA is shown in Fig. 4. The inductor at the drain of the LNA-MOSFET M1 resonates with the input capacitor of the following circuit (mixer) at the desired carrier frequency. The bias current is supplied via the current mirror, composed of the MOSFETs M2 and M3. Since the MOSFET M2 should emulate an ideal current source (compare Fig. 1(b)), its output resistance should as large as possible. To fulfill this requirement, the channel length of the current mirror is chosen much larger than the minimum channel length, since the output resistance decreases dramatically for short channel MOSFETs.

4 Noise of the CG-LNA

4.1 Noise in moderate inversion

The drain noise factor γ of long channel MOSFETs in saturation was calculated by van der Ziel (1970) to $\gamma = 2/3$. Several measurements of short channel MOSFETs were published by various authors, e.g. Abidi (1986); Knoblinger et al. (2000); Scholten et al. (2003), which show an increase of γ over 2/3. Furthermore, γ exhibits a bias dependence. Various theories about this excess noise in short channel MOSFETs exists. Unfortunately, most of them are not dedicated to the moderate inversion region or still unsuitable for hand calculations.

Klein (1998) proposed a model for the thermal noise, which accounts for velocity saturation and hot carrier effects. The model was originally developed for a MOSFET biased in strong inversion and extended by Enz and Cheng (2000), to cover the whole region from weak to strong inversion. The noise parameter γ for a long channel MOSFET in saturation can be expressed as

$$\gamma_{sat-long} = \frac{2}{3} \cdot \left(1 + \frac{1 - \sqrt{4 \cdot i_f + 1}}{8 \cdot i_f} \right) . \qquad (9)$$

It depends on the inversion coefficient i_f and converges to 1/2 for low values of i_f in weak inversion region and converges to 2/3 for large values of i_f in strong inversion. The transition between both occurs in the moderate inversion and is presented in the upper curve of Fig. 5. The short channel γ can be calculated from

$$\gamma_{sat}\left(i_f\right) = \gamma_{sat-long} \cdot \left(1 + \frac{1}{G\left(i_f\right)} \cdot \frac{\theta_{sat} \cdot \tau_r}{L_{eff}} \right) , \qquad (10)$$

where L_{eff} denote the effective channel length, θ_{sat} the saturation velocity and τ_r the relaxation time. The resulting curve is depicted in the lower curve of Fig. 5 with the typical values $\theta_{sat} \approx 10^5\,\mathrm{m\,s^{-1}}$ (Lee, 2004) and $\tau_r \approx 1\,\mathrm{ps}$ (Enz and Cheng, 2000) and $L_{eff} = 0.25\,\mu\mathrm{m}$. From this figure the dramatical increase in strong inversion can be seen as well as convergence to $\gamma = 0.7$ in weak inversion. In the middle of moderate inversion only a low increase to $\gamma = 0.93$ can be observed. This indicates the advantage of biasing the MOSFET in moderate inversion.

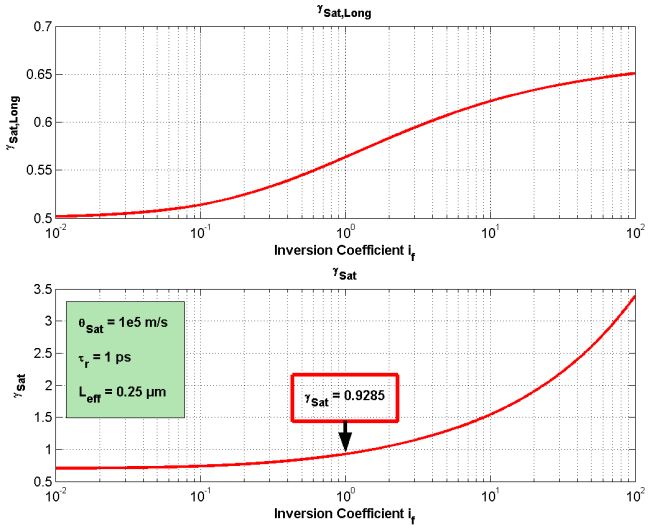

Fig. 5. Drain noise factor in dependence of inversion coefficient.

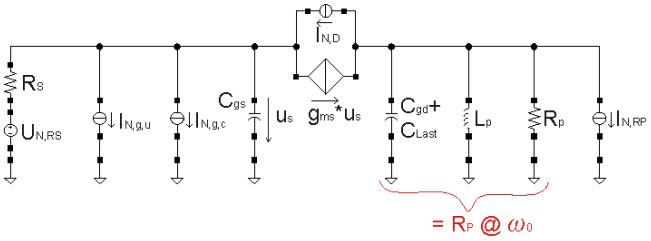

Fig. 6. Equivalent circuit CG-LNA for noise figure calculation.

4.2 Noise figure calculation

The noise figure can be calculated based on the equivalent circuit depicted in Fig. 6. The resonant circuit at the drain is tuned to the desired carrier frequency f_0 as described in Sect. 2. Therefore, only the resistor R_P which models the tank losses in a parallel equivalent circuit is used in the following noise calculation.

It is very important to note that in Eqs. (5) and (6), the noise contribution from the load R_P is neglected. This is a common way in the literature, but it is valid theoretically only, if the load and thus the gain approaches infinity. Since the LNA needs a finite load impedance to achieve a voltage gain, NF calculations must consider it.

The different noise sources are the thermal noise of R_P and R_s, the drain noise source and the induced gate noise source which is partly correlated with the drain noise. The noise sources can be described by (Shaeffer and Lee, 1997)

$$\overline{u_{R_s}^2} = 4kTR_s \cdot \Delta f \tag{11}$$

$$\overline{u_{R_P}^2} = 4kTR_P \cdot \Delta f \tag{12}$$

$$\overline{i_d^2} = 4kT\gamma g_{ms} \cdot \Delta f \tag{13}$$

$$\overline{i_{g,u}^2} = 4kT\delta g_g \cdot \left(1 - |c|^2\right) \cdot \Delta f \tag{14}$$

$$\overline{i_{g,c}^2} = 4kT\delta g_g \cdot |c|^2 \cdot \Delta f \ , \tag{15}$$

with $g_g = \omega C_{gs}/5g_{ms}$ and $c = -j\,0.395$ for long channel MOSFET in saturation (Shaeffer and Lee, 2005).

The impact of distributed gate resistance R_G (Razavi et al., 1994) is reduced, since multifinger gates are used and contacted from both sides. Furthermore, R_G can be reduced by using silicided polysilicon with low resistivity. Hence, R_G becomes small enough to be neglected in the noise figure calculation.

The resulting noise factor is provided by Eq. (16) and can be calculated with the equivalent circuit Fig. 6 and with the Eqs. (11) – (15). Since the sum in Eq. (16) is contributed by the LNA-MOSFET itself and by the load, it can be rewritten as Eq. (17).

$$F_{CG} = 1 + \gamma \frac{1}{g_{ms}R_s}\left(1 + \frac{1}{Q_{in}^2}\right)\Psi_{CG} + \frac{R_p}{R_s}\frac{1}{|G_v^*|^2} \tag{16}$$

$$F_{CG} = 1 + (F_{MOST} - 1) + (F_{load} - 1) \tag{17}$$

$$\Psi_{CG} = 1 + \frac{1}{Q_{in}^2 + 1}\left\{\frac{\delta}{5\gamma} - 2\,|c| \cdot \sqrt{\frac{\delta}{5\gamma}}\right\} \tag{18}$$

$$|G_v^*|^2 = \frac{g_{ms}^2 \cdot R_p^2}{\left|1 + g_{ms}R_s + sC_{gs}R_s\right|^2} \tag{19}$$

The portion of the induced gate noise is described by Eq. (18). Note, that it is different to Ψ_{CS} of the CS-LNA in Eq. (5). The expression $G_v^* = \left|\frac{v_{out}}{v_0}\right|$ in Eq. (19) denotes the gain with respect to the voltage v_0, which is located inside the 50 Ω source at the input of the LNA. In contrast to the common definition of voltage gain Eq. (3), it comprises also the input impedance Z_{in} in the denominator.

With numerical values one gets $Q_{in} \approx 6$, $g_{ms}R_s \approx 1$ because of the required input matching, $\Psi_{CG} \approx 1$ and $\frac{R_p}{R_s}\frac{1}{|G_v^*|^2} \approx 0.8$. Note at first that $\Psi_{CG} \approx 1$ shows clearly, that the induced gate noise has only a very little influence. Secondly, note that the large contribution of the load has a dramatic influence to the whole noise figure as discussed above. The result of the noise calculation is $F_{CG} = 2.49$ with $\gamma = 2/3$ and $F_{CG} = 2.73$ with $\gamma = 0.9$ if an increased γ is assumed according to Sect. 4.1.

If we consider additional noise sources e.g. from the resistive part of the pad and bondwire or from the biasing circuit, Eq. (17) can be rewritten as

$$F_{CG} = 1 + (F_{MOST} - 1) + (F_{load} - 1) + (F_{others} - 1) \ . \tag{20}$$

Unfortunately, the BSIM 3.3 model used in the simulation does not allow for the bias dependence of the noise. The

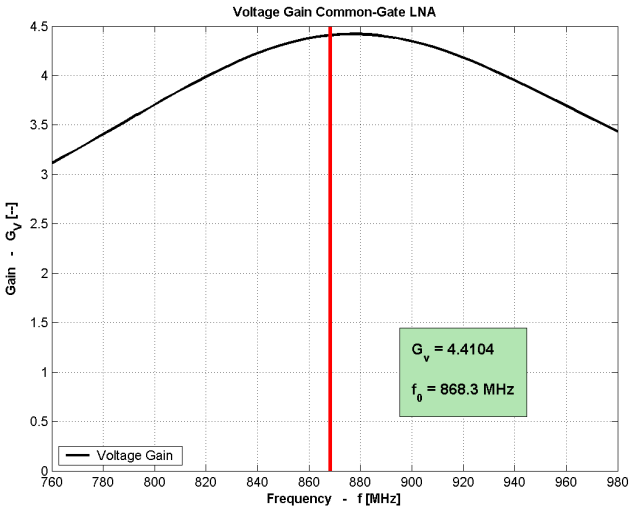

Fig. 7. Simulation result: voltage gain of the CG-LNA.

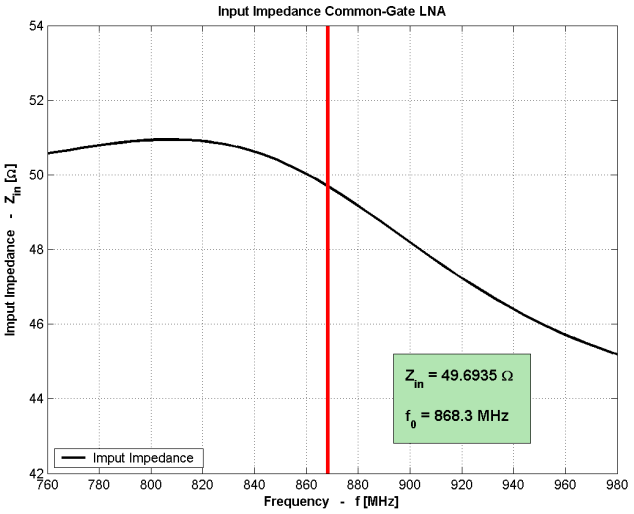

Fig. 8. Simulation result: input impedance of the CG-LNA.

circuit simulation is carried out with a $\gamma = 2/3$. The "real" value can be estimated with

$$F_{CG} = 1 + \frac{\gamma_{real}}{\gamma_{Simu}} \cdot (F_{MOST} - 1)|_{Simu} + (F_{load} - 1) + (F_{others} - 1) \ . \quad (21)$$

This stems from the assumption that only the LNA-MOSFET is affected by the higher γ value. Therefore, the simulation results can be corrected.

5 Simulation results

The circuit simulation is performed using Cadence and are based on the BSIM 3.3 MOSFET model. The pad parasitics are modeled as well as the bondwire inductors and accounted for in the simulation.

The inductor was modeled by its π-equivalent circuit with ten elements as described in Long. The parameter of the inductor model can be determined either by separate EM-simulation of the coil or by measurement of the inductor, followed by a parameter fitting.

In Fig. 7, the simulation result of the gain of the CG-LNA is shown. At the carrier frequency (868.3 MHz) the linear voltage gain amounts to 4.41 which is equivalent to 12.89 dB on logarithmic scale.

The simulated input impedance Z_{in} is shown in Fig. 8. The input impedance is close to 50 Ω, since the input reflection coefficient S_{11} is -15.56 dB. The remaining reflection coefficient is due to the parasitic effects of the gate source capacitance, the bondwire and pads.

The simulation result of the noise figure is depicted in Fig. 9. The circuit simulation evaluates a NF of 4.5 dB equivalent to a noise factor of 2.83. This value comprises the contribution from the load as described in Sect. 4.2. The contribution of the other parts is included and can be determined as $(F_{\text{others}} - 1) = 0.34$. As discussed in Sect. 4, the BSIM 3.3 model used in these simulations does not allow for the bias dependence of γ. The expected "real" value can be estimated using Eq. (21) and it amounts to $F = 3.07$ equivalent to a noise figure of 4.86 dB on logarithmic scale. According to the system simulation (Stücke et al., 2005), this suffices to meet the ZigBee requirements.

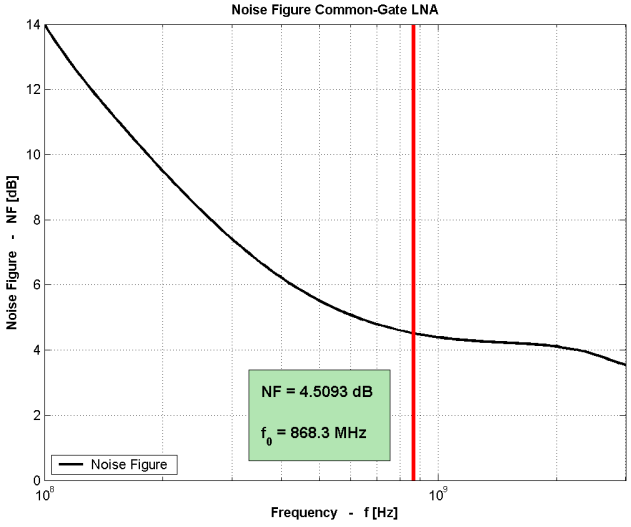

Fig. 9. Simulation result: noise figure of the CG-LNA.

The linearity of the LNA is determined in terms of the IIP3 as the intersection of the 3rd order intermodulation product with the fundamental component. The IIP3 is evaluated at -6.0 dBm as depicted in Fig. 10.

The simulation results of the CG-LNA biased in moderate inversion are finally summarized in Table 1.

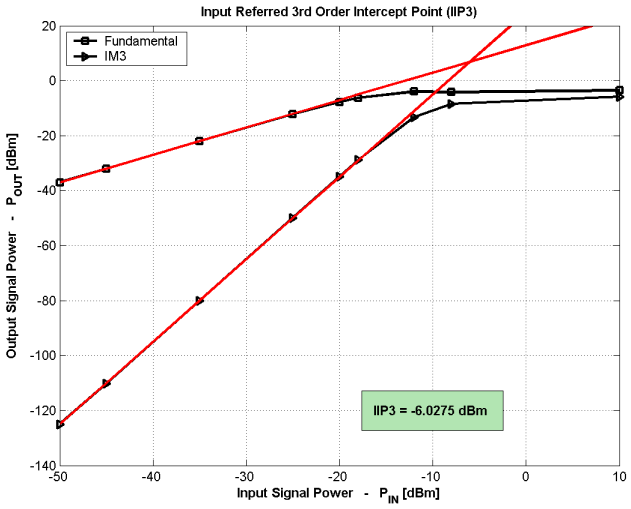

Fig. 10. Simulation result: linearity (IIP3) of the CG-LNA.

6 Conclusions and outlook

The features of the presented CG-LNA are: The LNA operates at a very low current consumption, and external components such as off-chip inductors or matching network are not necessary. The operating of point the MOSFET is moved to the moderate inversion with the above described advantages. The impact of bondwire, and pads are accounted for in the circuit simulation.

The designed CG-LNA is used in our IEEE 802.15.4 (ZigBee) receiver, which is at the moment in production at our 0.25 µm CMOS technology. Measurement results will be presented after the fab-out. A further optimization of Q-factor of the used drain inductor would result in a higher gain with simultaneous noise figure reduction.

Table 1. Simulation results.

CG-LNA Performance Summary Simulation with BSIM 3.3	
Frequency [MHz]	868.3
Voltage Gain [dB]	12.89
Noise Figure [dB]	4.51
Input Refection Coefficient [dB]	-15.56
DC Current [µA]	831
Supply Voltage [V]	2.5
Technology [µm]	0.25 CMOS

References

IEEE Std 802.15.4 -2003, IEEE Standard for Information technology - Telecommunications and information exchange between systems - Local and metropolitan area networks - Specific requirements - Part 15.4: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (WPANs), available in the internet: www.zigbee.org.

Abidi, A.: High-frequency noise measurements on FET's with small dimensions, IEEE Trans. Electron Devices, 33, 1801–1805, 1986.

Allstot, D., Li, X., and Shekhar, S.: Design considerations for CMOS low-noise amplifiers, in: IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, Digest of Papers, 97–100, 2004.

Enz, C. and Cheng, Y.: MOS transistor modeling for RF IC design, IEEE J. Solid-State Circuits, 35, 186–201, 2000.

Enz, C., Krummenacher, F., and Vittoz, E.: An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications, Analog Integrated Circuits Signal Processing, 8, 83–114, 1995.

Klein, P.: An Analytical Thermal Noise Model of deep submicron MOSFET's for Circuit Simulation with Emphasis on the BSIM3v3 SPICE Model, in: Proc. of the 28th European Solid-State Device Res. Conf., 1998, 460–463, 1998.

Knoblinger, G., Klein, P., and Baumann, U.: Thermal channel noise of quarter and sub-quarter micron NMOSFET's, in: Proc. of the 2000 Intern. Conf. on Microelectronic Test Structures ICMTS 2000, 95–98, 2000.

Lee, T.: The Design of CMOS Radio-Frequency Integrated Circuits, Cambridge University Press, Cambridge, New York, Melbourne, Madrid, Cape Town, 2. edn., 2004.

Long, J.: Passive Components and RF IC Design, Advanced Engineering Course on RF IC Design, at the EPFL, Lausanne 4–8 October 2004.

Razavi, B.: RF Microelectronics, Cambridge University Press, Cambridge, New York, Melbourne, Madrid, Cape Town, 1. edn., 1998.

Razavi, B., Yan, R.-H., and Lee, K.: Impact of distributed gate resistance on the performance of MOS devices, IEEE Trans. Circuits and Systems I, 41, 750–754, 1994.

Scholten, A., Tiemeijer, L., van Langevelde, R., Havens, R., Zegers-van Duijnhoven, A., and Venezia, V.: Noise modeling for RF CMOS circuit simulation, IEEE Trans. Electron Devices, 50, 618–632, 2003.

Shaeffer, D. and Lee, T.: A 1.5V, 1.5 GHz CMOS Low Noise Amplifier, IEEE J. Solid-State Circuits, 32, 745–59, 1997.

Shaeffer, D. and Lee, T.: Corrections to "'A 1.5V, 1.5 GHz CMOS Low Noise Amplifier"', IEEE J. Solid-State Circuits, 40, 1397–1398, 2005.

Stücke, T., Christoffers, N., Kokozinski, R., and Kolnsberg, S.: BER Optimization for Micro Power Receivers Using Quick and Accurate System Simulation, in: Proc. of the 14th IST Mobile and Wireless Communications Summit, 2005.

van der Ziel, A.: Noise in solid-state devices and lasers, in: Proc. of the IEEE, 58, 1178–1206, 1970.