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Yield-improving test and routing circuits for a novel 3-D interconnect technology

M. Bschorr[1], H.-J. Pfleiderer[1], P. Benkart[2], A. Kaiser[2], A. Munding[2], E. Kohn[2], A. Heittmann[3], H. Hübner[3], and U. Ramacher[3]

[1]University of Ulm, Microelectronics Department, Albert-Einstein-Allee 43, 89081 Ulm, Germany
[2]University of Ulm, Department of Electron Devices and Circuits, Germany
[3]Infineon Technologies AG, Germany

Abstract. This work presents a system to increase the yield of a novel 3-D chip integration technology. A built-in self-test and a routing system have been developed to identify and avoid faults on vertical connections between different stacked chips. The 3-D technology is based on stacking several active CMOS-ICs, which have through-substrate electrical contacts to communicate with each other. The expected defects of these vias are shorts and resistances that are too high.

The test and routing system is designed to analyze an arbitrary number of connections. The result ist used to gain information about the reliability of the new 3-D processing and to increase its yield. The circuits have been developed in 0.13 μm technology, one chip has been fabricated and tested, another one is in production.

1 Introduction

The recent development in micro- and nanotechnology is not sufficient to meet all the needs of upcoming electronic applications. For instance, the area of mobile communications demands a steadily increasing number of functions which leads to more and more energy and area consumption of integrated circuits. The shrinking of the technology alone is not able to compensate these drawbacks. Typical tasks are en- and decoding of video signals, multi-mega-pixel cameras, interactive mobile games or visual telephony. Standards like UMTS, WLAN or HiperLAN offer the required bandwidth and have to be included in current and future portable terminals. Many complex applications, e.g. in the field of video signal processing or human-machine interfaces cause a “power crisis”, which makes the realization difficult. The situation is exacerbated by the limited physical dimensions of a few square centimeters for integrated circuits. Another difficulty is presented by complex system architectures that require circuits in different material systems, like opto-electronics or HF-tranceivers. The solution of embedded technologies cause unacceptable production costs and some even reliability problems. Thus, a new solution for the mentioned problems has to be found.

A possible way out of this dead end is a new kind of 3-D integration of integrated circuits. It offers the possibility of distributing the connections between stacked chips freely, thus gaining in parallelism and consequently in transmission bandwidth. At the same time the length of interconnect lines and therefore power dissipation can be reduced considerably. Different material systems do not propose difficulties any more, because they can be produced and tested separately as a single chip, and then assembled on the 3-D stack. The integration of sensors, memory, processors or analogue circuits benefits from this approach.

Nevertheless this new technique, particularly the processing of vertical contacts, introduces new problems. The single chips are ”known good dies”, tested with standard test algorithms (Abramovici et al., 1990). The task at hand was now to develop a test method specialized in the new 3-D vias. Furthermore a dynamic routing system had to be designed to ensure the overall reliability of the system, even though some of the vertical connections might not be working. The defect model used consists of short to ground, V_{DD} or the next neighbor. In addition to that, a high resistance up to interrupted connection is considered.

The built in self test (BIST) is based on the transmission of simple test-signals and the storage of the test results. On the one hand this information can be analyzed to monitor the development of the new 3-D technology and gather statistical information about the distribution of defects. On the other hand it is used as an input of the routing circuit to avoid defective connections when transmitting data from one chip to another and thus increasing the yield of this novel technology.

Correspondence to: M. Bschorr
(Markus.Bschorr@uni-ulm.de)

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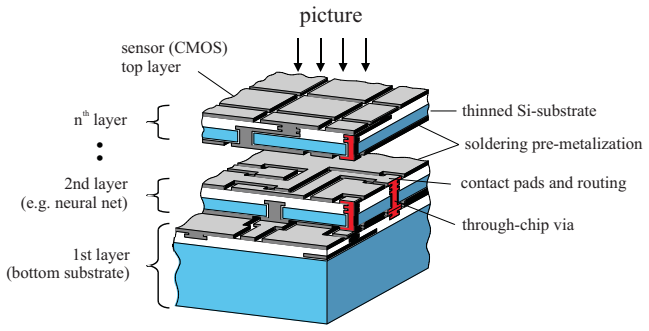

Fig. 1. Schematic description of the 3-D chip stacking

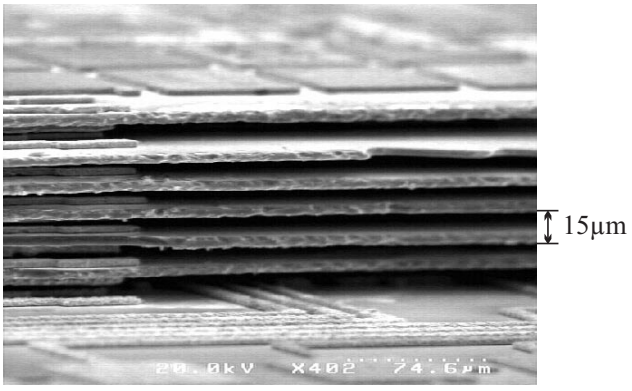

Fig. 2. REM inspection of a seven-chip 3-D stack

2 3-D chip stacking

The goal of the project is to fabricate a stack of chips that introduces a new 3-D connection and packaging technology. The application to be realized is video processing based on pulse-coded neural nets. The 3-D technology will provide the very demanding connection density for the neural net.

The individual parts of the system consist of mixed analogue/digital integrated circuits. Especially the analogue implementation of the integrate-and-fire neurons enable the system to process video signals in a robust manner. The use of moderate operating frequencies leads to the desired low power consumption (Schreiter et al., 2004).

Figure 1 shows a schematic description of 3-D chip stack providing feature detection using pulse-coded neural nets (Heittmann et al., 2002).

3 Technology

A whole new processing scheme was developed that not only provides for the electrical connections between the stacked chips, but also accounts for the mechanical stability of the whole stack (Munding et al., 2004). The starting point are CMOS chips. This standard processing is not altered, 3-D processing starts after their fabricating and testing.

Firstly, the substrate of the silicon CMOS chips has to be thinned to about 10 μm. This step leads to an aspect ratio for the desired vertical connections of 1:2, which is important for the following etching and electroplating. Holes of 5 μm diameter are then etched, isolated in respect to the substrate and filled with copper galvanically. To enable the soldering of different chips on top of each other, the bottom and top of each chip are coated with copper and tin. The soldering step (SOLID Huebner et al., 2002) takes into account, like the other 3-D processing steps, the temperature budget of the CMOS chips. A REM inspection of a fabricated chip stack is shown in Fig. 2. There, an unthinned bottom chip on which six thinned chips are soldered can be seen.

Table 1. Extracted values in the via model

capacitance per unit surface	$C'_{\text{substrate}} \approx [0,2]\frac{fF}{\mu m^2}$
substrate capacitance (Fig. 3)	$C_{\text{substrate}} = [100]fF$
coupling capacitance	$C_{\text{coup}} = [1]fF$
via resistance	$R_{\text{via}} < [5]\Omega$

3.1 Modelling the vias

The materials set by CMOS technology lead to a model for vertical connections dominated by capacitances. Figure 3 shows that caused by the relatively low oxide thickness of less than [1] μm between copper lines and the p^+ layer on the bottom of the substrate, a notable capacitance $C_{\text{substrate}}$ is created. This can be approximated by a parallel plate type capacitor. The influence of the capacitance inside the vias can be neglected, because of the high resistance of the almost undoped substrate R_{Si}. Likewise the capacitive coupling effects have not to be taken into consideration because the distances are magnitudes higher. The results are given ina Table 1. Estimations considering inductances delivered values that do not affect the signals, given the low operation frequency of the system.

3.2 Requirements of the circuits

The via fault possibilities mentioned in Sect. 1 are to be recognized by the BIST. The test result has to be stored and can, if desired, be read serially through a scan-path. In addition to that, requirements imposed by the complete chip stack system have to be considered, most important the area consumption.

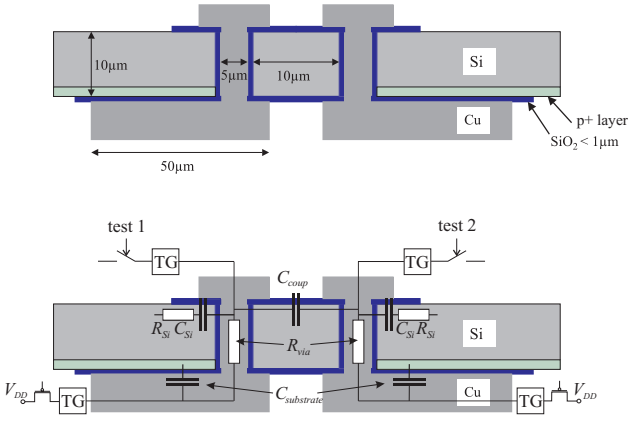

Fig. 3. Schematic description, model und test approach of two adjacent vias

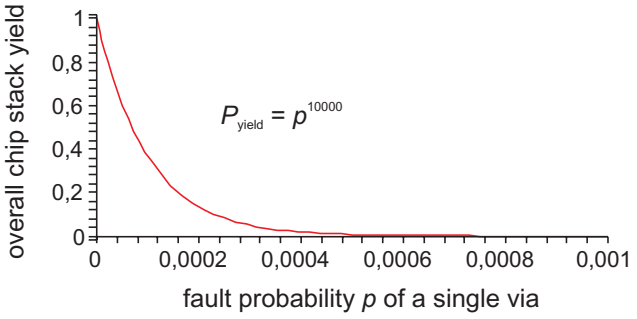

Fig. 4. Overall yield of a chip utilizing 10000 unreliable contacts

4 Unreliable connection and yield

Even if one element of a complex system is slightly unreliable, the overall yield decreases dramatically if this element is used several thousand times in the system. As can be seen in Fig. 4, the yield of a chip stack using 10000 vias rapidly converges towards zero if the fault probability of a single via increases.

Therefore a way of testing the connections has to be found. Only after the test, a dynamic routing circuit can determine a way so that all signals are transmitted through working vias. The proposed system can be seen in Fig. 5.

5 Test approach and circuit

Known and established test algorithms (Abramovici et al., 1990) require too much circuitry, because they do not match the fault model at hand. Their application is the testing of complex integrated circuits. A specialized scheme has been developed. Figure 6 shows that, if the connections between chip A and B have to be tested, circuitry on both chips is needed.

During the testing, the circuits on chip A send a voltage impulse through the vias. If chip B can correctly receive the

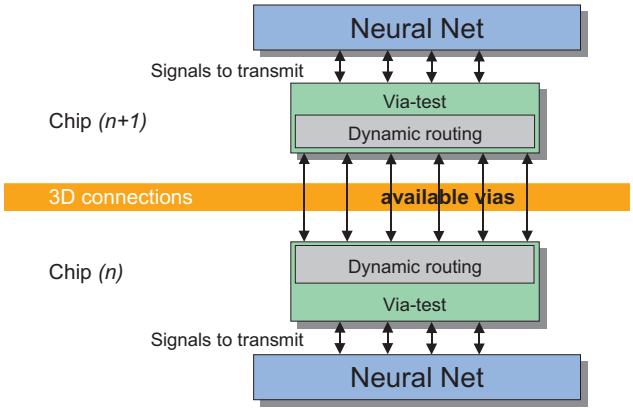

Fig. 5. Test and dynamic routing system overview

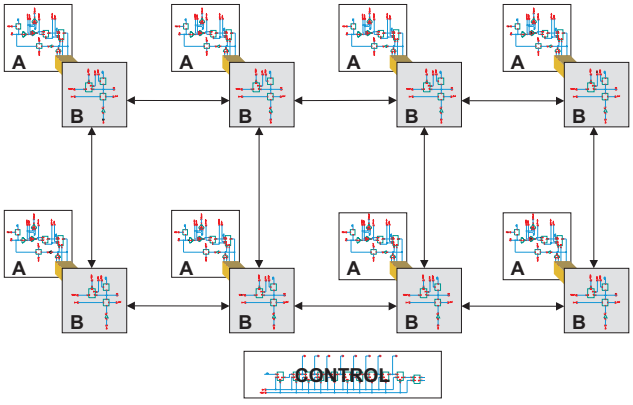

Fig. 6. Example: a 2 by 4 via-field test

test signal, the result is stored: that particular contact works. If not, the default value is kept: the contact is faulty. The impulse is not sent through all vias at the same time. That way shorts to next neighbors can be identified.

As a last step, the gathered information now stored on chip B is sent back to chip A. This is essential, as only when the same information is available on both sides, the routing system described in Sect. 6 is able to avoid faulty connections. In addition to that, the test results can be read out serially for external analysis of the statistics of occurring errors.

The BIST was designed in a [0.13] μm technology. Most of the logic uses transfer transistors and transmission gates to meet the requirements mentioned in Sect. 3.2. As can be seen in Fig. 6, an additional control block is needed on one side of the vias under test. For more information about the test circuit, refer to Bschorr et al. (2005).

6 Routing approaches and circuits

The key to effective routing is redundancy. Depending on the actual application and design of the chip stack, one has to consider two possibilities: are there more vias available

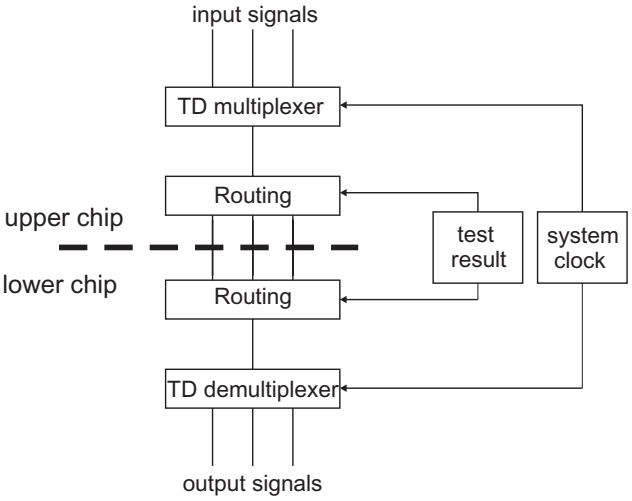

Fig. 7. Block diagram of the routing circuit

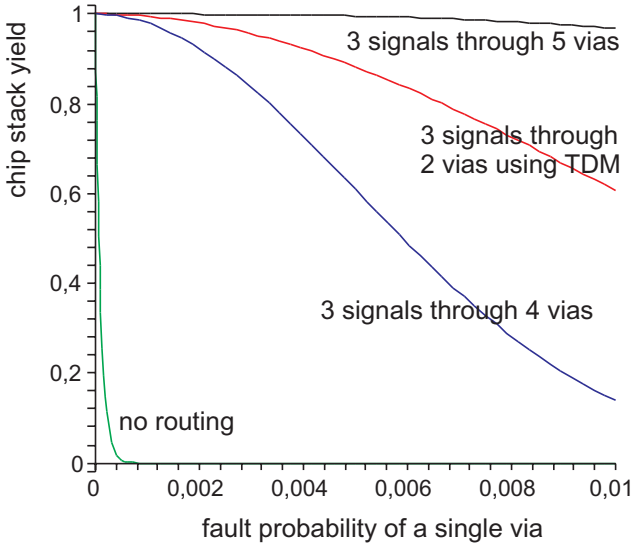

Fig. 8. Dynamic routing: improving the overall yield of a chip stack transmitting 10000 signals vertically

than signals have to be transmitted, or not. In the second case the system does not have built-in redundancy and therefore a time division multiplexing (TDM) scheme has to be introduced to transmit several signals through one connection. Both approaches subdivide the task into groups of vias to limit the use of logic and horizontal interconnect lines to an amount feasible for the application.

If more vias than needed are on-hand, the circuit that identifies possible routes through the unreliable vertical connections is straightforward. Basically the circuit consists of a multiplexer and controlling combinatorial logic that decodes the information found by the test circuit. The same circuitry is needed on the second chip to channel the signals to the appropriate receiver. This whole system works asynchronously.

If TDM has to be introduced, more area consuming circuits are needed. The most severe change is that the system now works synchronously using a global clock signal. To minimize the delay effect caused by TDM, the clock frequency has to be chosen comparatively high. Figure 7 shows an exemplary block diagram of the developed circuits. the routing system was also designed using a [0.13] μm technology.

Under the assumption of evenly distributed defects with the probability p, the yield of the whole system P_{yield} can be calculated. The combinatorial equation used is

$$P_{\text{yield}} = \left(\sum_{n=0}^{N_{\max}} \binom{N_{\text{vias}}}{n} p^n (1-p)^{(N_{\text{vias}}-n)} \right)^{N_{\text{sections}}},$$

where $N_{\max}$ represents the maximum acceptable number of errors per section, N_{vias} the number of vias used per section and N_{sections} the number of sections in the chip stack. The yield improvements achieved by different routing concepts are shown in Fig. 8. As expected one can see that without TDM, the more redundancy is spent, the better the system yield becomes. Applying TDM leads to another trade-off. The higher the amount of signals per connection is chosen, the fewer vias are needed for the transmission, without compromising the reliability. The drawback of this solution is the increasing delay caused by the multiplexing scheme. Here the system designer must decide, what delay is acceptable for the application at hand.

7 Summary and outlook

Vertical inter-chip connections of a technology still under development can be expected to be defect-ridden. To overcome this problem test and dynamic routing circuits were developed that automatically test the unreliable connections and route the signals through working vias. The whole system was designed and simulated using [0.13] μm technology and SPICE-based simulation. A prototype chip containing the test scheme was fabricated and tested, a second is in production. Our future work will consist of combining test and routing circuits to show that the developed system offers a 3-D-communication construction kit which allows designers to use the new technology and improve the overall yield by utilizing a routing scheme fit for the application.

The novel 3-D technology is not only applicable for the proposed neural net example, it is a way out of several problems circuit designers have to face in the near future. One topic is the interconnect problem, another the continuously increasing size of integrated circuits. This stacking technique allows to drastically reduce the length of global interconnects and even enables designers to use different material systems (e.g. silicon CMOS, GaAs optoelectronics, micromechanics) in a compact device.

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