Adv. Radio Sci., 4, 243–246, 2006
www.adv-radio-sci.net/4/243/2006/

Advances in Radio Science

A 10 bit very low-power CMOS SAR-ADC for capacitive micro-mechanical pressure measurement in implants

B. Bechen, D. Weiler, T. v. d. Boom, and B. J. Hosticka

Fraunhofer Institute of Microelectronic Circuits and Systems, Duisburg, Germany

Abstract. This paper presents the development of a 10 bit very low-power CMOS SAR-ADC to be used in medical implants. The first part discusses the principle schematic and the requirements for component matching and the comparator of the ADC. Additionally, the measurement results of a fabricated test chip will be given. The second part of this paper discusses the possibility of direct on-chip implementation of a capacitive pressure sensor in a switched-capacitor SAR-ADC.

1 Introduction

The surge of interest in low-power circuits for implants is driven by the emerging need to extend the battery lifetime. The power supply of a cardiac pacemaker, for example, should last for about 10 years, to avoid a frequent change of the implanted battery by surgery.

Pressure measurement is an interesting application for different types of implants: for example blood, bladder, or ear pressure. Further signal processing is increasingly digital. Therefore, an analog-to-digital converter (ADC) is needed for signal conversion and, due to limited battery capacity, it has to be low-power. A successive approximation architecture ADC (SAR-ADC) seems to be best suited for low-power owing to low hardware complexity.

This paper is organized as follows: the principle of the SAR-ADC and the requirements concerning component matching and the comparator are presented in Sect. 2. The proposed layout and the measured performance of the integrated ADC are given in Sect. 3. Section 4 discusses a system that converts a change in the capacitance of a capacitive pressure sensor to a binary word.

Correspondence to: B. Bechen
(benjamin.bechen@ims.fraunhofer.de)

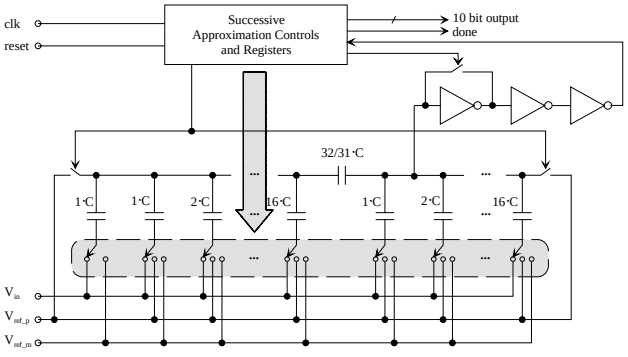

Fig. 1. Principle schematic of a 10 bit very low-power SAR-ADC.

2 The very low-power CMOS SAR-ADC

The principle schematic of the proposed SAR-ADC is shown in Fig. 1. It depends on using the same hardware in N conversion cycles, where N is the resolution of the ADC. The SAR-ADC usually consists of a sample-and-hold stage (S/H), a digital-to-analog converter (DAC), a comparator and a successive approximation register. As can be seen in Fig. 1, the S/H stage and the DAC are realized using a switched-capacitor array, which is divided into two arrays by a transformation capacitor. In the reset phase the MSB node and LSB node are initialized. The comparator, consisting of three inverters, works as an auto-zero comparator using the capacitor array. In the sampling phase the comparator is short-circuited and, therefore, the reference voltage V_m, which is simply the mid voltage between the power supply voltage and ground, rises at the comparator input. Thus, the capacitor array is charged to the difference of the reference voltage V_m and the input voltage V_{in}. During the converting phase, the binary weighted capacitors are either connected to a positive or a negative reference voltage according to the bits of the control register. In the first conversion cycle only the MSB

Published by Copernicus GmbH on behalf of the URSI Landesausschuss in der Bundesrepublik Deutschland e.V.

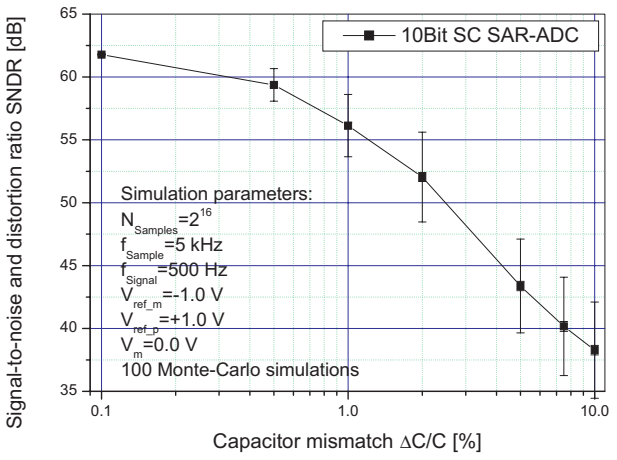

Fig. 2 Monte-Carlo simulations concerning capacitor mismatch.

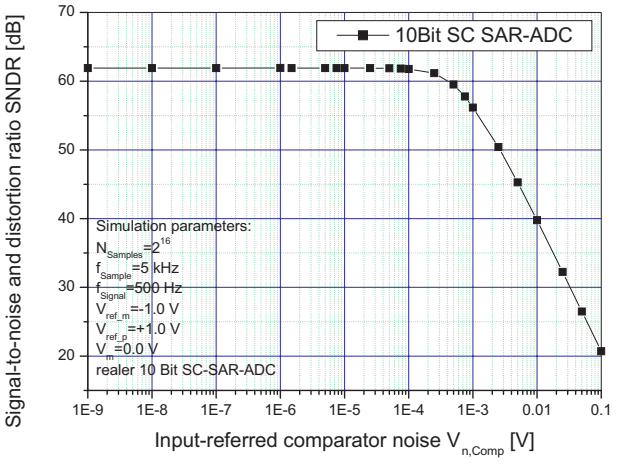

Fig. 3 SNDR over input-referred comparator noise.

in the control register is set. The resulting comparator output determines if the bit remains set or not. Then the next lower bit will be set and the procedure continues until all bits are defined.

In order to save an extra reference network and to verify the current consumption of the pure ADC the analog power supply voltage is used as a reference. In a single-well CMOS process some measures have to be applied to suppress effects of leakage currents caused by conductive pn-junctions, when realizing the SAR-ADC. Due to the fact that the MSB node voltage can become temporarily negative, the n^+ contact of the poly / n^+ transformation capacitor has to be on the LSB side. Additionally, the comparator feedback switch and the MSB node initialization switch have to be realized using only PMOS devices. Accordingly, for the LSB node initialization switch only a NMOS is used, because the LSB node voltage can become higher than the power supply voltage.

The effect of component matching in case of the capacitor array, has been investigated by performing Matlab simulations of a simplified SAR-ADC model. The MSB capacitor has the most deleterious effect on the signal-to-noise and distortion ratio (SNDR). If the mismatch affects only the MSB capacitor, the deviation has to be much lower than 1% to limit the loss in SNDR to 3dB. Due to mismatch in all binary weighted capacitors consisting of unity-size capacitors the Monte Carlo simulation results in Fig. 2 are more meaningful. Each unity- capacitance was randomly "mismatched" and for each of the ΔC's 100 simulations were made. For 3dB loss in SNDR the capacitor mismatch is limited to about 0.5%.

The requirements for the comparator are greatly affected by parasitic capacitances. This can be seen when considering the comparator input voltage:

$$V_{LSB}^{Sample} = V_m \cdot \frac{C_s}{C_s + C_{LSB} + C_{par,LSB}} + V_{in} \cdot \frac{C_{LSB}}{C_s + C_{LSB} + C_{par,LSB}}, \tag{1}$$

$$Q_{LSB}^{Sample} = C_{LSB} \cdot \left(V_{LSB}^{Sample} - V_{in}\right) - C_s \cdot \left(V_m - V_{LSB}^{Sample}\right) + C_{par,LSB} \cdot V_{LSB}^{Sample}, \tag{2}$$

$$Q_{MSB}^{Sample} = C_{MSB} \cdot (V_m - V_{in}) + C_s \cdot \left(V_m - V_{LSB}^{Sample}\right) + C_{par,MSB} \cdot V_m, \tag{3}$$

$$V_{MSB} = \frac{Q_{MSB}^{Sample} + \sum_{Ncycle/2+1}^{Ncycle} C_i \cdot V_i + C_s \cdot \frac{Q_{LSB}^{Sample} + \sum_{0}^{Ncycle/2} C_i \cdot V_i}{C_{LSB}+C_s+C_{par,LSB}}}{C_{MSB} + C_s + C_{par,MSB} - C_s \cdot \frac{C_s}{C_{LSB}+C_s+C_{par,LSB}}}. \tag{4}$$

It can be seen that the comparator input voltage V_{MSB} approaches the mid voltage V_m for large parasitic capacitances $C_{par,MSB}$ from the MSB node to ground and $C_{par,LSB}$ from the LSB node to ground. Since the smallest change in the input voltage, which has to be detected from the comparator, decreases, the accuracy of the comparator has to be increased.

Table 1. Summary of the measured ADC performance.

Resolution	10 Bit	Accuracy	9 Bit
Minimum INL	-1 LSB	Maximum INL	1 LSB
Minimum DNL	- 0.19 LSB	Maximum DNL	0.67 LSB
Offset Error	443 μ V	Gain Error	0.13 %
Sampling Rate	0.8 kSample/s	Supply Voltage	2.5 V
Current Cons. (Analog)	$\sim$ 700 nA	Current Cons. (Digital)	$\sim$ 500 nA

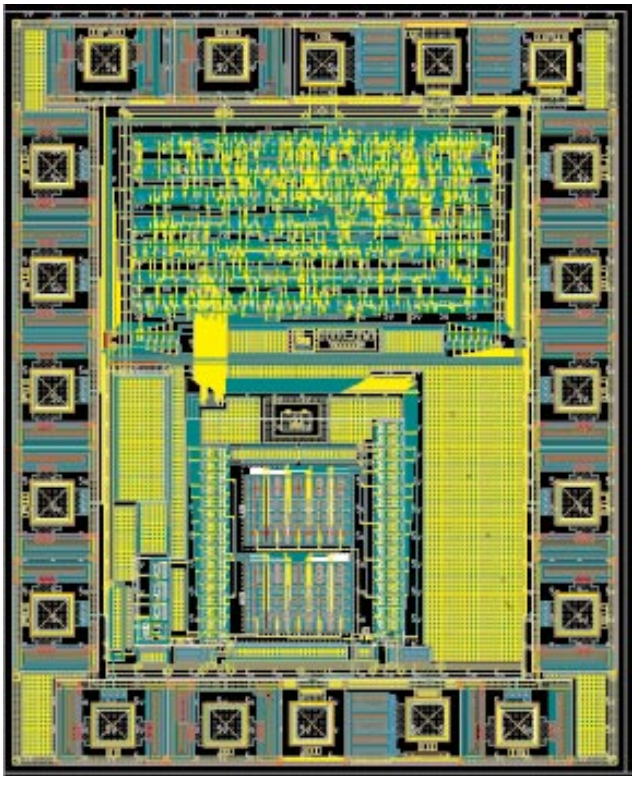

Fig. 4 Layout of the 10 bit SAR-ADC.

The influence of the input-referred comparator noise on the SNDR of a 10 bit SAR-ADC is shown in Fig. 3. For 3dB loss in SNDR the input-referred comparator noise can be about 600μ V. The SNDR of a switched capacitor SAR-ADC is independent of the comparator threshold, because an offset will be stored on the capacitor array and is subsequently cancelled.

3 Layout and measurement results

The layout of the fabricated test chip is shown in Fig. 4. It was designed and fabricated in a standard 0.8μ m single-well CMOS process. Special attention was paid to the capacitive DAC. Unity-size capacitors were used in the arrays and matching was mainly achieved in the MSB and LSB capacitor arrays. Careful arrangement of the wiring makes the parasitic capacitances also binary weighted.

A summary of the measured ADC performance is given in Table I. The measurements correspond to a mean value from a sample collection of 10 chips. Exemplary plots of the differential and integral non-linearity (DNL and INL, respectively) are shown in Figs. 5 and 6. Figure 7 shows the output spectrum of the ADC when a full scale 80Hz sine wave was applied at the input and sampled at 0.8kSample/s. This means it was sampled at fivefold Nyquist rate. The power supply voltage was 2.5 V.

4 An application example

An application example of the presented very low-power SAR-ADC is the pressure measurement in implants based on a direct implementation of a capacitive pressure sensor element in the capacitor array of a SAR-ADC. Weiler et al. (1999) introduced such capacitive pressure sensor element. Advantages are the possibility of full monolithic co-integration with sensor electronics on a single CMOS chip and the saving of a C/V converter. This means a much lower power consumption. Drawbacks are a reduction in the possible resolution of the SAR-ADC, high parasitic capacitances of the pressure sensor, and it is more difficult to achieve good capacitor matching.

The pressure dependent capacitive sensor element is then implemented as MSB capacitor to have the heaviest effect on the resulting output. Simulation results suggest that the best applied input voltage is the mid voltage, and that SNDR increases as the range of the sensor capacitance increases. But the maximum achievable resolution of such system is limited to 2 bits lower than the resolution of the SAR-ADC. Reason for this limitation is that sensor capacitance affects only the MSB and cannot become negative.

In order to get an acceptable value of unity-capacitance multiple pressure sensors have to be switched in parallel. The simulation results with four parallel 1 bar pressure sensors as MSB capacitor are presented in Figs. 8 and 9. The resolution over the whole pressure range of a 1 bar pressure sensor is 7.32 bit, when using a 10 bit SAR-ADC. The pressure-dependent non-linearity has to be compensated.

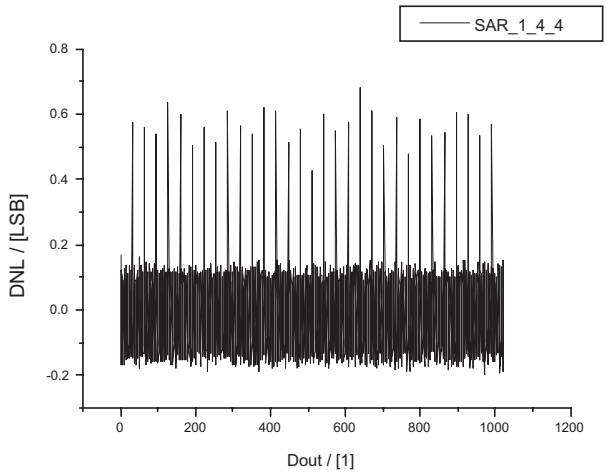

Fig. 5. Exemplary DNL.

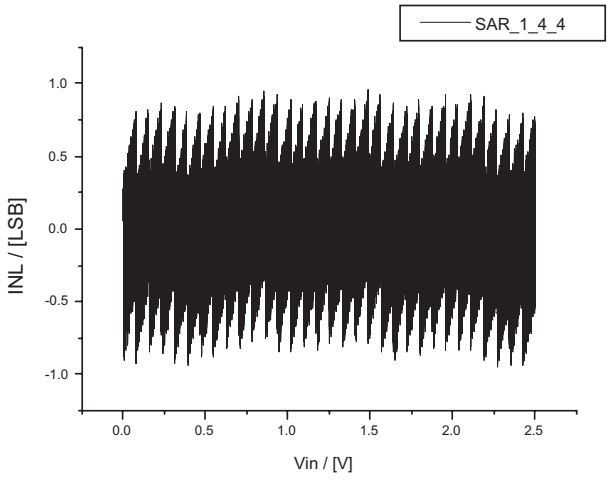

Fig. 6. Exemplary INL.

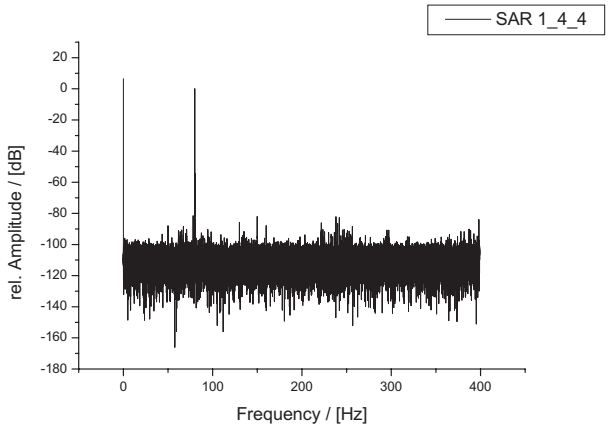

Fig. 7. Measured FFT spectrum at VDD = 2.5 V, 80 Hz input signal frequency, and 0.8 kSample/s sampling rate.

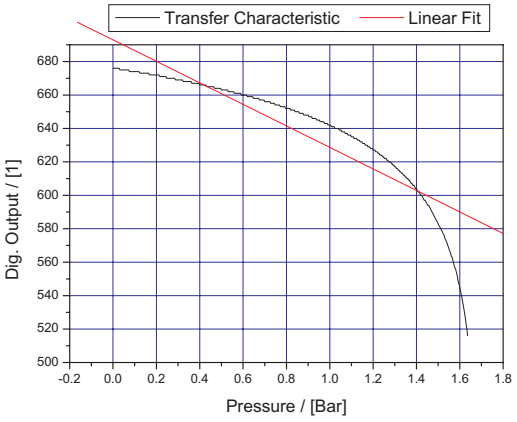

Fig. 8. Transfer characteristic.

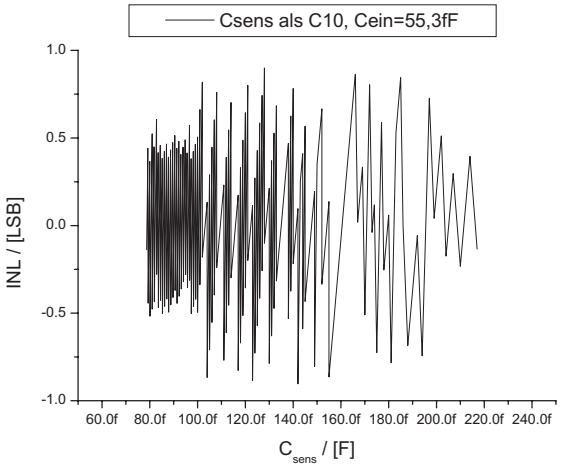

Fig. 9. INL vs. sensor-capacitance.

5 Conclusions

A 10 bit SAR-ADC with 9 bit accuracy and 3μW power consumption has been designed and integrated in standard CMOS technology. The principle and the requirements for matching and the comparator were presented and measures to suppress effects of leakage currents in a single-well process were introduced. The feasibility of direct implementation of an on-chip capacitive pressure sensor using the SAR-ADC was discussed and proven as possible. Hence, a very low-power digital pressure sensor readout for medical implants can be realized.

Acknowledgements. The authors thank R. Thiel, N. Haas, J. Michael, P. Fürst, and M. Jung for their help to obtain a fast realization of the test chip.

References

Weiler, D., Machul, O., Amelung, J., Hammerschmidt, D., and Hosticka, B. J.: An absolute air pressure smart sensor family with 2 dimensional calibration, Proc. 25th European Solid-State Circuits Conf., 21–23 Sept., Duisburg (Germany), 254–257, 1999.