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Towards a generic operational amplifier with dynamic reconfiguration capability

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Abstract. Analog and analog-digital mixed signal electronics needed for sensor systems are indispensable components which tend to drifts from the normal phase of operation due to the impact of manufacturing conditions and environmental influences like etching, aging etc. Precise design methodology, trimming / calibration are essential to restore functionality of the system. Recent block level granular approaches using Field Programmable Analog Array and the more recent approaches from evolutionary electronics providing transistor level granularity using Field Programmable Transistor Arrays offers considerable extensions. In our work, we started on a new medium granular level approach called Field Programmable medium-granular Mixed-signal Array (FPMA) providing basic building blocks of heterogeneous array of active and passive devices to configure established circuit structures which are adaptive, biologically inspired and dynamically re-configurable. Our design objective is to create components of clear compatibility to that of the industrial standards having predictable behavior along with the incorporation of existing design knowledge. The cells can be used in as a single instance or multiple instances. Further, we will focus on a generic dynamic reconfigurable amplifier cell with flexible topology and dimension called Generic Operational Amplifier (GOPA). The incentive of our work comes from recent development in the field of measurement and instrumentation. The digital programming of analog devices is carried out using range of algorithms from simple to evolutionary. Physical realization of the basic cells is carried out in 0.35 μm CMOS technology.

1 Introduction

Primary sensor and mixed signal electronics are indispensable components, which are subjected to strong manufacturing conditions and environmental influences like etching, doping concentration, ageing etc. Subsequently the system tends to drift from its normal functionality. In order to reduce the substantial impact of the undesirable conditions or influences, usual approaches employ trimming / calibration and careful matched layouts during production time (Analog Devices, 2004). The counter measures adapted helps to restore the functionality of the system. The so adapted conservative procedures are slow, static, expensive, and have to be performed repeatedly, if dynamic. More improved approaches adapt these established procedures by compensation techniques during actual working phase in the name of self diagnosis / self-calibration. Block level granular approach entitled Field Programmable Analog Array (FPAA) uses digitally programmable resistors for compensation which are interconnected to the whole amplifier blocks (Fruehauf et al., 2002). The field programmable array structures of the commercially available Anadigm chip best suites the category. The chip allows interconnection of passive elements with the amplifier blocks to application specific in time-discrete domain (Anadigm Inc., 2003). More recent approaches comes from the field of evolutionary electronics (Zebulum et al., 2002), where the circuit synthesis are carried out through learning procedures by a suitable flexible transistor level granular hardware structure called Field Programmable Transistor Arrays (FPTA) (Langeheine et al., 2003). Substantial drawbacks here are the fact that optimisation algorithm should invent the knowledge of an experienced designer, e.g, designing a sensor signal amplifier, uses excessive switching resources resulting in large internal memory configuration. These structures also exhibit characteristics of a black box, where the underlying behaviour remains unforeseeable. Here the point of preservation is that the quality parameters essential for automatic control comes from a special flexible structure of hardware, especially dynamic reconfiguration. Our research work, focuses on developing a suitable, flexible and dynamically re-configurable hardware structure called Field Programmable medium-granular Mixed-signal

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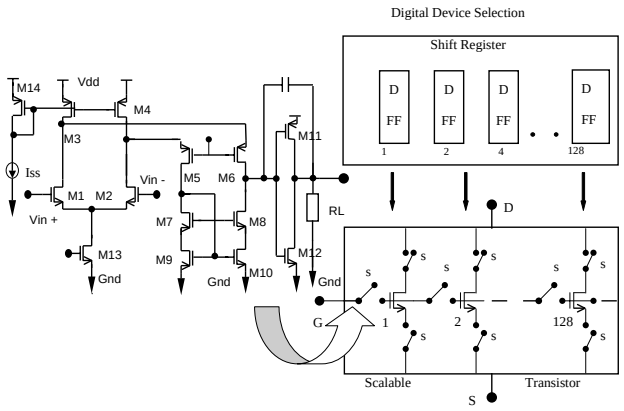

Fig. 1. Folded Cascode amplifier and the replacement scheme of ordinary by the heterogeneous array / scalable transistors (Lakshmanan and Koenig, 2004).

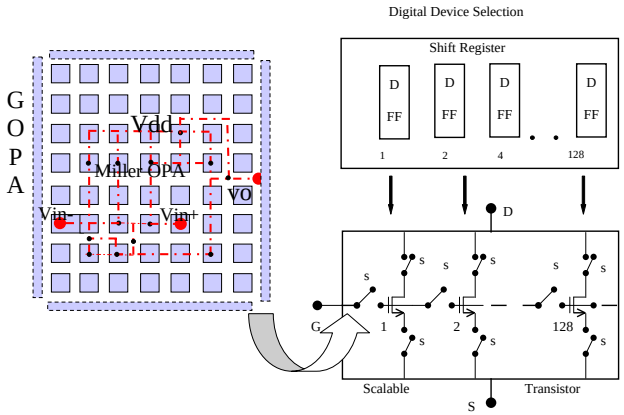

Fig. 2. Schematic representation of GOPA realizing miller operational amplifier.

Array (FPMA) providing a platform for the implementation of algorithms ranging from a simple to the more recent organic computing, paving the way in realising the favourable behaviour or characteristics of living organisms. The favourable characteristics for our interest include self-monitoring, self-testing, self-healing, self-repair, which are generally referred to as Self x characteristics. The implementation of the work is carried out in 0.35μm CMOS technology of Austriamicrosystems provided by EUROPRACTICE.

2 Re-configurable operational amplifier

The approach pursued by our work combines the concepts presented in the previous section with the objective of building flexible hardware structure suitable for sensor electronics. In our work, we focused on the design and implementation of sensor signal amplifier reducing the fine grained homogenous FPTA structure to a suitable medium grained heterogeneous structure thereby reducing the switching resources and consequently the parasitic effects of the switches. The approach also reduces the on chip storage requirement and decreases the reconfiguration time compared to that of its counterpart namely FPTA. The choice of the dimensions of the basic active and passive elements of the heterogeneous array are determined by simulations for the chosen technology (Lakshmanan and Koenig, 2004) and from the inspiration taken from A/D – D/A converters.

The dimensions of the transistors vary in the powers of two that are interconnected through switches. The selection of the appropriate dimension for the switches plays a vital role as it has subsequent impact on the overall system performance. The selection of active or passive device from the array are carried out by turning on the switches connected to their corresponding terminals. The switching patterns are fed sequentially through shift registers. Figure 1 shows the schematic of the time-continuous sensor signal amplifier with folded cascode topology using ordinary transistors and their corresponding replacement scheme by the scalable transistors / heterogeneous array.

3 Generic operational amplifier - GOPA

In the previous section, realisation of a time continuous sensor signal amplifier was carried out. In this section we focus on building a generic amplifier block which is flexible to both dimensions and topology. GOPA consists of array of scalable active and passive devices.

The next level hierarchical switches called Topology Switches (TS) interconnect the heterogeneous arrays. By switching ON and OFF these topology switches interconnecting the scalable array, various established amplifier topologies are realized ranging from a simple Miller to Telescopic operational amplifier. The flexibility is not only restricted to two stages but are also extended to three stage amplifier structures with programmable compensation capacitors and nullifying resistors. Some possible building structures of any operational amplifier topology that are realized by GOPA are simple and cascoded current mirrors, Wilson current mirror in the tail current region. Diode or current mirror loaded differential pairs and cascoded output stages. Realization of single ended and differentially ended output is also realized. The GOPA structure is capable of realizing more than 15 established simulation verified amplifier structures providing complete flexibility both in the choice of the structure and in dimensioning the devices constituting the structures. Figure 2 represents GOPA structure realizing Miller operational amplifier.

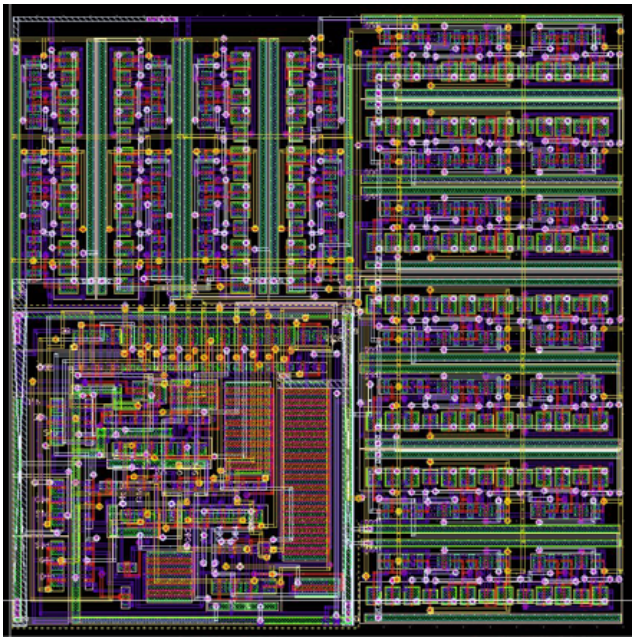

Fig. 3. Layout of NMOS scalable transistors.

4 Implementation

After promising results from the schematic level simulations of the pursued concepts in the previous sections, are thereafter implemented for a sensor signal amplifier. Fig.3 shows the layout of the NMOS scalable transistor array along with the digital interface surrounding the. heterogeneous array. The layout area of the NMOS scalable transistor is $60\,\mu\text{m} \cdot 64\,\mu\text{m}$. The flexibility does not come for free. A compromising additional layout area is consumed. The scalable transistors form the basic building blocks of FPMA. The array consists of 11 transistors interconnected by transmission switches. The minimum sized transistors are replicated 4 times in order to avoid the effects of mismatching. The remaining 7 transistors vary in the powers of two. Therefore, a total of 11 switch signal are needed for each scalable transistor array. The selection of the appropriate transistors from the array is performed by feeding in the bit patterns to the shift registers, which is a sequential process. The concept of dimensioning or programming is not refrained to active devices but also extended to passive devices like resistors and capacitors.

The passive element array plays a vital role in compensation and in feedback circuitry. Unlike the active devices, the passive array consists of 8 re-configurable bits ranging from 125 fF to 16 pF for the compensation capacitance and from 125 Ω to 16 KΩ for the scalable resistors. The heterogeneous array of passive elements, both resistors and capacitors are built in similar fashion like the transistor array through interconnection of the switches. The selection process of the devices remains identical. Combination of all scalable active and passive devices constitutes GOPA. Figure 4 shows the physical implementation of the sensor signal amplifier realized from GOPA constructed with the scalable devices.

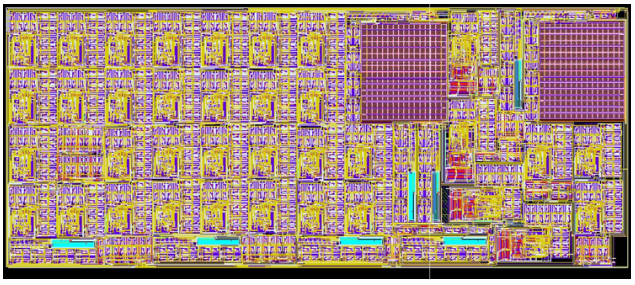

Fig. 4. Layout of complete GOPA realizing one possible OpAmp topology namely folded cascode.

The layout consists a total of 45 scalable devices and 59 topological switches. The performance curve of the folded cascode operational amplifier is shown in Figs. 5 and 6 for its gain and phase margin respectively. Different curves in the graph shown in Figs. 5 and 6 refers to simulation results obtained initially with ordinary transistors and later by replacing with the scalable version. In this work, simulations were carried out in the so called extrinsic fashion. A considerable degree of behavior comparability is to be expected with the manufactured chip of the dynamic re-configurable folded cascode operational amplifier performed later with intrinsic simulations. With regard to practical applications, in addition to normal pins of the OpAmp, data (D) pin, enable (EN) pin, clock (clk) pin are essential. The enable signal ensures that the digital section does not interact with operation phase of the amplifier after suitable device selections are performed. This ensures additional separation between the different domains of analog and digital is not necessary. The objective of this chip comes after studying the need and advancement in the field of measurement and instrumentation. Our design objective is to create cells of clear compatibility to that of the industrial standards with expectable behavior along with incorporation of existing design knowledge. The chip can be used in as a single or multiple instances. The prototype of the chip is under preparation.

5 Conclusion

In this paper, we have realized the implementation of the time continuous dynamically re-configurable sensor signal amplifier that is flexible in both topology and in sizing of the active and passive devices with drift compensation capabilities, compatible to that of the industrial standards. The flexibility does not come for free. A compromising additional layout area is consumed. The chip under preparation will allow implementation of algorithms ranging from a simple to Organic / Evolutionary, exhibiting the desirable self-x char-

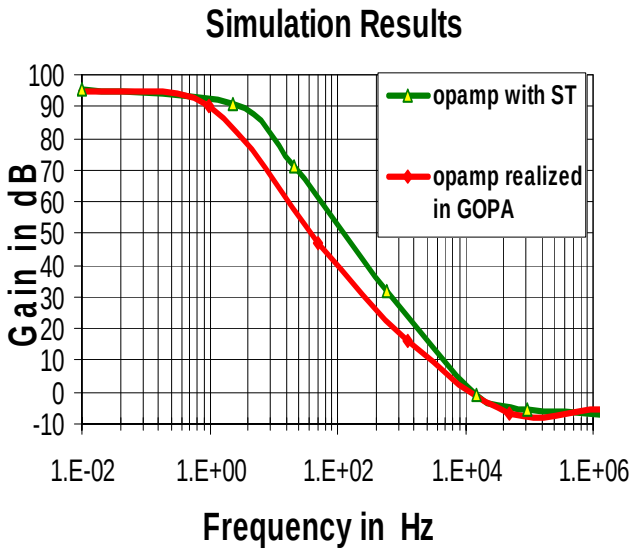

Fig. 5. Folded-cascode OPA-gain.

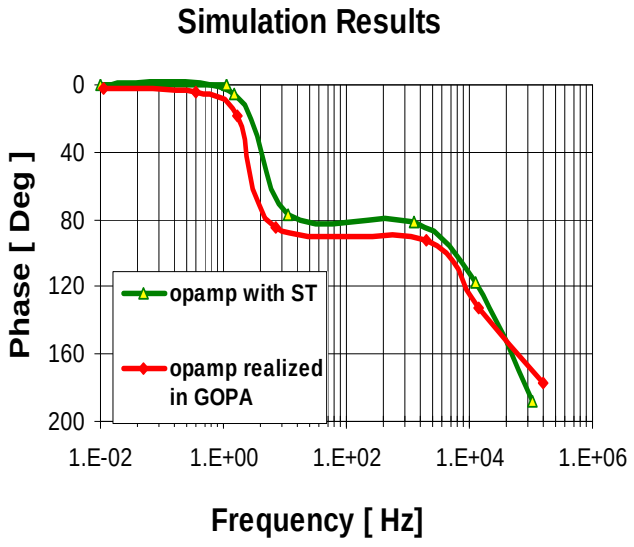

Fig. 6. Folded-cascode OPA-phase.

acteristics of biological organisms. In future works, the developed chip will be subjected to reconfigure in a mixtrinsic fashion. Result confirmation through measurements. Optimization of the area through much compact layouts. As a long-term research, adaptation could be extended to the sensor in the optimization loop.

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