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On the synthesis and optimization of cascaded continuous-time Sigma-Delta modulators

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Abstract. Up to now, there exist two completely different approaches for the synthesis of cascaded CT Sigma-Delta modulators. While the first method is based on a DT prototype and thus on the application of a DT-to-CT transformation, the second one is entirely performed in the CT domain. In this contribution, the method of lifting will be applied to overcome the disadvantages afflicted with the first method (e.g. less ideal anti-aliasing filter performance, increased circuit complexity) and to establish a time efficient DT simulation model for the second method. Thereby, optimal modulator coefficients as well as optimal digital cancellation filters for an arbitrary cascaded CT modulator can be simulated in an efficient and rapid manner. For illustrative purposes, the complete synthesis procedure is demonstrated by the example of a 2-1-1 cascaded CT modulator.

1 Introduction

Owning to their inherent robustness to most circuit non-idealities afflicted with deep-submicron CMOS technologies, the concept of Sigma-Delta A/D conversion has proven itself as a very efficient technique for the implementation of A/D converters in such technologies over the last decades. While their classical field of application is found in low to medium bandwidth with medium to high resolutions such as telephone or audio, nowadays, they have to deal with ever-growing bandwidth standards altogether with the demand for higher or even adjustable resolution as it may be imposed by video or broadband data communication applications.

For several reasons, especially the principle of cascaded continuous-time (CT) Sigma-Delta modulators seems to be a most promising concept for such applications. Compared to a single stage realization of the same overall modulator order N ($N \geq 3$), they achieve a higher resolution (Marques et al., 1998). This benefit stems from the a priori stability of such modulators when only first and second order modulators are used in the cascade, which enables a noise-shaping filter behavior more closely to the one of an ideal high-pass filter of the same order. Moreover, the resolution of cascaded architectures can simply be adjusted by switching on or off several stages in the cascade which makes them very attractive for multi-standard adaptive circuits (Rodríguez-Vázquez, 2005). Compared to DT realizations, CT modulators show the advantage of a lower power consumption due to their lower bandwidth requirements for their operational amplifiers. Finally, any CT modulator offers an intrinsic anti-aliasing filter, thus giving it the additional advantages of reduced die area and further power savings compared to DT realizations.

After a short introduction to the state-of-the-art techniques for the synthesis of cascaded CT modulators and their afflicted drawbacks in the next Section, the method of lifting will be introduced using the example of a CT 2-1-1 modulator to overcome these drawbacks.

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2 State-of-the-art techniques

2.1 DT-to-CT transformation

The first method (Ortmanns et al., 2001) benefits from the extensive work and its ongoing results performed on cascaded DT modulators for which a broad spectrum of literature is available, among others (Marques et al., 1998; Medeiro et al., 1999). By means of the DT-to-CT transformation, which was already well known from single stage modulators (Cherry et al., 2000), it was not only possible to translate any DT coefficients into CT ones, but also to re-use the very simple digital cancellation filters developed for cascaded DT modulators in CT architectures. Unfortunately, the resulting cascaded CT architecture as shown for the example of the 2-1-1 modulator in Fig. 1 differs from its DT equivalent in that addi-

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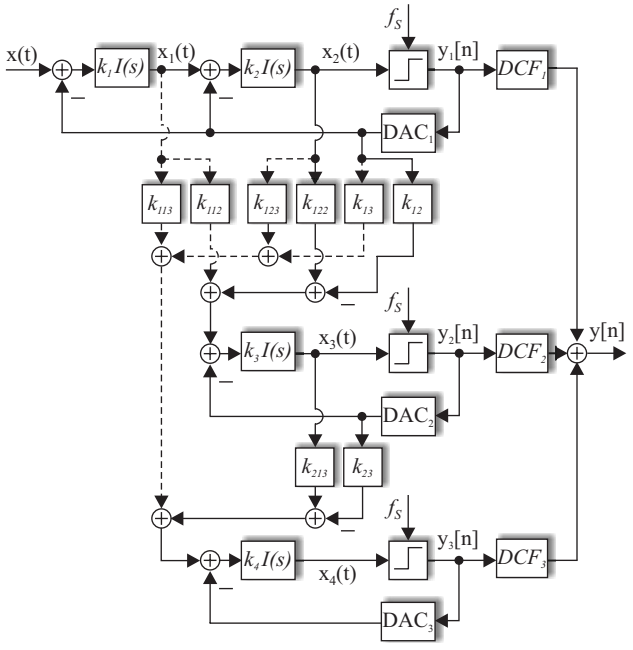

Fig. 1. Continuous-time 2-1-1 modulator based on the classical DT architecture (solid) and as obtained from a DT-to-CT transformation (including dashed signal paths).

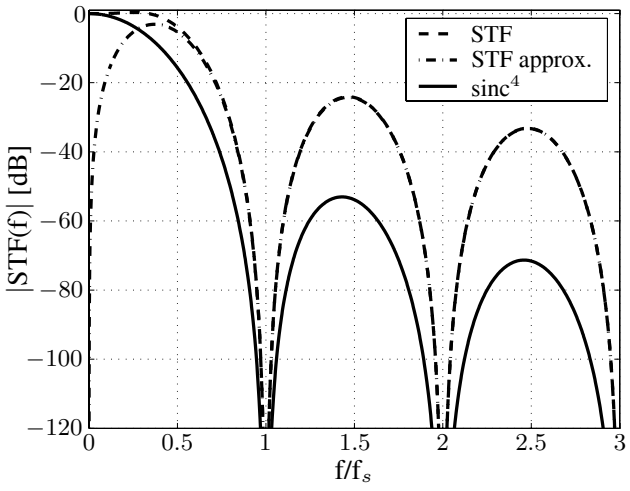

Fig. 2. Signal transfer function of the CT 2-1-1 modulator shown in Fig.1 with and without additional signal paths (dashed line vs. solid line) and approximation of the former by Eq. (1) (dashdot line).

tional signal paths (Fig. 1, dashed lines) are needed in order to enable the DT-to-CT transformation. Other than the mentioned drawback of increased circuit complexity (Tortosa et al., 2005), it has been shown that due to the direct connection from the first stage to the third stage via k_{113}, the high frequency behavior of the signal transfer function $STF(s)$ and therewith the anti-aliasing feature is given by Keller et al. (to be published):

$$STF(s) \approx k_1 k_{113} k_4 \left(\frac{f_s}{s}\right)^2 \frac{DCF_3[z]}{LF_3[z]}\bigg|_{z=e^{s/fs}} \qquad (1)$$

where f_s/s represents the integrator transfer function $I(s)$, $DCF_3[z]$ the digital cancellation filter and $LF_3[z]$ the loop filter of the last stage, respectively. The magnitude of the STF together with its approximation for high frequency input signals according to Eq. (1) is shown in Fig. 2 (dashed line vs. dashdot line). All CT coefficients have been derived via a DT-to-CT transformation of the DT coefficients given in Marques et al. (1998).

2.2 Direct synthesis

To overcome the drawback of increased circuit complexity afflicted with the DT-to-CT transformation, it has been proposed to skip the additional signal paths, which are solely needed to make the DT-to-CT transformation possible, and rather to re-adjust the digital cancellation filters (Tortosa et al., 2005). The first step toward that end is to transform the given modulator into its mathematical representation as shown in Fig. 3. A detailed description to this approach is given in Keller et al. (to be published). Replacing the strongly nonlinear quantizers by their linear white noise models and transforming every conglomerate of DAC, CT loop-filter LF or CT connecting loop-filter CLF and sampler to its DT equivalent allows for each noise transfer function, i.e. the transfer function from one quantization error to the output $y[n]$, to be entirely calculated in the z-domain. Therewith, the digital cancellation filter can be adjusted in the traditional manner, namely to cancel the quantization errors of all stages but the last. Furthermore, the overall noise transfer function related to the quantization error of the last stage should result in an ideal high-pass filter whose order is equal to the overall modulator order, i.e. the sum of the orders of all single stage modulators in the cascade, while maintaining a DC gain of one for the signal transfer function.

The application of this method overcomes the drawback of increased circuit complexity. Moreover, the resulting signal transfer function is equal to an ideal fourth order sinc-filter and therewith offers a superior anti-aliasing feature compared to the approach of the DT-to-CT transformation (Fig. 2, solid line vs. dashed line). However, it is detrimental in that one still has to resort to time consuming CT simulations. This becomes even more apparent whenever optimal coefficients as well as optimal digital cancellation filters for any cascaded CT architecture have to be found or to be verified by simulation.

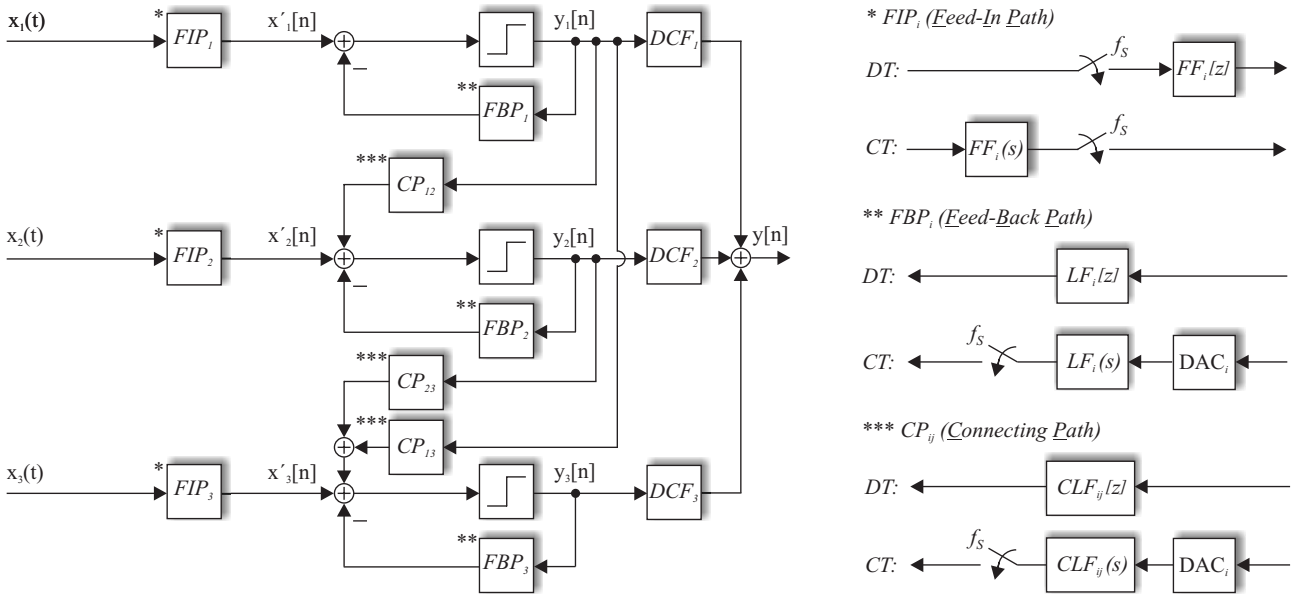

Fig. 3. System theoretical approach for a DT or CT modulator realized as a cascade of three single stage modulators possessing arbitrary orders. All $x_i(t)$ are equal to the input signal $x(t)$ - generally applied to the first stage of the cascade only - and may therefore be shorted.

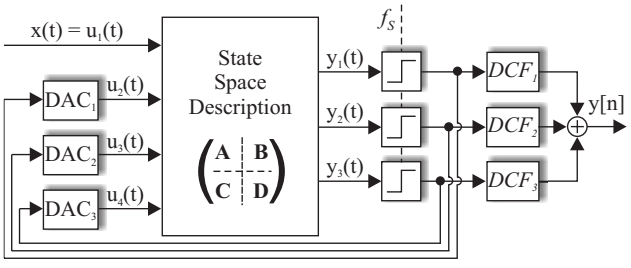

Fig. 4. State space representation of a cascaded CT modulator composed of three single stage modulators possessing arbitrary orders.

3 Lifting

To obtain a fast but yet precise DT simulation model for any CT cascaded modulator, the method of lifting is introduced using the example of the CT 2-1-1 modulator without additional signal paths in Fig. 1. Toward that end, the state space description of this modulator has to be found. Assuming a sample frequency equal to one and following the notations in Figs. 1 and 4, the state space description of this multiple input and multiple output system results in:

$$\begin{aligned} \dot{\boldsymbol{X}}(\boldsymbol{t}) &= \boldsymbol{A}\ \boldsymbol{X}(\boldsymbol{t}) + \boldsymbol{B}\ \boldsymbol{U}(\boldsymbol{t}) \\ \boldsymbol{Y}(\boldsymbol{t}) &= \boldsymbol{C}\ \boldsymbol{X}(\boldsymbol{t}) + \boldsymbol{D}\ \boldsymbol{U}(\boldsymbol{t}) \end{aligned} \tag{2}$$

with

$$\boldsymbol{A} = \begin{pmatrix} 0 & 0 & 0 & 0 \\ k_2 & 0 & 0 & 0 \\ 0 & k_{122}k_3 & 0 & 0 \\ 0 & 0 & k_{213}k_4 & 0 \end{pmatrix} \quad \boldsymbol{C} = \begin{pmatrix} 0\,1\,0\,0 \\ 0\,0\,1\,0 \\ 0\,0\,0\,1 \end{pmatrix}$$

$$\boldsymbol{B} = \begin{pmatrix} k_1 & -k_1 & 0 & 0 \\ 0 & -k_2 & 0 & 0 \\ 0 & -k_{12}k_3 & -k_3 & 0 \\ 0 & 0 & -k_{23}k_4 & -k_4 \end{pmatrix} \quad \boldsymbol{D} = \boldsymbol{0} \tag{3}$$

The DT state space description is then easily obtained as (Yamamoto, 1999):

$$\begin{aligned} \boldsymbol{X}[\boldsymbol{n}+\boldsymbol{1}] &= e^{\boldsymbol{A}}\boldsymbol{X}[\boldsymbol{n}] + \int_0^1 e^{\boldsymbol{A}(\boldsymbol{1}-\boldsymbol{\tau})}\boldsymbol{B}\boldsymbol{U}[\boldsymbol{n}](\boldsymbol{\tau})d\tau \\ \boldsymbol{Y}[\boldsymbol{n}] &= \boldsymbol{C}\boldsymbol{X}[\boldsymbol{n}] \end{aligned} \tag{4}$$

$\boldsymbol{U}[\boldsymbol{n}](\boldsymbol{\tau})$ is a vector containing the lifted input signals to the state space system block, each defined as a sequence of functions:

$$\begin{aligned} &\mathcal{L} : u \mapsto \{u[n](\tau)\}_{n=0}^{\infty}, \\ &u[n](\tau) = u(n+\tau), \\ &0 \le \tau \le 1 \end{aligned} \tag{5}$$

$$DCF_1[z] = \frac{(k_1 + 12b_1k_1 + 4)z^3 + (11k_1 + 12 - 12b_1k_1)z^2 + (11k_1 - 12 - 12b_1k_1)z + k_1 + 12b_1k_1 - 4}{24k_1z^4}$$
$$DCF_2[z] = \frac{(2b_2 + 1)z^3 - (6b_2 + 1)z^2 + (6b_2 - 1)z + 1 - 2b_2}{2c_1z^4}$$
$$DCF_3[z] = \frac{(1 - z^{-1})^3}{c_1c_2} \quad (6)$$

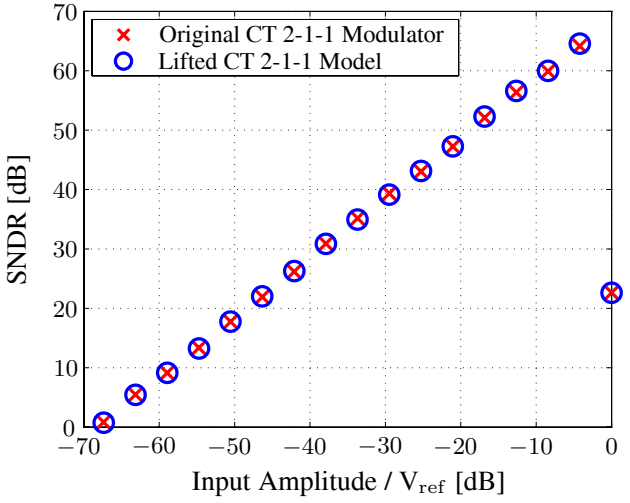

Fig. 5. SNDR of the CT 2-1-1 modulator, simulated on the original modulator (x-mark) and its lifted model (o-mark).

Unlike the classical DT state space transformation, which assumes the input signals $u_i(t)$ to be constant over one sampling interval, this approach allows for arbitrary waveforms of both the input signal as well as the feedback signals. With regard to the mathematical modelling of cascaded CT Sigma-Delta modulators, the former has its justification only in case of a DC input signal in combination with non-return-to-zero (NRZ) DAC output signals while it is erroneous for every other type of input or DAC output signal.

The only condition to be fulfilled for an efficient implementation of this model in a simulator like MATLAB is imposed by the integral in Eq. (4) to be solvable in closed form. Since usually criteria like stability, dynamic range or achievable signal-to-noise-ratio are determined by applying a sine wave input signal to the modulator (Schreier et al., 2005), troubles in solving the integrals may only be encountered depending on the choice of the DAC signal waveforms.

The application of lifting to the CT modulator thus results in an exact DT state space representation of the CT modulator. This in turn allows for fast and yet precise DT simulations to be performed without paying the penalty of loosing the inter-sampling behavior of the CT system and therewith loosing the information of the exact states of the state space variables. In this way optimal coefficients for a cascaded CT modulator based on the traditional DT architecture, i.e. feeding the quantization error of one stage to the next stage only, may be found by resorting to fast simulations. Moreover, scaling of the state space variables can easily be performed.

In order to validate the correctness of the application of lifting, exemplary simulations have been performed on the lifted model of the 2-1-1 modulator in Fig. 1 to find optimal values for the connecting coefficients k_{112}, k_{12}, k_{213} and k_{23}. More precisely, these connecting coefficients have been substituted by $c_1/(k_1k_2)$, c_1b_1, c_2/k_3 and c_2b_2 and the new coefficients b_i and c_i have been optimized. Although beyond the scope of this paper, this allows for a direct comparison with the optimal DT connecting coefficients as presented in Marques et al. (1998). Note that already a parametric sweep over these four coefficients between 0.1 and 2 with a step width of 0.1 results in 160000 simulations. In this context, a set of coefficients is defined as optimal in case that the highest signal-to-noise-and-distortion ratio (SNDR) within a signal bandwidth f_b of 1/32 (OSR 16, f_s 1) is achieved using a sine wave input signal with an amplitude of 0.7 times the reference voltage of the DAC and a frequency of $f_b/4$. The remaining coefficients k_1 to k_4 (2/3, 3/8, 1/2, 1/2) have been chosen according to a DT-to-CT transformation of the DT coefficients given in Marques et al. (1998). For the reason of simplicity, only NRZ digital-to-analog converters have been used. The digital cancellation filters given in Eq. (6) are obtained by calculations using effective quantizer gains of $1/(k_1k_2)$ in the first stage, $1/k_3$ in the second stage and $1/k_4$ in the third stage, respectively. With the obtained coefficients b_1, b_2, c_1 and c_2 (9/10, 1/5, 1/5, 11/10), simulations concerning the dynamic range of the modulator have been performed on both the original modulator and its lifted model. Obviously, the results shown in Fig. 5 are almost identical and therewith do confirm the correctness of the lifting approach.

4 Conclusions

In this contribution, it has been shown that cascaded CT modulators based on the classical DT architecture, i.e. feeding the quantization error to the next stage only, have two important advantages over those derived by DT prototypes: reduced circuit complexity and superior anti-aliasing filter behavior. The drawback of long simulation runtime afflicted with behavioral models of cascaded CT modulators was overcome by the application of lifting to the CT modulator. Time effi-

cient simulations can then be performed on the equivalent DT model with almost identical results. However, lifting is thus far only applied to the simulation of ideal modulators. The embedding of non-idealities such as finite opamp gain or even jitter in these simulations will further improve both the quality and the profitableness of this method.

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