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A Verilog-A model of an undoped symmetric dual-gate MOSFET

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Abstract. We describe a new procedure of solving the electrostatic potentials in the silicon film of an undoped DG SOI MOSFET structure. Starting from a model previously described in the literature by Malobabic et al. (2004), we propose the bisection method for the solution of transcendental equation giving the surface electrostatic potential of the silicon channel, as a function of the gate to source voltage and the voltage along the channel. The above calculated results are used for obtaining the charges and corresponding drain current in the DG MOSFET transistor. The entire model is implemented in Verilog A and can be used inside Cadence for the determination of the static regime of electrical circuits based on undoped symmetric DG SOI MOSFET. As a case study, a simple common-source amplifier built with such a novel device is analyzed, showing the currents and voltages present in the circuit.

1 Introduction

Scaling CMOS devices and associated technologies down to nanometer sizes is limited by short channel effects in terms of: band to band tunneling current, drain induced barrier lowering (DIBL) leakage, gate induced drain leakage, direct tunneling through gate oxide leakage current. The double-gate SOI MOSFET appeared as a promising technological alternative with the following advantages: 1) light doping of the channel reducing the mobility degradation due to elimination of impurity scattering; 2) good control of short channel effects because of reduced influence of the drain voltage on the channel charge; 3) ideal subthreshold slope due to elimination of substrate doping; 4) increased electrostatic control due to gate voltage applied on both sides; 5) increased current drive capability due to volume inversion Balestra et al. (1987) of the entire silicon film. However, some disadvantages exist in terms of 3D technological complexity and ultra thin silicon film needed for these SOI MOSFET devices.

In parallel with technological efforts for the realization of these nanostructures, much work has been devoted to the understanding and modeling of the behavior of DG MOSFET devices (Balestra et al., 1987; Taur, 2000; Malobabic et al., 2004; Kilchytska et al., 2004). The absence of doping in the silicon substrate and channel has created increased possibilities for analytical calculation of Poisson's equation in the silicon film (Taur, 2000), where only one type of mobile mobile charge has been used. An important step in the analytical modeling of DG SOI MOSFET has been done by Malobabic et al. (2004) where the influence of the applied voltage along the channel on the mobile charge in the silicon film is introduced. In their paper Malobabic et al. (2004), the Lambert function has been used for the calculation of the surface electrostatic potential in the silicon.

The purpose of our paper is to show a simple method for the calculation of that surface electrostatic potential in silicon film and, thus, making unnecessary the application of Lambert function. Actually, our approach consists of the usage of bisection method for finding the surface potential as a function of gate to source voltage and the applied voltage on drain terminal. For the DC characterization of DG MOSFET transistor, in the next step,the charge and current are calculated based on the model given in literature by Ortiz-Conde et al. (2005). The entire procedure is implemented in Verilog A and can be used as a library for the DC modeling of an electric circuit built with undoped symmetric DG SOI MOSFET. At the end of the paper, we shall show an example of DG MOSFET based common source amplifier circuit solved in the static regime by means of Cadence.

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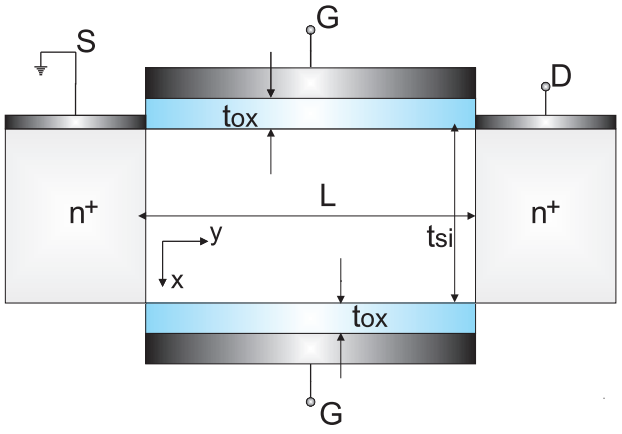

Fig. 1. Double Gate SOI MOSFET structure.

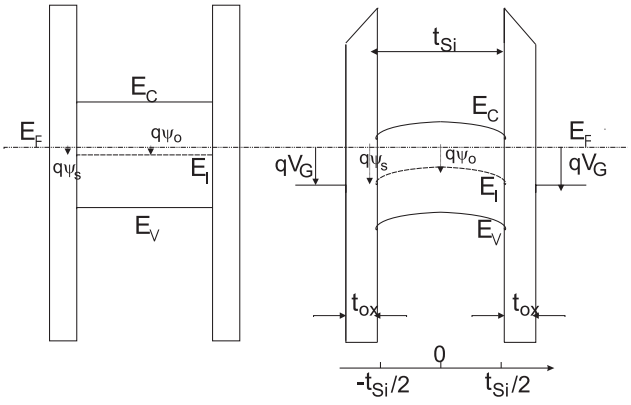

Fig. 2. Energy bands diagram for a DG SOI MOSFET.

2 Background

Figure 1 depicts an undoped symmetric Double Gate SOI MOSFET structure which is one-dimension (1-D) analytically analyzed. Here, the current flows only on the y direction. Due to its symmetry property, both gates have the same work function, oxide thickness and the same applied voltage on their terminals.

The corresponding energy bands diagram of DG SOI MOSFET is represented in Fig. 2. Because of the lack of contact in the silicon body, the Quasi-Fermi level is constant along the vertical direction ($x-$axis) and the energy levels are referred to the electron quasi-Fermi level of the n^+ source/drain (Taur, 2000). On the left side, the energy bands diagram at thermodynamic equilibrium in the structure is shown, while on the right side the band bendings in the presence of an applied voltage on the gates is presented. In addition, this figure proves intuitively also the volume inversion specific to this DG SOI MOSFET.

In agreement with Fig. 2, within this approach, it is assumed that the silicon film of undoped symmetric DG SOI MOSFET is in the volume inversion state (Balestra et al., 1987). In addition, quantum confinement effects are not taken into account, even if they can play a role for very thin silicon thickness. Another assumption of the model is the application of Maxwell-Boltzmann statistics for the charge carriers in silicon which can be well-supported by the very low doping of the substrate. Based on this supposition, the starting point of the analytical model consists of calculation of Poisson's equation as in Taur (2000), Malobabic et al. (2004) and Ortiz-Conde et al. (2005):

$$\frac{d^2\psi}{dx^2} = \frac{qn_i}{\varepsilon_{si}} \cdot e^{\frac{q(\psi - V)}{kT}} \tag{1}$$

with the following boundary conditions, compatible with a DG SOI MOSFET:

$$\frac{d\psi}{dx}|_{x=0} = 0 \tag{2}$$

$$V_{GS} - V_{FB} = \psi|_{x=\frac{t_{si}}{2}} + \frac{\varepsilon_{si} t_{ox}}{\varepsilon_{ox}} \cdot \frac{d\psi}{dx}|_{x=\frac{t_{si}}{2}} \tag{3}$$

where: Ψ is the electrostatic potential in the silicon body, V_{FB} represents the flatband voltage, V_{GS} is the gate to source voltage, V refers to applied channel potential and takes values from 0 at the source to V_{DS} at the drain end, n_i is the intrinsic carrier concentration in silicon, t_{ox} and t_{si} are the oxide, respectively silicon, thickness, ε_{ox} and ε_{si} are the oxide and silicon dielectrical permittivity, respectively. Boundary condition expressed by Eq. (2) is modeling the maximum electrostatic potential present in the central part of silicon film. The condition given by Relation (3) is the normal electrical displacement at the interface between silicon and $Si\,O_2$.

Due to volume inversion assumption, contribution of minority holes in neglected is the above Poisson's equation.

From the first integration of Poisson's Eq. (1), the electric field in silicon is obtained:

$$\frac{d\psi}{dx} = \sqrt{\frac{2kTn_i}{\varepsilon_{si}} \cdot e^{-\frac{qV}{kT}} \left[e^{\frac{q\psi}{kT}} - e^{\frac{q\psi_0}{kT}} \right]} \tag{4}$$

and the electrostatic potential is derived from the second integration of it:

$$\psi(x) = \psi_0 - \frac{2kT}{q} \cdot ln \left[\cos\left(b \cdot e^{\frac{q(\psi_0 - V)}{2kT}} \cdot x \right) \right] \tag{5}$$

When x equals to $t_{si}/2$, one can calculate the electrostatic potential at the surface of silicon film from Eq. (5) as follows:

$$\Psi_S = \Psi_0 - \frac{2kT}{q} \cdot \ln \left[\cos\left(b \cdot \mathrm{e}^{\frac{q(\Psi_0 - V)}{2kT}} \cdot \frac{t_{si}}{2} \right) \right] \tag{6}$$

where $b = \sqrt{\frac{q^2 n_i}{2\varepsilon_{si} kT}}$.

By taking into account the definition domain of natural logarithm function from Eq. (6), one can obtain the maximum electrostatic potential in the central point of silicon film as follows:

$$\psi_{0max} = V + \frac{kT}{q} \cdot \ln\left(\frac{2\pi^2 \varepsilon_{si} kT}{q^2 n_i t_{si}^2}\right) \tag{7}$$

Introducing Relation (4) in the Eq. (3), a transcendental equation dependent on both electrostatic potentials in silicon film is obtained:

$$\Psi_S = V_{GS} - V_{FB} - a \cdot \sqrt{e^{-\frac{qV}{kT}}\left(e^{\frac{q\Psi_S}{kT}} - e^{\frac{q\psi_0}{kT}}\right)} \tag{8}$$

where

$$a = \frac{t_{ox} \cdot \sqrt{2\varepsilon_{si} kT n_i}}{\varepsilon_{ox}}$$

and Ψ_S and Ψ_0 are the electrostatic potentials at the surface and the center of the silicon body, respectively.

For the calculation of ψ_0, Malobabic et al. (2004) have used smoothing functions, previously applied for the description of the drain voltage at transistor saturation. These equations are presented below:

$$\psi_0 = U - \sqrt{U^2 - (V_{GS} - V_{FB}) \cdot V_{FB}} \tag{9}$$

$$U = \frac{1}{2} \cdot [(V_{GS} - V_{FB}) + (1 + r) \cdot \psi_{0max}] \tag{10}$$

$$r = (At_{ox} + B)\left(\frac{C}{t_{si}} + D\right) e^{-EV} \tag{11}$$

where the following parameters were found in order to model ψ_0 from the above authors: $A = 0.0267\,\mathrm{nm}^{-1}$, $B = 0.0270$, $C = 0.4526\,\mathrm{nm}$, $D = 0.0650$, $E = 3.2823\,\mathrm{V}^{-1}$, $V_{FB} = 0\,\mathrm{V}$ for simplicity, r is the shoulder smoothing parameter and Eq. (11) is empirical.

Based on Eq. (9), one can calculate ψ_0 for each applied gate voltage. For the calculation of ψ_S, the above authors have used the Lambert function, which in our opinion is a complex approach.

3 Description of bisection method

Our method is considering the above set of equation characterizing the DG SOI MOSFET behavior, but we are proposing a new procedure of solving the transcendental equation described in the Relation (8), based on the bisection method. For this purpose, we rearrange the equation this equation as shown below:

$$\psi_S - V_{GS} + a \cdot \sqrt{e^{-\frac{qV}{kT}}\left(e^{\frac{q\Psi_S}{kT}} - e^{\frac{q\psi_0}{kT}}\right)} = 0 \tag{12}$$

The next step is to define a function with the left hand side of the equation as follows:

$$f(\psi_S) = \psi_S - V_{GS} + a \cdot \sqrt{e^{-\frac{qV}{kT}}\left(e^{\frac{q\Psi_S}{kT}} - e^{\frac{q\psi_0}{kT}}\right)} \tag{13}$$

Now, one can easily observe that the solution of Eq. (12) is the intersection of the function f with horizontal axis represented by the variation of ψ_S amount. If the function keeps the same monotony in a given interval $[c, d]$ and goes to a zero value inside that interval, then the following condition $f(c) * f(d) < 0$ is fulfilled.

In our case, the searched value of ψ_S must be in the range $[0, V_{GS}]$ because the electrostatic potential in the n-channel DG SOI MOSFET is positive and cannot exceed the applied V_{GS} voltage.

For the application of bisection method to determine the solution ψ_S, we have to consider an interval $[c, d]$ and the median point $m = (c + d)/2$. Then we have to calculate the values of the f, in the following points: $f(c)$, $f(m)$ and $f(d)$. If the product $f(c) * f(m) < 0$, then the desired value of ψ_S is in the interval $[c, m]$. If the product $f(m) * f(d) < 0$, then the searched solution of transcendental Eq. (8) is in interval $[m, d]$. After the identification of the reduced interval where the solution is located ($[c, m]$, $[m, d]$) we shall continue the procedure in the same way until the moment we find the solution ψ_S with the desired accuracy. This algorithm has been implemented in the Verilog A program and has provided very good solutions for each V_{GS} applied on both gates of DG MOSFET and ψ_0 calculated by the above method.

By taking into consideration the above electrostatic potentials in silicon and the applied voltages of DG SOI MOSFET, one can calculate the drain current in the device. Different analytical models are used for description drain current in the literature and we are presenting here the following expression given in Ortiz-Conde et al. (2005).

$$\begin{aligned} I_D = \mu \frac{W}{L} \cdot \Bigg\{ & 2\frac{\varepsilon_{ox}}{t_{ox}} \cdot \Big[V_{GF} \cdot (\psi_{SL} - \psi_{s0}) \\ & - \frac{1}{2}\left(\psi_{SL}^2 - \psi_{S0}^2\right) \Big] + 4\frac{kT\varepsilon_{ox}}{qt_{ox}} \cdot (\psi_{sL} - \psi_{S0}) \\ & + t_{si} kT n_i \cdot \left(e^{\frac{q(\psi_{0L} - V_{DS})}{kT}} - e^{\frac{q\psi_{00}}{kT}}\right) \Bigg\} \end{aligned} \tag{14}$$

For our I_D calculations the following technological and material parameters have been used: $\psi_S 0$, ψ_{sL} are the surface silicon potentials at the ends of the channel, source respectively drain and $\psi_0 0$, ψ_{0L} represent the central silicon potential at the source end and drain end, $\mu = 300\,\mathrm{cm}^2/\mathrm{Vs}$, $W/L = 1$, $t_{ox} = 2\,\mathrm{nm}$, $t_{si} = 20\,\mathrm{nm}$.

In the above electrostatic potentials equations, the drain current and bisection algorithm has been implemented in Verilog A and, further, integrated in Cadence Design Framework II for the simulation of undoped symmetric DG SOI MOSFET. Figure 3 shows such a simulation schematic realized in Cadence for supplied voltage of 2 V and V_{GS} equal to 0.5 V. In that figure, only three terminals are depicted because of dual-gate's symmetry.

In Fig. 4, we show the DC output characteristics of an undoped symmetric SDG SOI MOSFET, for given gate to

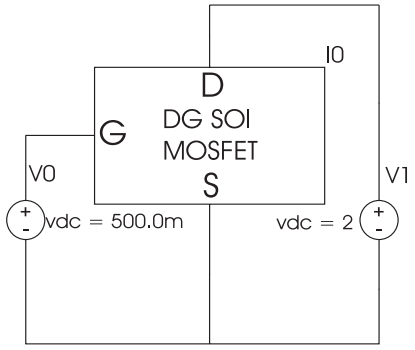

Fig. 3. DG SOI MOSFET realised in CADENCE.

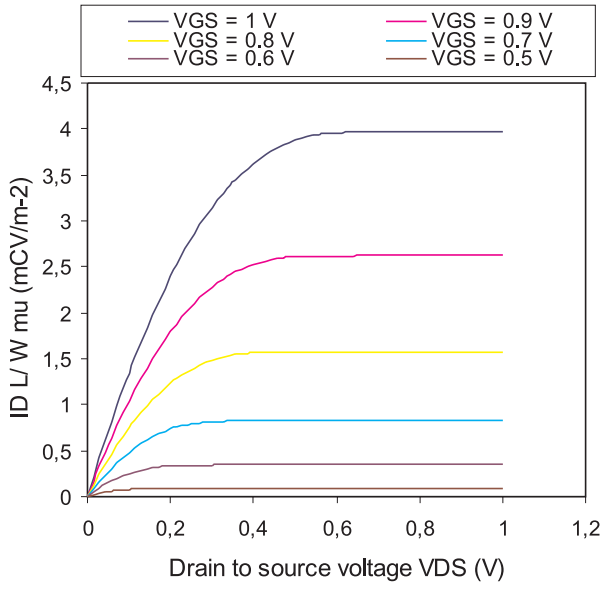

Fig. 4. DC output characteristics of the undoped symmetric DG MOSFET obtained with bisection method.

source voltages, for the surface electrostatic potential calculated with our bisection method.

As a confirmation of the quality of our bisection method used for the ψ_S calculation, we have compared the results obtained by us with the similar results got in reference by Ortiz-Conde et al. (2005) and have found very good fit.

The above results can be important for the DC characterization of electronic circuits based on DG SOI MOSFET devices. As a case study, in Fig. 5, we present common source amplifier circuit built in Cadence with the MOSFET behavior imported from Verilog A.

As an example, we have solved this circuit for a supplied voltage of 2 V. The solution obtained by Cadence for the above circuit and DG SOI MOSFET model described above is the following: $V_{DS} = 1.767$ V, $I_D = 93.37\,\mu$A, $V_{GS} = 0.5$ V. More complex electrical circuits can be solved

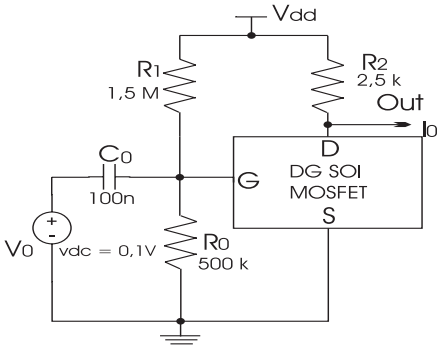

Fig. 5. Common-Source Amplifier having the DG MOSFET.

in the same way, having the DG SOI MOSFET model implemented as above.

4 Conclusions

A simple numerical method based on bisection procedure has been proposed for the calculation of the surface electrostatic potential in an undoped symmetric DG SOI MOSFET device, starting from the analytical approach of Poisson's equation. Our method could replace other complex approaches based on Lambert function and smoothing factor without physical meaning which were previously used for the same electrostatic potential calculation. Our method has given the same results when it is compared with similar approaches in the literature. The entire electrostatic potential and current model of DG MOSFET has been implemented in Verilog A and further integrated in Cadence. The usefulness of our method has been proved by the simulation of the static regime of a simple common source amplifier where the current and the voltages have been very easily obtained.

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