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Analog circuits using FinFETs: benefits in speed-accuracy-power trade-off and simulation of parasitic effects

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Abstract. Multi-gate FET, e.g. FinFET devices are the most promising contenders to replace bulk FETs in sub-45 nm CMOS technologies due to their improved sub threshold and short channel behavior, associated with low leakage currents. The introduction of novel gate stack materials (e.g. metal gate, high-k dielectric) and modified device architectures (e.g. fully depleted, undoped fins) affect the analog device properties significantly. First measurements indicate enhanced intrinsic gain (g_m/g_{DS}) and promising matching behavior of FinFETs. The resulting benefits regarding the speed-accuracy-power trade-off in analog circuit design will be shown in this work. Additionally novel device specific effects will be discussed. The hysteresis effect caused by charge trapping in high-k dielectrics or self-heating due to the high thermal resistor of the BOX isolation are possible challenges for analog design in these emerging technologies. To gain an early assessment of the impact of such parasitic effects SPICE based models are derived and applied in analog building blocks.

1 Introduction

Scaling limitations of standard planar bulk CMOS technologies such as short channel effects or leakage currents enforce the introduction of new device concepts like silicon-on-insulator (SOI) and/or multi-gate transistors.

Especially 3-dimensional FinFET devices as shown in Fig. 1 offer a large variety of interesting features. Here the transistor consists of vertical (fully-depleted) Si fins on a buried oxide (BOX), surrounded by the gate stack. The channel width per fin of this tri-gate device results in $W{=}2H_{\text{fin}}{+}W_{\text{fin}}$. FinFET devices combine the advantages of fully depleted (FD) SOI devices with the features of a multi-gate device. So they show low short channel effects (SCE), however the requirements on the Si layer thickness (i.e. the fin height) on top of the BOX are relaxed compared to planar (single-gate) FD devices. On the other hand the fin width has to be chosen as small as possible ($W_{\text{fin}}{\leq}2/3L_{\text{min}}$) to keep the short channel effects under control, (Colinge, 2004). Using small fin pitches (i.e. $\leq 2H_{\text{fin}}{+}W_{\text{fin}}$) enables comparable or even higher area efficiency in terms of the current per device width ratio. Table 2 shows an example for a prototype FinFET technology, targeting a 45 nm LP process, (Schulz et al., 2005).

Of course also novel process features can be implemented in a FinFET technology. Metal gates eliminate poly depletion effects and enable undoped Si fins. HALO implants are no longer necessary due to the low SCE. High-k dielectrics can be used to reduce gate tunneling currents while bringing up other new issues such as increased flicker noise or reduced mobility. The introduction of these new materials and device concepts implicates changes in analog transistor characteristics as output resistance or matching behavior. Sect. 2 covers the basic analog transistor properties of FinFETs compared to standard bulk devices. Also their specific impact on circuit design is discussed. New materials and device architectures cause also new effects, such as transient variations in transistor current due to self heating or charge trapping. In Sect. 3 these effects are shown, concerning their impact on transistor behavior, modeling aspects and their influence on analog circuits.

2 Analog device properties and impact on circuit design

The feasibility of digital and analog multi-gate circuits has already been proven, (Knoblinger et al., 2005; Pacha et al., 2006). But these circuits do not take advantage of special multi-gate device features, as discussed in this section. The FinFET devices presented here are based on the technology

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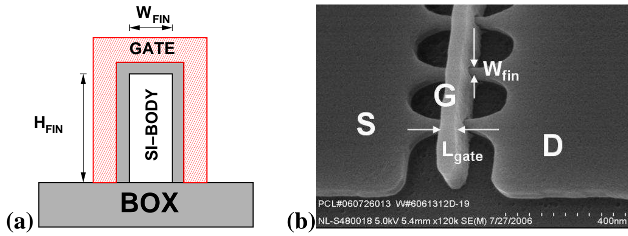

Fig. 1. Schematic X-section **(a)** and TEM image **(b)** of FinFET.

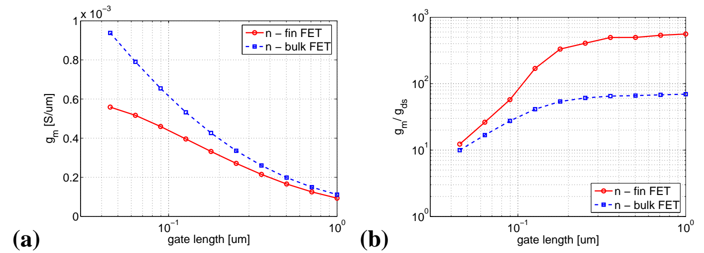

Fig. 2. g_m and g_m/g_{ds} of bulk- and FinFET.

Table 1. Example for FinFET technology.

Technology features		
W_{fin} [nm]	30	
H_{fin} [nm]	60	
L_{min} [nm]	45	
Gate electrode	TiSiN	
Dielectric	HfSiON	
Fin doping [cm^{-3}]	10^{15}	
Electrical features	**NMOS**	**PMOS**
L_{gate} [nm]	60	60
V_{DD} [V]	1.0	1.0
I_{ON} [μA/μm]	560	330
I_{OFF} [nA/μm]	1.4	0.027
S [mV/dec]	69	72
DIBL [mV]	46	44

shown in Table 2, the bulk devices are based on a comparable 45 nm process.

2.1 Small signal parameters

The transconductance g_m and the output conductance g_{DS} are the basic DC transistor properties that determine the performance of analog circuits. Figure 2.1 compares g_m of FinFET and bulk nFET at $V_{GS}=V_T+200$ mV and $V_{DS}=V_{DD}$. The g_m of the FinFET is reduced for short channel lengths up to 30%. This is attributed to the lowered mobility on the rough fin sidewall and the high resistance of the connection from the source-drain landing pads to the active channel region under the gate. Lowered g_m values implicate lowered transit frequency values and decreased RF performance. A possible solution for this issue is a selective epitaxial growth (SEG) process to fill the gaps between gate and source-drain pads and to reduce the high source-drain resistance.

The output conductance of FinFETs is expected to be very low due to the missing HALO implants. HALO implants introduce an additional barrier at the drain side of the channel region that can be modulated by the drain-source voltage. This effect degrades significantly the output resistance of bulk devices in modern CMOS technologies. For a fair comparison we use the intrinsic transistor gain defined as g_m/g_{DS} here. Figure 2.1 shows that the gain of the FinFET is improved, despite the lower g_m. For typical analog device dimensions the gain is about 2–10 times higher. Taking g_m and g_{DS} into account we conclude that FinFETs are best suited for low power analog circuits with frequencies below 10 GHz.

2.2 Benefits in speed-power trade-off

To investigate the benefits of the improved intrinsic gain on circuit level a standard two stage Miller compensated OTA is simulated. The following specifications are used: DC voltage gain $A_{V0}\geq 50$ dB, gain bandwidth product $GBW\geq 10$ MHz for a 5pF capacitive load and a phase margin of 60°. To compare FinFET and bulk implementation a figure-of-merit is defined as gain bandwidth to power ratio: FOM=GBW/P. The starting point of the comparison is a bulk design using only $3L_{\text{min}}$ devices that fulfills the given specifications. This design is compared to a FinFET implementation using devices with the same channel length of $3L_{\text{min}}$. Due to the high intrinsic transistor gain, the FinFET version shows an improved voltage gain (about 30 dB higher) and reaches the same gain bandwidth product, see the Bode diagram in Fig. 3.

As the specifications do not require such a high gain, the FinFET implementation can use shorter channel lengths to reach higher g_m values. The improved g_m can then be used to enhance the gain bandwidth product or to decrease the power consumption. Figure 3 shows two FinFET implementations using devices with $1.4L_{\text{min}}$ channel length. Both OTAs have a voltage gain of around 50dB, while one is optimized for high gain bandwidth and the other for low power. Table 2 shows the quantitative results of the comparison. Using the improved output conductance the FOM of the FinFET implementation can be improved by about 30%, although the g_m is reduced.

2.3 Matching behavior

Random variations such as fluctuations of channel/gate dopants, oxide charge or surface roughness lead to current mismatch of nominal identical devices. In today's CMOS technologies the mismatch of the threshold voltage V_T is the dominant effect. The variation of V_T can be approximated

Table 2. Characteristic values of different implementations.

Version	$3\,L_{\text{min}}$ bulk	$3\,L_{\text{min}}$ FinFET	$1.4\,L_{\text{min}}$ FinFET	$1.4\,L_{\text{min}}$ FinFET
GBW [MHz]	10.8	10.6	14.7	10.4
A_{V0} [dB]	48.4	81.3	47.1	47.6
P [W]	53.2	55.6	56.8	41.9
FOM	0.203	0.191	0.259	0.248
Improvement	–	–6%	+28%	+22%

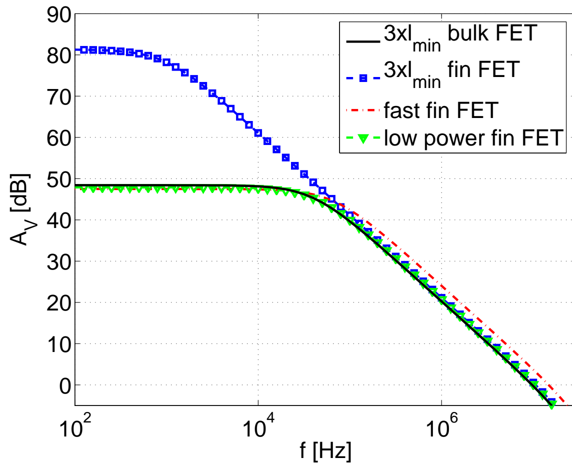

Fig. 3. Bode diagram of different implementations.

as $\sigma_{V_T}=\frac{A_{V_T}}{\sqrt{WL}}$, (Pelgrom et al., 1989). A_{V_T} is a technology constant proportional to the oxide thickness and the channel doping: $A_{V_T} \propto t_{ox}\sqrt[4]{N_D}$. Thus metal gate FinFETs with undoped body are expected to show good matching behavior. This assumption can be proven by measurements as shown in Fig. 4. Compared to bulk devices with poly gate, the matching constant of FinFETs with metal gate amounts roughly to the half. It is important to note that the matching behavior degrades for very narrow fins in the current state of technology. Here other effects are dominant, e.g. the variations of the source-drain resistance, gate misalignment or line edge and sidewall roughness. Technology optimization is still necessary. E.g. SEG could improve the matching behavior by decreasing the source-drain resistance.

2.4 Benefits in speed-accuracy-power trade-off

Of course matching is one of the most important device properties for analog circuit design. It can be shown that in many cases the speed-accuracy-power trade-off is limited in general by the matching behavior (Kinget and Steyaert, 1996):

$$\frac{\text{Speed} \cdot \text{Accuracy}}{\text{Power}} \propto \frac{1}{C_{ox}A_{V_T}^2} \tag{1}$$

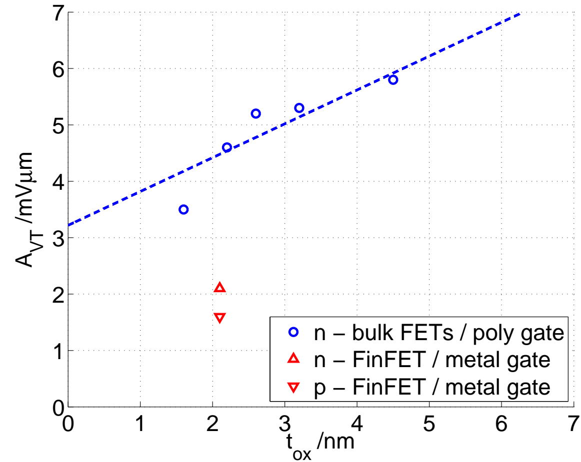

Fig. 4. Matching constant in different technology nodes (Gustin et al., 2006; Parvais et al., 2006; Decoutere, 2006).

Obviously an improved matching constant A_{V_T} can be used to reduce the area consumption or enhance the resolution without the drawback of increased power consumption. As concrete example for this relationship we use a current source in a current steering DA converter. The DAC specifications for resolution and yield determine the tolerable current variation $\frac{\sigma(I)}{I}$ of the current sources (van den Bosch et al., 2001). These matching requirements can be converted into area requirements:

$$WL_{\text{current source}} = \frac{1}{2\left(\frac{\sigma(I)}{I}\right)^2}\left(A_\beta^2 + \frac{4A_{V_T}^2}{(V_{GS}-V_T)^2}\right) \tag{2}$$

Assuming that the mobility mismatch given by A_β^2 is negligible compared to the V_T mismatch, a reduction of A_{V_T} by a factor of two enables a reduction of the current source area by a factor of four.

3 Simulation of parasitic effects

Besides the beneficial analog properties presented above, FinFETs show some new effects that have to be considered in the design of analog circuits. As example we discuss self heating and charge trapping. Both effects lead to transient variations of the transistor current and influence the behavior of analog circuits.

3.1 Self heating – modeling and scaling behavior

The local temperature increase of active devices due to their dissipated power is called self heating (SH). Important transistor parameters, e.g. V_T or the mobility μ depend on the temperature and thus on the dissipated power. For high values of V_{DS} and V_{GS} the reduction of the mobility is the dominant effect, so the transistor current is decreased by SH. Self

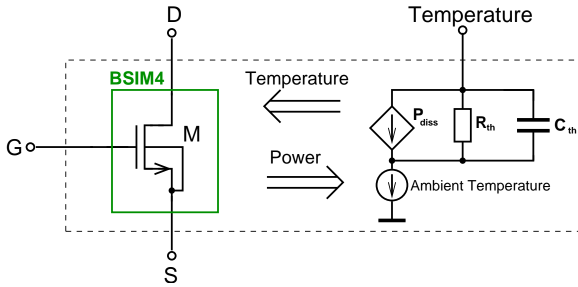

Fig. 5. Self heating equivalent circuit.

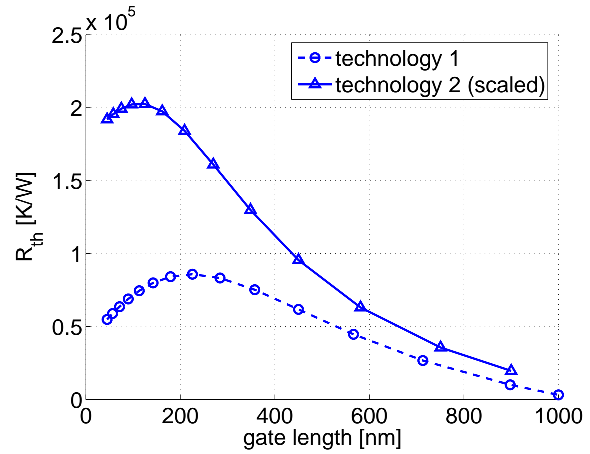

Fig. 6. Impact of technology scaling on R_{th}.

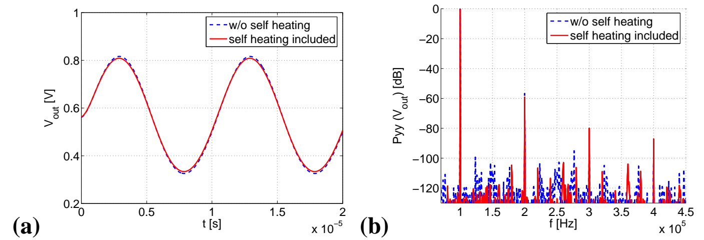

Fig. 7. OTA output voltage with and without SH in time **(a)** and spectral domain **(b)**.

heating is more severe in SOI technologies due to the low thermal conductivity of the surrounding oxide that acts as thermal insulator. To quantify SH usually the thermal resistance R_{th} is used. The time dependence of SH can be described with the thermal capacitance C_{th} as shown in the equivalent circuit model for a transistor with self heating in Fig. 5. The equivalent circuit is based on electro-thermal coupling: the dissipated power is sensed and applied to the thermal RC network which determines the actual device temperature which then again influences the transistor parameters. To avoid complex measurements or device simulations for the extraction of the thermal resistance, in (Bertolissi, 2004) an alternative approach is shown. Here a thermal network of complex 3d FinFET structures is constructed based on small building blocks where a analytic calculation of R_{th} is possible. This model is used here to investigate the impact of technology scaling on the thermal resistance. A scenario with relaxed design rules is compared to a scaled technology as shown in Fig. 6. Fin dimensions and pitch, metal/contact dimensions and pitch as well as the BOX thickness are reduced. The thermal resistance of a test device with 2 fins is increased up to a factor of two in case on the scaled technology, although the density of contacts with high thermal conductivity increases. So SH will become even more severe in future SOI technologies.

3.2 Impact of self heating on analog circuit performance

Using the equivalent circuit model, the impact of SH on FinFET circuits is investigated. R_{th} is obtained from simulations as described above, C_{th} from measurement and device simulations (Molzer et al., 2006) revealing a time constant of about 100ns and a maximum current reduction of about 10%. First a single-ended two stage OTA as presented above is analyzed in terms of it's transient response. A sinusoidal differential input signal is applied with a frequency of $f_{\text{sig}} \ll 1/\tau_{th}$. Figure 3.2 shows the impact of self heating on the output signal. The signal amplitude is decreased by about 2% through SH whereas the waveform is not affected. This is confirmed by the spectral analysis of this signal in Fig. 3.2. The second and third harmonic of the signal are even a touch lower in case of self heating, which can be explained by the decreased amplitude of the output signal. Consequently the impact of SH on the gain and the linearity of the amplifier is negligible here, although the current of a single transistor can be decreased by nearly 10%. This is attributed to the bias points typically chosen for amplifiers with moderate bandwidths. To reach a high g_m/I_D ratio V_{GS} is typically set to values in the range of 50 mV–300 mV above V_T leading to quite low current densities.

Next the impact of SH on comparator circuits is shown. A simple comparator structure with differential input stage, MOS diode loads and common source output is used as example. The adjacent latch is not considered here. In the simulation the differential input voltage is pulsed from a large (positive) value to a small (positive) residual voltage V_{res}, see Fig. 3.3. Without self heating, the comparator output voltage follows the input as intended. If self heating is included, the differential output voltage is negative for a certain period of time. This can be explained with the history of the comparator. Before the step of the input voltage, the devices providing the positive part of the differential output signal suffer much more from self heating than the devices providing the negative part. This situation remains for a short time after the step to small input values near common mode, yielding to strong thermal mismatch and a wrong comparator decision if the latch is activated at this point of time, see Fig. 3.3. The

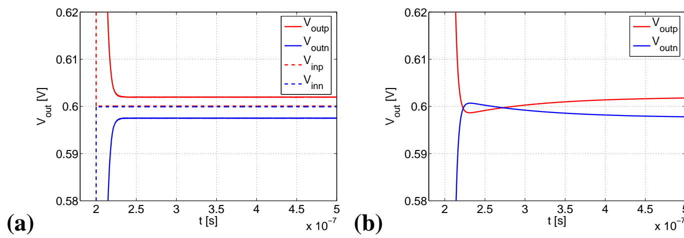

Fig. 8. Comparator input and output voltage without SH **(a)** and with SH **(b)** included.

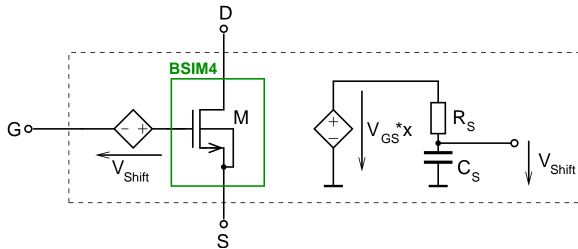

Fig. 9. Charge trapping equivalent circuit.

maximum residual voltage which causes wrong decisions is depending on the input signal, the comparator gain and the sampling time. In this scenario a V_{res} of 0.16 mV leads to a wrong decision for about 50ns. Assuming a reference voltage of 1V, self heating limits the performance of this comparator to a resolution of 12bit or sampling frequencies below 20 MHz. Thus SH is a potential issue for high speed, high resolution AD converters.

3.3 Charge trapping – modeling and impact on analog circuits

Another -not FinFET specific- effect is charge trapping in high-k materials. Under strong positive (in case of nFET) gate bias charges tunnel through the dielectric barrier and occupy free states in the dielectric material. Thereby the threshold voltage of the device is increased. Detrapping of charges is possible leading to a hysteresis effect as shown in Fig. 10. Material properties such as the dielectric itself (e.g. HfO_2) or the interface layer, temperature and bias conditions determine the amount of trapped charges (Ribes et al., 2005). Measured V_T shifts reach values in the range of 100 mV, while values around 10 mV are supposed to be tolerable for digital circuits. Time constants are reported from μs up to ms. For circuit simulations, an equivalent circuit model can be used (Fulde et al., 2006; Tewksbury and Lee, 1994) as shown in Fig. 9. The gate-source voltage is sensed and used to calculate the steady-state V_T shift via a voltage controlled voltage source. This voltage is applied to a RC network that creates an exponential time dependence and then subtracted from the gate-source voltage. Similar to the self heating effect, charge trapping causes transient variations of

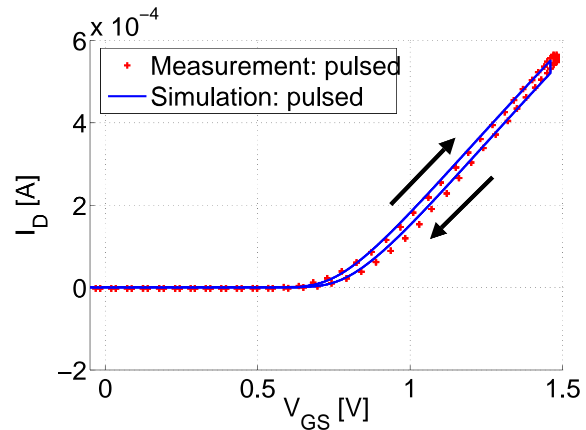

Fig. 10. Measurement and simulation of charge trapping effect.

the transistor current. Therefore the impact of charge trapping on circuit behavior is comparable. The linearity and gain of operational amplifiers is nearly not affected because the input devices see only a small signal oscillation of the gate-source voltage around the bias point. So the amount of charge trapping is almost constant over time. However charge trapping can cause erroneous comparator decisions as discussed above. The maximum residual voltage V_{res} that is necessary to modify the comparator decision is in the range of the maximum steady-state V_T shift. That means V_{res} can be much higher than in case of self-heating, e.g. in the mV regime. Fulde et al. (2006) shows how a dynamic V_T shift of a few mV can degrade the resolution of a 12bit SAR converter.

4 Conclusions

FinFETs offer a lot of interesting device features and show beneficial analog device properties. Primarily the low output conductance and the good matching behavior can be used to improve the figure-of-merit of typical analog applications as operational amplifiers or AD/DA converters. Nevertheless technology optimization, e.g. SEG, is still needed to eliminate parasitic effects like the high source-drain resistance or the matching issues for very narrow fins. Additionally new effects have to be considered in the design of analog circuits. Self heating and charge trapping influence transistor behavior significantly and introduce transient variations. Simple approaches based on equivalent circuit models enable an early assessment of the impact of such effects on circuit performance, revealing possible limitations for high speed, high resolution converters.

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References

Bertolissi, L.: Modeling and Simulation of Self-Heating Effects in Deep Sub-Micron Silicon on Insulator (SOI) Technologies for Analog Circuits, Ph.D. thesis, Universita Degli Studi di Udine, 2004.

Colinge, J.-P.: Novel Gate Concepts for MOS devices, in: IEEE Proceedings of the 34th European Solid-State Device Research conference, ESSDERC, 45–49, 2004.

Decoutere, S.: Perspectives of Downscaled CMOS for RFIC and mm-wave Applications, in: IEEE MTT-S International Microwave Symposium, 2006.

Fulde, M., Schmitt-Landsiedel, D., and Knoblinger, G.: Transient Variations in Emerging SOI Technologies: Modeling and Impact on Analog/Mixed-Signal Circuits, in: Proceedings of the IEEE International Symposium on Circuits and Systems, ISCAS, 2007.

Gustin, C., Mercha, A., Loo, J., Subramanian, V., Parvais, B., Dehan, M., and Decoutere, S.: Stochastic Matching Properties of FinFETs, IEEE Electron Device Letters, 27, 846–848, 2006.

Kinget, P. and Steyaert, M.: Impact of transistor mismatch on the speed-accuracy-power trade-off of analog CMOS circuits, in: Proceedings of the IEEE Custom Integrated Circuits Conference, CICC 1996, 333–336, 1996.

Knoblinger, G., Kuttner, F., Marshall, A., Russ, C., Haibach, P., Patruno, P., Schulz, T., Xiong, W., Gostkowski, M., Schruefer, K., and Cleavelin, C.: Design and evaluation of basic analog circuits in an emerging MuGFET technology, in: Proceedings of the IEEE International SOI Conference, 39–40, 2005.

Molzer et al., W.: Self Heating Simulation of Multi-Gate FETs, in: IEEE Proceedings of 36th European Solid-State Device Research conference, ESSDERC, 311–314, 2006.

Pacha, C., von Arnim, K., Schulz, T., Xiong, W., Gostkowski, M., Knoblinger, G., Marshall, A., Nirschl, T., Berthold, J., Russ, C., Gossner, H., Duvvury, C., Patruno, P., Cleavelin, R., and Schruefer, K.: Circuit design issues in multi-gate FET CMOS technologies, in: IEEE International Solid-State Circuits Conference, Digest of Technical Papers, 1656–1665, 2006.

Parvais, B., Gustin, C., de Heyn, V., Loo, J., Dehan, M., Subramanian, V., Mercha, A., Collaert, N., Rooyackers, R., Jurczak, M., Wambacq, P., and Decoutere, S.: Suitability of FinFET technology for low-power mixed-signal applications, in: IEEE International Conference on Integrated Circuit Design and Technology, ICICDT ’06, 1–4, 2006.

Pelgrom, M., Duinmaijer, A., and Welbers, A.: Matching properties of MOS transistors, IEEE Journal of Solid-State Circuits, 24, 1433–1439, 1989.

Ribes, G., Mitard, J., Denais, M., Bruyere, S., Monsieur, F., Parthasarathy, C., Vincent, E., and Ghibaudo, G.: Review on high-k dielectrics reliability issues, Device and Materials Reliability, IEEE Transactions on, 5, 5–19, 2005.

Schulz, T., Xiong, W., Cleavelin, C., Schruefer, K., Gostkowski, M., Matthews, K., Gebara, G., Zaman, R., Patruno, P., Chaudhry, A., Woo, A., and Colinge, J.: Fin thickness asymmetry effects in multiple-gate SOI FETs (MuGFETs), in: Proceedings of the IEEE International SOI Conference, 154–156, 2005.

Tewksbury, T.L., I. and Lee, H.-S.: Characterization, modeling, and minimization of transient thresholdvoltage shifts in MOSFETs, IEEE Journal of Solid-State Circuits, 29, 239–252, 1994.

van den Bosch, A., Borremans, M., Steyaert, M., and Sansen, W.: A 10-bit 1-GSample/s Nyquist current-steering CMOS D/A converter, IEEE Journal of Solid-State Circuits, 36, 315–324, 2001.