

Impact of process variations and long term degradation on 6T-SRAM cells

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Abstract. In modern deep-submicron CMOS technologies voltage scaling can not keep up with the scaling of the dimensions of transistors. Therefore the electrical fields inside the transistors are not constant anymore, while scaling down the device area. The rising electrical fields bring up reliability problems, such as hot carrier injection. Also other long term degradation mechanisms like Negative Bias Temperature Instability (NBTI) come into the focus of circuit design.

Along with process device parameter variations (threshold voltage, mobility), variations due to the degradation of devices form a big challenge for designers to build circuits that both yield high under the influence of process variations and remain functional with respect to long term device drift.

In this work we present the influence of long term degradation and process variations on the performance of SRAM core-cells and parametric yield of SRAM arrays. For different use cases we show the performance degradation depending on temperature and supply voltage.

that occur during the use of a product. Most of these long term effects happen under the influence of large electrical fields. Due to the scaling of the semiconductor devices and the under-proportional scaling of the supply voltage (ITRS, 2005) the electrical fields in UDSM technologies rise. Hence aging effects such as Hot Carrier degradation and Bias Temperature Stress (BTS) play an increasing role in CMOS circuit design.

SRAM arrays consume a large portion of the chip area in today's embedded systems, hence

The influence of long term degradation effects on the SRAM cell performance plays an important role in the design of embedded systems mainly due to two factors: a) SRAM arrays consume a large portion of the chip area in today's embedded systems and highly contribute to the system yield and b) SRAM devices use minimal feature sizes and therefore already drifts are accelerated.

1 Introduction

Increasing parametric variations due to the ongoing scaling of the semiconductor device dimensions determine more and more the circuit design in modern ultra deep-submicron (UDSM) CMOS technologies. Multiple variation mechanisms sum up to large deviations in the device characteristics.

On the one side, global variations introduced by the process lithographical width and length variation already decrease the device performance, on the other side the statistical dopant distribution under the gate area and process induced local variations like line edge roughness lead to local mismatch of neighboring devices, which further reduce the device performance in sub 100 nm technologies.

Additionally the circuit designer has to consider deviations in the device parameters due to long term variations

2 Negative Bias Temperature Instability (NBTI)

A Bias Temperature Stress (BTS) is most prominent when a p-Type MOSFET is biased in inversion. This Negative Bias Temperature Instability (NBTI) results in a higher absolute threshold voltage $|V_{th}|$ of the stressed p-MOSFET thus making the transistor harder to turn on. While the effect is not understood in full detail, it is widely accepted that positive charges are trapped near the Si/SiO_2 interface and induced interface states build up under high V_{gs} and high temperature (Ogawa, 1995). The stress induced damage is distributed homogeneously over the whole active area and the degradation on the threshold voltage is worst for a drain-source voltage of $V_{ds}=0$ while it shows lower degradation with higher V_{ds} (Schlunder, 2005). The stress conditions are shown in Fig. 1.

There is also an Biased Temperature Stress effect on positive biased n-type MOSFETs, but it shows only a minor change in the device characteristics.

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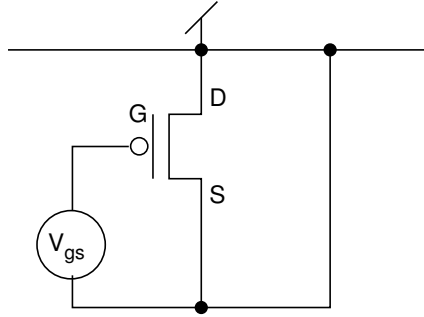


Fig. 1. Bias conditions for the Negative Bias Temperature Stress.

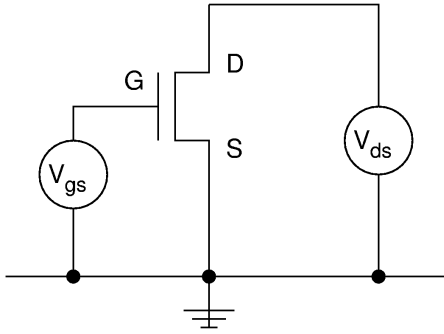


Fig. 2. Bias conditions for the Hot Carrier Stress.

The V_{th} shift due to NBTS partially recovers after device stress and AC operation has some annealing effects (Alam, 2003).

In UDSM technologies the degradation due to NBTI is becoming more critical due to the higher electrical fields across the gate resulting from the continuous size scaling without the proper voltage scaling (ITRS, 2005).

3 Hot Carrier Stress

Hot Carrier Stress is a long known hot electron induced degradation mechanism in CMOS semiconductors (Hu, 1985). Hot electrons coming from the high lateral electrical field cause electron-hole pairs by impact ionization. They can cause stress induced interface states and decrease the drain current I_d . The generated electrons can surmount the gate oxide barrier and cause the generation of trapped charges resulting in an increased threshold voltage V_{th} . The worst case operating conditions for Hot Carrier Stress are at drain-source voltages $V_{ds} > 0$ and a gate-source voltage of $V_{gs} \approx V_{ds}/2$ for n-type MOSFETs and $V_{gs} \approx V_{ds}/5$ for p-type MOSFETs (Bravaix, 1999). Figure 2 shows the stress conditions for HCS.

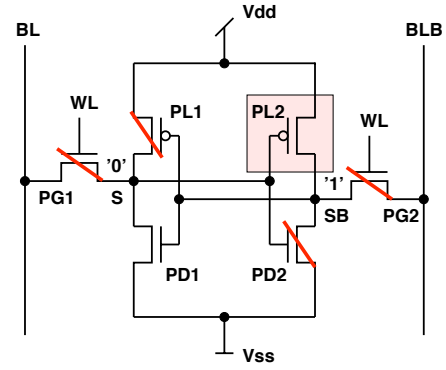


Fig. 3. SRAM core cell in hold operation. Transistor PL2 is subject to NBTS.

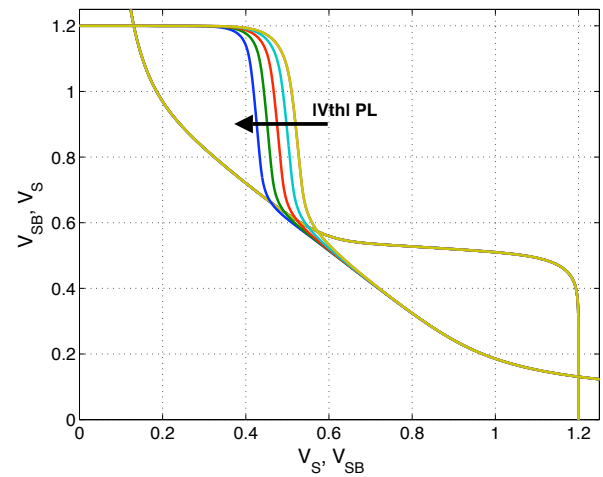


Fig. 4. Butterfly-curve for an SRAM core cell with activated word-line (read stability). The arrow shows the increase in $|V_{th}|$ of the p-type load transistor PL.

4 SRAM core cell stability degradation

An important key parameter of SRAM core cell circuits is the read stability. It describes the ability to read the information stored inside a memory cell without destroying the information. Measuring the Static Noise Margin (SNM) (Seevinck, 1987) on an SRAM cell with conducting access transistors gives a metric of the read stability.

When investigating the influence of device degradation on the performance of SRAM core cells the stress conditions of the different SRAM operating conditions have to be considered. In the following stress scenarios and the influence of the device degradation on the SNM performance of SRAM cells are investigated for data hold, read operation, and write operation.

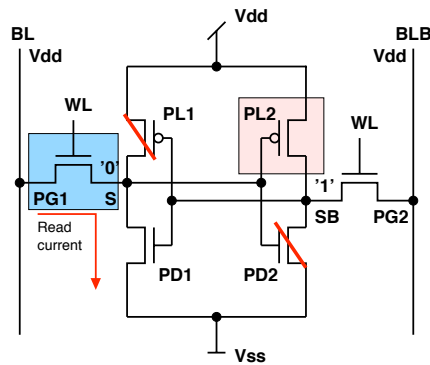


Fig. 5. SRAM core cell in read operation. Transistor PG1 is subject to HCS and Transistor PL2 to NBTS.

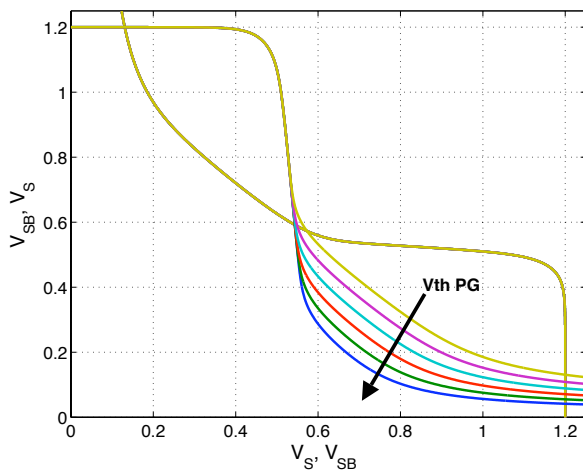


Fig. 6. Butterfly-curve for an SRAM core cell with activated word-line (read stability). The arrow shows the increase in V_{th} of the n-type access transistor PG1.

4.1 Data hold

In Fig. 3 the SRAM core cell is shown in hold operation. The two access transistors PG1 and PG2 are non-conducting and the information inside the memory cell is retained. The p-type load transistor PL2 on the “HIGH” side of the memory cell is exposed to a NBTS condition with a high field across the gate and no drain to source voltage. Whereas the p-type load transistor PG1 is non-conducting and sees no stress. In this operation mode of the core cell no Hot Carrier Stress can be expected due to the static nature of the hold state.

The NBTS on the PL2 transistor increases the threshold voltage $|V_{th}|$ of the p-MOSFET. This shifts the switching level of the inverter on the BLB side of the inverter to lower input voltages, thus reducing the eye opening of the butterfly curve that defines the read stability of the SRAM circuit (Fig. 4)

The stress to the p-type load transistor occurs whenever a

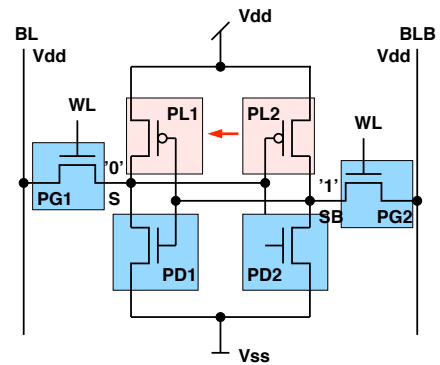


Fig. 7. SRAM core cell in write operation. The n-type transistors are subject to HCS, and NBTS changes from PL2 to PL1.

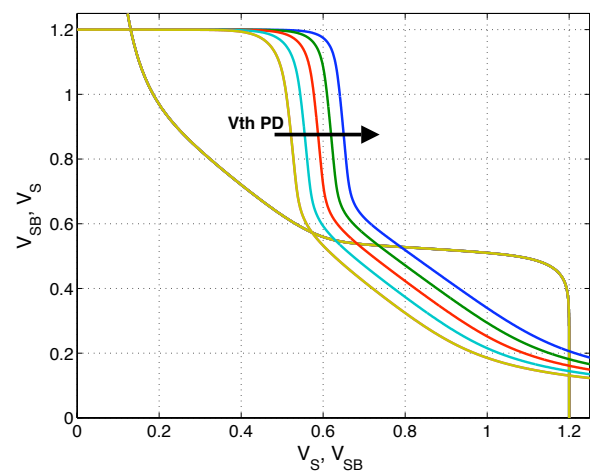


Fig. 8. Butterfly-curve for an SRAM core cell with open word-line (read stability). The arrow shows the increase in V_{th} of the n-type pull-down transistor PD.

“0” is stored on the storage node SB. In the worst case, when the data does not change, this stress is applied 100% of the operating time. The best case is at high switching activity, when the information is changed frequently so that the NBTS is present 50% of the time at each node and recovery and annealing effects also decrease the effect of the NBTS.

4.2 Data read

In the read operation the n-type word-line transistors are conducting and the two bit-lines, BL and BLB, are pre-charged to Vdd. A read current I_{read} flows through the transistors PG1 and PD1. Due to the read current and the high gate voltage the transistor PG1 is subject to HCS during the read operation. The aging of the access transistor PG1 increases the threshold voltage and decreases the drain current of the transistor. The p-type load device PL1 is still under NBTS,

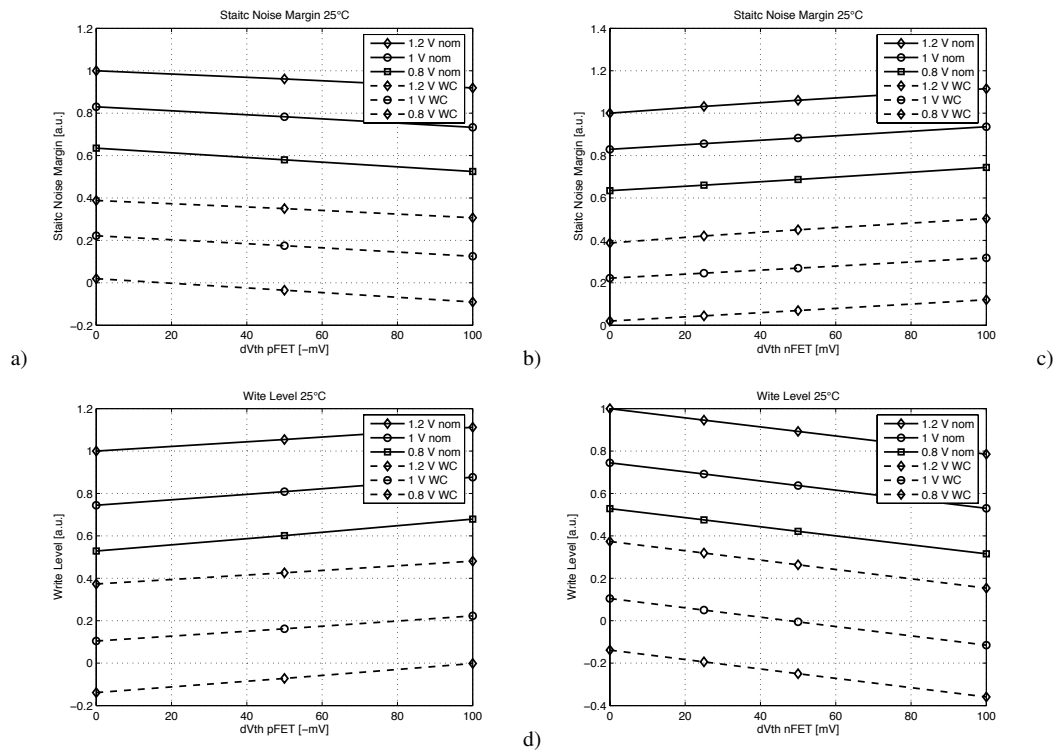


Fig. 9. Simulation results showing SRAM performance for nominal conditions (nom.) and worst case (WC) variation parameters for a 1MBit Array. **(a)** Static Noise Margin (read stability) vs. V_{th} -drift of p-FETs due to NBTS. **(b)** Static Noise Margin (read stability) vs. V_{th} -drift of n-FETs due to HCS. **(c)** Write Level (ability to write) vs. V_{th} -drift of p-FETs due to NBTS. **(d)** Write Level (ability to write) vs. V_{th} -drift of n-FETs due to HCS.

but sees a lower stress condition than in the hold state, due to the raised voltage level on node “S” (s. Fig. 5).

The influence of the threshold voltage increase of transistor PG1 on the read stability of the SRAM core cell is shown in Fig. 6. The voltage at node ‘S’ decreases due to the lower drain current and the eye of the butterfly curve opens.

A large number of read operation on one side of the SRAM cell stresses the access transistor, but influences the read stability in a positive way.

4.3 Data write

During the write operation the content of an SRAM core cell is changed. Therefore all transistors change their operating conditions and are stressed during the transition. The n-type access transistors and the pull-down devices are all subject to HCS due to the active current flowing in the switching process of the write operation. After the switching event the NBTS changes from transistor PL2 to PL1.

Figure 8 shows the influence of the threshold voltage increase of the transistor PD due to HCS. The increase in V_{th} changes the switching level of the core cell to higher input voltages. The voltage level defined by the voltage divider PG1/PD1 on the node “S” increases due to the weaker tran-

sistor PD1. This results in a smaller eye-opening of the butterfly-curve and a smaller read stability.

A large number of write operations stresses the core cell most due to the high number of switching events. This decreases the read stability.

5 Simulations

The impacts of the above described aging mechanisms on the performances of an SRAM array was simulated using a worst case distance simulation (Fischer, 2005) (Antreich, 1994). This simulation method allows to simulate the worst case performance for an SRAM array with a given array-size considering process variations and local mismatch. The simulations were performed for the Static Noise Margin (SNM) with conducting access transistors to obtain the read stability and for the Write Level that measures the ability to write an SRAM cell.

Figure 9a shows the degradation of the SNM on nominal SRAM core cells and on cells with worst case variations due to process and mismatch. The V_{th} shift of the threshold voltage of the p-type transistors results from NBTS. The read stability decreases with the V_{th} degradation. On the other hand

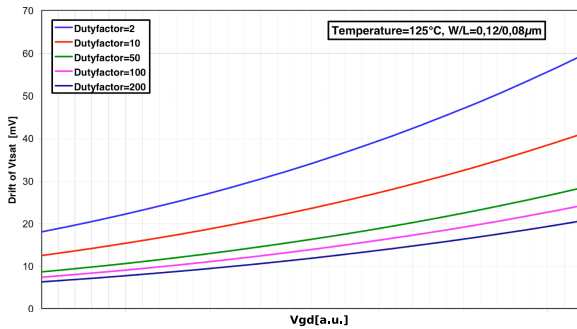


Fig. 10. The interrelation of stress voltage, duty factors, and the drift of NBTS induced threshold voltage.

the SNM increases with the a shift in the threshold voltage of the n-type transistors affected by HCS (Fig. 9b).

The ability to write, measured by the Write Level, shows the opposite behavior. When the core cell is subject to NBTS the Write Level rises with increasing V_{th} degradation and decreases with n-FET aging caused by the HCS (s. Figs. 9c and d).

It is therefore necessary to know the aging parameters and the worst case use scenarios to quantify the effect of NBTS and HCI on the SRAM performances. Figure 10 exemplary shows the interrelation of stress voltages and duty cycles and the drift of NBTS induces threshold voltage.

6 Yield considerations

The simulated Worst Case Distances, as a measure of the variation induced yield, show an increase of the total variation of 0.25 sigma for a 25 mV NBTS V_{th} shift of the p-type load transistors. The yield of an SRAM array is calculated using the simulated Worst Case Distance (WCD) and array size N (Fischer, 2005).

$$\text{Yield} = \left(\frac{1}{2} \left(1 + \operatorname{erf} \left(\frac{WCD}{\sqrt{2}} \right) \right) \right)^N \quad (1)$$

Figure 11 shows the yield for a 256 k SRAM calculated from the specification of the read stability. A 25 mV NBTS induced threshold voltage shift of the p-type transistor lowers minimum supply voltage by 50 mV.

7 Conclusions

We have shown the qualitative influence of Hot Carrier Stress and Negative Bias Temperature Stress on the read stability of SRAM core cells for different operating conditions. The differing impact on the aging mechanisms depending on the operation mode of the SRAM cell needs a thorough analysis of the use case of the SRAM array. With the drift values for the individual use cases simulations show the quantitative impact

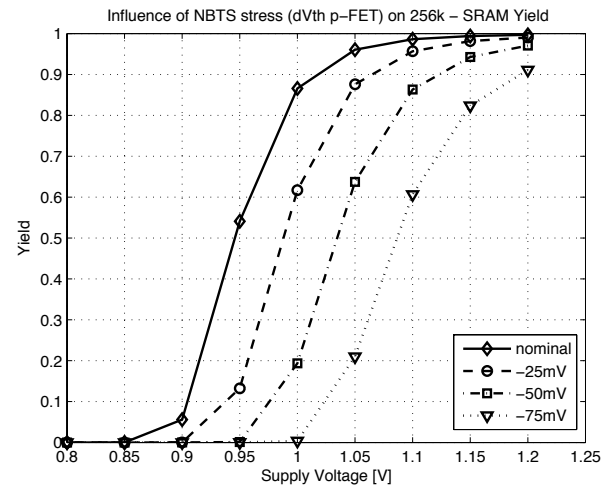


Fig. 11. The impact of NBTS induced V_{th} degradation on the read stability limited yield of a 256 k SRAM array.

on read and write performance for the total variation, including process variation, mismatch and stress degradation. The yield can be calculated and its influence on system specifications such as minimum supply voltage can be determined.

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