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Results and limits in the 1-D analytical modeling for the asymmetric DG SOI MOSFET

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Abstract. This paper presents the results and the limits of 1-D analytical modeling of electrostatic potential in the low-doped p type silicon body of the asymmetric n-channel DG SOI MOSFET, where the contribution to the asymmetry comes only from p- and n-type doping of polysilicon used as the gate electrodes. Solving Poisson's equation with boundary conditions based on the continuity of normal electrical displacement at interfaces and the presence of a minimum electrostatic potential by using the Matlab code we have obtained a minimum potential with a slow variation in the central zone of silicon with the value pinned around 0.46 V, where the applied V_{GS} voltage varies from 0.45 V to 0.95 V. The paper states clearly the validity domain of the analytical solution and the important effect of the localization of the minimum electrostatic potential value on the potential variation at interfaces as a function of the applied V_{GS} voltage.

1 Introduction

It is generally accepted that the dual-gate (DG) SOI MOSFET device represents a reliable solution of the scaling down of the SOI ULSI circuits to the lowest technological sizes. On the other hand, this DG concept removes the short channel effects and gives a good electrostatic control of the channel charge by the gate voltage (Thompson et al., 1998).

For the same type of the gates materials, doping and dielectric layers, a symmetric DG SOI MOSFET is obtained, while any technology differences at the gate or dielectric level will imply the asymmetry of the device. In the last years, 1-D analytical modeling of both symmetric (Taur, 2000; Cobianu and Glesner, 2006; Cobianu et al., 2006; Malobabic et al., 2004) and asymmetric (Taur, 2001) DG SOI MOSFETs has been used for the description of their DC electrical behavior and the understanding of the device physics.

The analytical approach of Poisson's equation was possible by using only the inversion charge and ignoring the fixed charge due to the lightly silicon doped film specific to this DG SOI technology. One of the important results of the above modeling assumptions was the demonstration of the volume inversion in the ultrathin silicon film of SOI MOSFET devices (Balestra et al., 1987).

However, only a few modelling results were presented for the asymmetric devices, without description of the used procedure and a clear presentation of the validity domain. It is the purpose of our paper to present detailed results and limitations of the 1-D analytical modelling of the asymmetric DG SOI MOSFET and to show its differences compared to the symmetric case.

The paper will present the background and the assumptions of the analytical modelling, followed by our detailed mathematical approach which includes the identification of the definition domain for the involved model parameters and the limitations of the calculation of the electrostatic potential as a function of the applied V_{GS} voltage.

2 Background of the 1-D analytical modelling

All the analytical modelling results from this paper will be related to the n-channel DG SOI MOSFET, where the silicon thickness of the p-type silicon substrate (t_{Si}) is equal to 20 nm, while the $Si\,O_2$ gates dielectric thicknesses (t_{ox}) are equal to 2 nm. The geometry and the band diagram of the asymmetric DG SOI MOSFET are presented in Fig. 1 (Taur, 2001), where one can be observed that, due to p and n type doping of the two gates at thermal equilibrium, one silicon surface is already in inversion, while the other becomes accumulated due to the differences in the work functions of gates materials and silicon substrate.

For slightly doped silicon film of the asymmetric DG SOI MOSFET, the analytical approach was similar to the symmetrical case, where a minimum of electrostatic potential, ψ_0, was assumed in the silicon body, at the position x_0, but not exactly located in the center of the Si layer as in the case of symmetrical DG SOI MOSFET. Thus, the calculation of the electrostatic potential was done by means of Poisson's

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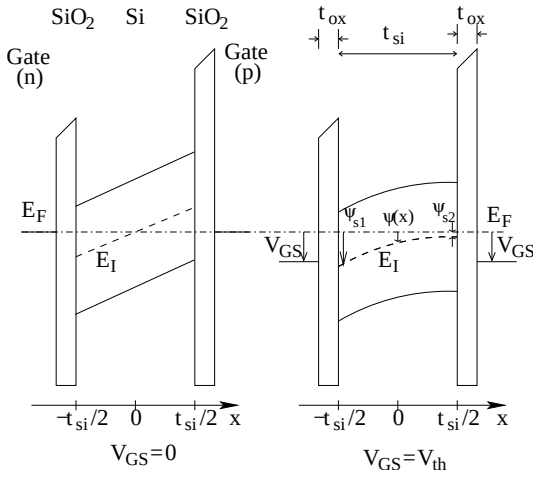

Fig. 1. Schematic band diagrams of an asymmetric, undoped DGn-MOSFET (Taur, 2001).

equation and the specific boundary conditions as shown below:

$$\frac{d^2\psi}{dx^2} = \frac{qn_i}{\varepsilon_{si}} \cdot e^{\frac{q\psi}{kT}} \tag{1}$$

$$\frac{d\psi}{dx}|_{x=x_0} = 0 \tag{2}$$

$$\varepsilon_{si} \cdot \frac{V_{GS} - \psi_{s1} - \Delta\phi_1}{t_{ox}} = \varepsilon_{ox} \cdot E_{si}|_{x=-\frac{t_{si}}{2}} \tag{3}$$

$$\varepsilon_{si} \cdot \frac{V_{GS} - \psi_{s2} - \Delta\phi_2}{t_{ox}} = \varepsilon_{ox} \cdot E_{si}|_{x=\frac{t_{si}}{2}} \tag{4}$$

In the above equations, $\Delta\phi_1$ and $\Delta\phi_2$ are the work function differences of n doped gate and p doped gate, respectively, while E_{si} represents the electric field at the corresponding Si/SiO_2 interfaces.

The Eqs. (3) and (4) represent the continuity of the normal component of the electrical displacement at the two interfaces between silicon and dielectrics. We also assume the presence of the minimum electrostatic potential in the silicon layer at relatively higher V_{GS} voltages (Taur, 2000, 2001).

By the integration of the Poisson's equation with its boundary conditions giving a minimum electrostatic potential (ψ_0) at the position x_0, one obtains the solution for the electrostatic potential as shown below:

$$\psi(x) = \psi_0 - \frac{2kT}{q} \cdot ln[\cos(b \cdot e^{\frac{q\psi_0}{2kT}} \cdot (x - x_0)] \tag{5}$$

where $b = \sqrt{\frac{q^2 n_i}{2\varepsilon_{si} kT}}$.

At low applied gate voltages, Taur has assumed a constant electrostatic field in minimum electrostatic potential was found at 0.462 V being located near the center of Si layer (Taur, 2001).

3 Clarifications and new results of 1-D analytical modelling

An important limitation of 1-D analytical modelling of the DG SOI MOSFET is given by the use of only electron mobile inversion charge in the Poisson's equation. This assumption is valid for very low substrate doping and by neglecting the hole mobile charge. In our case, for a better validation of the model assumption, we have used the p-type substrate doping equal to $N_B = 10^{15}\,\mathrm{cm}^{-3}$ which is a much lower value than the one described in the literature (Taur, 2001). Based on our calculations, the electrostatic potentials higher than 0.37 V will make negligible the influence of (mobile) holes and fixed depleted charge in the above Poisson's equation. For our N_B value, the Fermi level is located below the intrinsec Fermi level, E_i, and at 0.24 eV above E_v.

From the Eqs. (3) and (4) from above and the dependence given by Eq. (5), we have derived the explicit system that provides the minimum electrostatic potential (ψ_0) and its location (x_0) in silicon body, as it follows:

$$\begin{aligned} V_{GS} - \psi_0 - \Delta\phi_1 \\ = -a \cdot e^{\frac{q\psi}{2kT}} \cdot \tan(b \cdot e^{\frac{q\psi_0}{2kT}} \cdot (-\frac{t_{si}}{2} - x_0)) \\ -\frac{2kT}{q} \cdot ln\{\cos(b \cdot e^{\frac{q\psi_0}{2kT}} \cdot (-\frac{t_{si}}{2} - x_0))\} \end{aligned} \tag{6}$$

$$\begin{aligned} V_{GS} - \psi_0 - \Delta\phi_2 \\ = -a \cdot e^{\frac{q\psi}{2kT}} \cdot \tan(b \cdot e^{\frac{q\psi_0}{2kT}} \cdot (\frac{t_{si}}{2} - x_0)) \\ -\frac{2kT}{q} \cdot ln\{\cos(b \cdot e^{\frac{q\psi_0}{2kT}} \cdot (\frac{t_{si}}{2} - x_0))\} \end{aligned} \tag{7}$$

where $a = \frac{t_{ox} \cdot \sqrt{2\varepsilon_{si} kT n_i}}{\varepsilon_{ox}}$.

From the Eqs. (6) and (7), we see that the solutions ψ_0 and x_0 should be in the definition domains of natural logarithmic function and the tan function. Thus, the conditions for the existence of the logarithm function and tan function are:

$$\psi_0 < \frac{2kT}{q} \cdot ln\{\frac{\pi}{2b(\frac{t_{si}}{2} + x_0)}\} \tag{8}$$

$$\psi_0 < \frac{2kT}{q} \cdot ln\{\frac{\pi}{2b(\frac{t_{si}}{2} - x_0)}\} \tag{9}$$

From the relations Eqs. (8) and (9), one can estimate an upper limit value of the minimum electrostatic potential (ψ_0), by assuming the localization (x_0) of this minimum in the center of the silicon body. For this case, we calculated an upper limit value of ψ_0 equal to 0.4643 V. Thus, according to our model, device geometry and above assumption, we prove that the minimum electrostatic potential should be in the range from 0.37 V to 0.4643 V.

In the same time, for finding the definition domain of the tan function, we need to eliminate those values of (x_0,

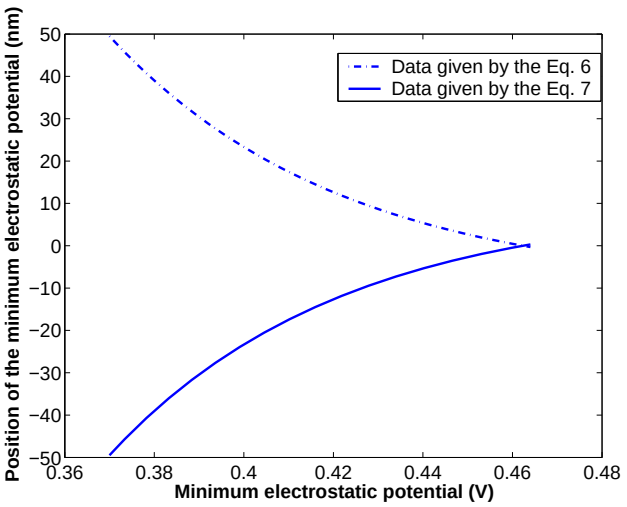

Fig. 2. The domain of definition for both minimum electrostatic potential and its localization.

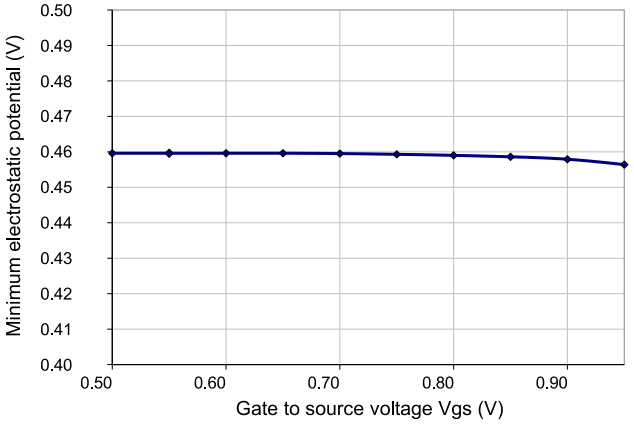

Fig. 3. The dependence of minimum electrostatic potential as a function of the applied gate potential.

ψ_0) which determine an infinite value of the function. Such (x_0, ψ_0) pairs are obtained by transforming the inequalities Eqs. (8) and (9) into equalities and solving the coresponding system. Based on this approach, in Fig. 2, we present the two plots with the data points which do not belong to the definition domain for x_0 and ψ_0.

Therefore, the final value of the two-dimensional definition domain of our 1-D analytical modelling and chosen geometry is considered as follows:

$$(x_0;\, \psi_0) \in (((-10\,\text{nm}, 10\,\text{nm}) \times (0.37\,\text{V}, 0.4643\,\text{V})) - (x_0;\, \psi_0)_{\text{plot}})$$

where $(x_0;\, \psi_0)_{\text{plot}}$ represents the data points located in the two plots in Fig. 2.

Now, after we have found the definition domain, we have solved the system of Eqs. (6) and (7) in the Matlab code, by means of an iterative method which provides the x_0, ψ_0 solutions as it follows. Firstly, we introduce the following notations:

$$f_1 = V_{GS} - \psi_0 - \Delta\phi_1 \tag{10}$$

$$g_1 = -a \cdot e^{\frac{q\psi}{2kT}} \cdot \tan(b \cdot e^{\frac{q\psi_0}{2kT}} \cdot (-\tfrac{t_{si}}{2} - x_0)) - \tfrac{2kT}{q} \cdot ln\{\cos(b \cdot e^{\frac{q\psi_0}{2kT}} \cdot (-\tfrac{t_{si}}{2} - x_0))\} \tag{11}$$

$$f_2 = V_{GS} - \psi_0 - \Delta\phi_2 \tag{12}$$

$$g_2 = -a \cdot e^{\frac{q\psi}{2kT}} \cdot \tan(b \cdot e^{\frac{q\psi_0}{2kT}} \cdot (\tfrac{t_{si}}{2} - x_0)) - \tfrac{2kT}{q} \cdot ln\{\cos(b \cdot e^{\frac{q\psi_0}{2kT}} \cdot (\tfrac{t_{si}}{2} - x_0))\} \tag{13}$$

Based on the above relations, the system formed on Eqs. (6) and (7) becomes:

$$h_1 = f_1 - g_1 = 0 \tag{14}$$

$$h_2 = f_2 - g_2 = 0 \tag{15}$$

The above system of equations is solved by considering the work function differences $\Delta\phi_1$=−0.56 eV (between the n-type gate electrode and the intrinsic silicon) and $\Delta\phi_2$=0.56 eV (between the p-type gate electrode and the intrinsic silicon). As the system has no analytical solutions, we have solved it by using a numerical approach . For each applied V_{GS} voltage in the range of (0.5 V, 0.95 V) and x_0 values in the domain (−10 nm, 10 nm), we calculate the values of h_1 and h_2 for ψ_0 ranging from 0.37 V to 0.4643 V. The solution of the system given by relations Eqs. (14) and (15) is found for those (x_0; ψ_0) values that satisfy the conditions written below:

$$\text{abs}(h_1) < 10^{-6} \tag{16}$$

$$\text{abs}(h_2) < 10^{-6} \tag{17}$$

From the above system, for V_{GS} variation in the range from 0.5 V to 0.95 V, we obtain a minimum electrostatic potential dependence as shown in Fig. 3. Solutions x_0 of the positions of the minimum electrostatic potentials were found closed to the center of silicon film, but the difficulty associated with their extraction will be commented later.

From Fig. 3, we see for the first time a pinning effect of the minimum electrostatic potential as a function of the applied V_{GS} voltage for asymmetric DG SOI MOSFET devices. If we consider the minimum electrostatic potential dependence in Fig. 3 and look at the qualitative energy band diagrams in Fig. 1, it is easy to understand that, at V_{GS} higher than 0.5 V, the Fermi level in the silicon body is closed to bottom of the conduction band for the whole silicon body which demonstrates the presence of the volume inversion even in the case

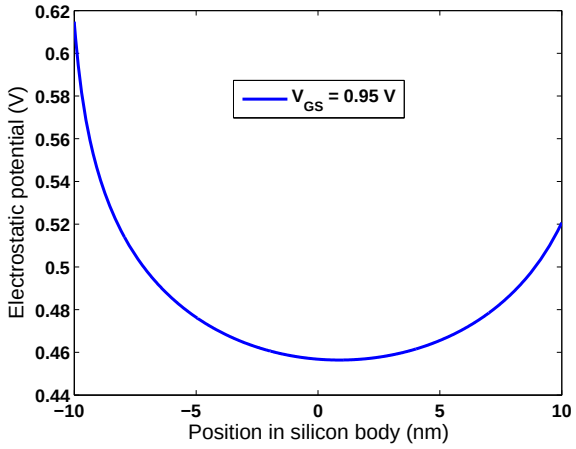

Fig. 4. The dependence of electrostatic potential as a function of position in silicon body for an applied gate-to-source voltages of 0.95 V.

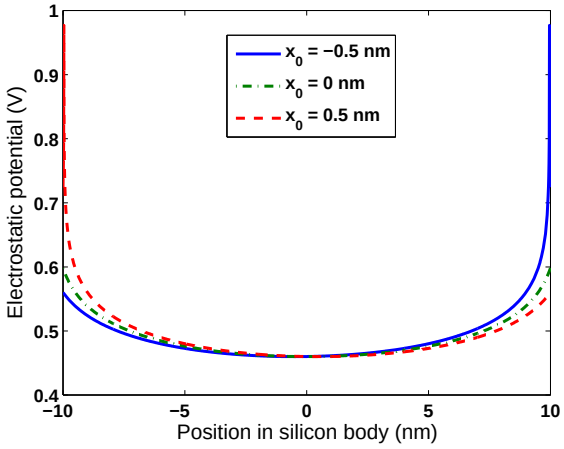

Fig. 5. The distribution of the electrostatic potential as a function of position in silicon body, with different minimum locations at the constant value of the minimum of 0.46 V.

of asymmetric DG SOI MOSFET. This volume inversion can also be demonstrated by representing the electrostatic potential profile as a function of the position in the silicon body of the DG SOI MOSFET. Such result is presented in Fig. 4 by means of Eq. (5), where we show the dependence of electrostatic potential as a function of position in silicon body for an applied V_{GS} voltage equal to 0.95 V. That plot was obtained for a ψ_0=0.4564 V and x_0=0.878 nm.

From Fig. 4, we notice that the electrostatic potential is much higher at the interface with n-doped polysilicon gate, which can be understood from the initial bands bending of the silicon layer due to the work function differences at thermal equilibrum. This figure, also, shows a wide sink shape of the electrostatic potential in the middle of the silicon body, which makes its minimum location to be a difficult numerical task. In his paper (Taur, 2001), Taur has presented a calculation of the electrostatic potential only for an applied voltage V_{GS}=1.4 V and he obtained the minimum electrostatic potential of 0.462 V located at 0.425 nm, far from the center of silicon layer. Unfortunately, the paper was not focussed on the description of more details about method used to obtain the results. If we make an analyses of our and Taur's results, we can deduce that the minimum electrostatic potential is further maintained up to a rather constant value of V_{GS}=1.4 V. Actually, due to a flat profile of the electrostatic potential in the central region of silicon body as shown in Fig. 4, one can understand the difficulty of extracting position of the minimum electrostatic potential. Thus, the coordinates of the minimum electrostatic potential are very critical for the calculation of the electrostatic potential distribution in the entire silicon body.

In order to prove the sensitivity of the electrostatic potential distribution to the location of its minimum, in Fig. 5, we present the effect of a slight variation in x_0 position on the shape of the entire distribution. In this example, we have considered three arbitrary values in the position of minimum electrostatic potential in the range from −0.5 nm to +0.5 nm around the center of silicon layer, but we kept constant the value of the minimum electrostatic potential equal to 0.46 V.

From this figure, one can see high differences for the electrostatic potential at the two interfaces in the three cases, where some of the interface potential values not even having a physical meanings. In the same time, in the central silicon region, the effect of different locations on the electrostatic distributions is very weak.

Overall, despite the sensitivity of the results to the accuracy of the numerical calculations, our approach has shown the capability of the 1-D modelling to provide a good understanding of the physics of the asymmetric DG SOI MOSFET devices, where volume inversion is found for a typical defined geometry and biasing.

4 Conclusions

This paper has shown the results and limits of a 1-D analytical modelling for the electrostatic potential distribution in the very slightly doped silicon body of the asymmetric DG SOI MOSFET devices, where the asymmetry was given by the different p or n type doping of the polysilicon gate electrodes.

For applied V_{GS} voltages higher than 0.5 V, the Poisson's equation was analytically solved by using only electrons as charge carriers and boundary conditions given by the continuity of the electric displacement at the two interfaces and the presence of a minimum electrostatic potential in the silicon body.

Analytical approach was done in two steps. In the first step, the coordinates of the minimum electrostatic potential

were derived, while in the second step the electrostatic potential distribution was obtained. The analytical functions involved in the modelling have restricted the coordinates of the minimum potential value to a well-defined 2-D existence domain.

An iterative method performed in the Matlab code was used for the calculation of the coordinates of the minimum electrostatic potential. At the end of this process, we have demonstrated for the first time that, when the applied V_{GS} voltage varied from 0.5 V to 1 V, the minimum electrostatic potential was pinned at a value of about 0.459 V rather similar with the pinning phenomenon shown in the analytical modelling of symmetric DG SOI MOSFET.

The coordinates of the above minimum allowed us the calculation of the electrostatic potential distribution in the whole silicon body. This potential distribution has had a wide sink shape minimum pinned at such a value which assures a volume inversion in the silicon body for V_{GS} higher that 0.5 V. However, the entire analytical modelling process has shown a very high sensitivity of the near interface electrostatic potentials to the position of its minimum from the central region, where for only 0.5 nm variation in that location, very high changes in the electrostatic potential from interfaces appeared.

Despite the sensitivity of the electrostatic potential solution to the accuracy of its minimum localization, our theoretical study described in this paper has shown that the 1-D analytical modelling is a powerful tool to understand the physics of asymmetric DG SOI MOSFET devices and to prove a volume inversion for a typical geometry and biasing.

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