**Advances in
Radio Science**

A 3rd-order current-mode filter in $0.12\,\mu$m CMOS

R. Kolm and H. Zimmermann

Vienna University of Technology, Institute of Electrical Measurements and Circuit Design, Gusshausstraße 25/354, 1040
Vienna, Austria

Abstract. For software radio applications in system-on-chips, a 3rd-order current-mode Butterworth filter in 120 nm CMOS is realized. This filter is used for reconstruction purposes between a current-steering DAC and a current-mode mixer. Power can be reduced by using a current-mode architecture. The cut-off frequency of this filter is switchable between 1 MHz and 4 MHz, the current consumption is 4.5 mA at V_{DD}=1.5 V, the inband noise density is $100\,\mathrm{pA}/\sqrt{Hz}$ and it has a dynamic range up to 65 dB.

1 Introduction

The integration of analog and digital functions can be achieved only when analog sections are also designed with low-voltage and short-channel devices. As a consequence of the low supply voltage the dynamic range and the signal-to-noise ratio are reduced Annema et al. (2005).

The transmit path of a software radio system consists of a DAC, a filter and a mixer (see Fig. 1). For the DAC the current-steering architecture is a good opportunity because it has a high accuracy and high speed and can drive low ohmic loads and large capacitive loads. But it would be necessary to transform the current at the DAC output into a voltage when it is applied to a voltage-mode filter. Also if the signal at the filter output is applied to a current-mode mixer, the voltage must be converted into a current. The electrical power, which is used for the conversions, can be reduced, if a current-mode low-pass is used. In our case the power savings amount to 4 mW.

Current-mode design can be defined as the processing of current signals in an environment where voltage signals are irrelevant in determining circuits. Usually current-mode circuits have low impedance nodes such that voltage swings are small. To obtain a high power-supply rejection ratio and to suppress common-mode noise and even-order distortions we use a fully differential topology.
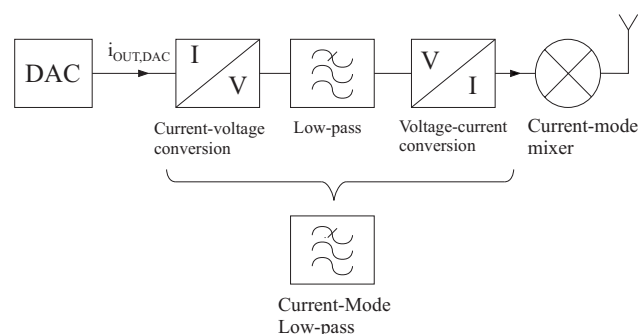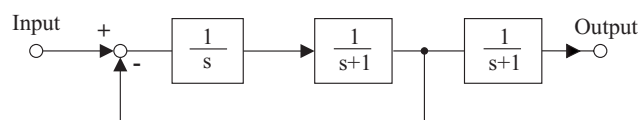
Fig. 1. Transmit path of a software radio.

Fig. 2. Block diagram of the filter.

2 Filter design

For the design of current-mode filters in principle two architectures were possible (Ramirez-Angulo et al., 1992). The G_m-C approach is discussed in Manhattanakul and Toumazou (1998) in a very detailed way. Our filter is realized with the second possible approach which consists of current-mirrors and are discussed in Smith and Sanchez-Sinencio (1996), Zele and Allstot (1996). The realized filter is a 3-order Butterworth configuration with the block-diagram shown in Fig. 2. For simplicity the differential signal paths are only shown as single wires. This Butterworth-filter consists of an integrator and a first-order low-pass in a feedback loop configuration and a first-order low-pass. An integrator in a fully differential way can be realized by two cross-coupled one-to-one current mirrors (see Fig. 3) and an integration capacitor. The cross interconnection provides a high differential gain and a low common-mode gain. The resistors R_0 improve the linearity performance and reduce the flicker

Fig. 3. Current-mode integrator.

Fig. 4. 2nd and 3rd stage.

noise. The cut-off frequencies are controlled by switchable capacitors. The reason to switch capacitors instead of resistors is because the noise level should not change in the passband. The transfer function of this integrator is given by

$$H_{\text{int}}(s) = \frac{1}{(R_0 + 1/g_m) \cdot C \cdot s}. \tag{1}$$

The third harmonics of the current i_{1p}, i_{1n} can be calculated from Smith and Sanchez-Sinencio (1996) by

$$HD3 = \frac{1}{32 \cdot N^2} \cdot \left(\frac{i_{in}}{2 \cdot I_B}\right)^2 \tag{2}$$

where i_{in} is the amplitude of the input current and N denotes the source degeneration factor and is

$$N = 1 + g_m R_0. \tag{3}$$

We chose for the degeneration factor N=2.66 which improves the third harmonics by 11.3 dB. The output current of this integrator i_{1p}, i_{1n} is now mirrored to the second stage. This stage consists of a first-order low-pass which is formed by current-mirrors (see Fig. 4) and decoupling RC-low-passes. The time constant (R_2, C_2) of this low-pass defines the second filter pole. The output-currents of this low-pass (i_{2n}, i_{2p}) are now fed back negatively to the input of the integrator (this means that the drain of M17 is connected to the drain of M2 respectively the drain of M18 is connected

to the drain of M1). The current through the transistors M15 and M16 are now applied to a further low-pass (R_3, C_3) and mirrored then to the output transistors M19 and M20.

The entire transfer function of this filter is given by

$$H(s) = \frac{i_{\text{outp}}}{i_{\text{inp}}} = \frac{i_{\text{outn}}}{i_{\text{inn}}} =$$

$$= \frac{1}{1 + s/(\omega_0 Q) + s^2/\omega_0^2} \cdot \frac{1}{1 + s/\omega_3} \tag{4}$$

with the filter parameter

$$Q = \sqrt{\frac{R_2 C_2}{(R_0 + 1/g_{m1,2}) C_1}}, \tag{5}$$

$$\omega_0 = \sqrt{\frac{1}{(R_0 + 1/g_{m1,2}) R_2 C_2}}, \tag{6}$$

$$\omega_3 = \frac{1}{R_3 C_3}. \tag{7}$$

A Butterworth chararcteristics can be obtained if the quality factor Q is set to 1 and if the condition $\omega_0 = \omega_3$ is satisfied.

3 Measured results

This filter with a switchable cut-off frequency of 1 MHz and 4 MHz was fabricated in a standard digital 120 nm CMOS process. To keep the production costs low, it was the goal to use only technology options which are available in the purely digital technology. In this design, therefore, only regular-threshold transistors are used. The chip photomicrograph of the chip is shown in Fig. 5. Due to the passivation layer and the planarization of the metal layers almost only the upper metal layer can be seen on the chip photo. To illustrate more

Fig. 5. Chip photomicrograph of the realized filter.

Fig. 7. Amplitude frequency response.

Fig. 6. Layout plot of the realized filter.

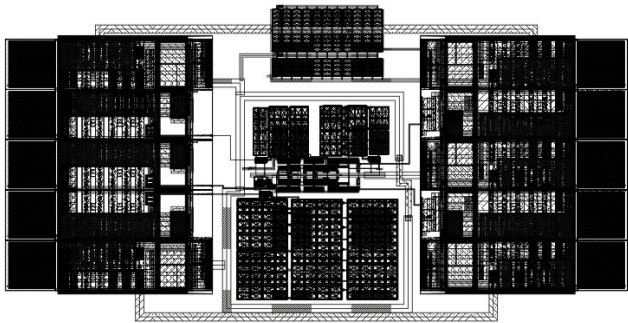**Fig. 8.** Amplitude frequency response.

details also a layout plot of the filter is presented in Fig. 6. The measured current consumption is 4.5mA at V_{DD}=1.5V, the chip area including the pads is 850 μm$\times$400 μm, the chip area of the filter is 350 μm$\times$240 μm.

All measurements were done in a fully differential way. The AC and distortion measurement were done with a differential probe, for the noise measurement a low-noise differential-to-single-ended amplifier was used. In Fig. 7 the measured DC-transfer characteristics is shown. The curve is linear for an input current of $\pm$280 μA and it has an offset of 15 μA. In Fig. 8 the amplitude frequency response and in Fig. 9 the phase frequency response is shown. The filter characteristics falls with $-$60 dB/decade in the cut-off region, it has no resonance peak, the 3 dB cut-off frequencies are 1.28 MHz and 4.18 MHz and the DC gain is $-$0.4 dB.

In Table 1 we present the measured spectral components for a single-tone measurement. From theory it is expected for a fully differential circuit that the distortions of even order, however, are not cancelled completely in practice.

For the characterization of the linearity near the corner frequency a 2-tone measurement is also necessary. The third-order intermodulation (IM3) of this filter is for a 2-tone input signal of 145 μA (the two-tone signals have the frequencies of 700 kHz and 800 kHz for the filter with f_C=1 MHz and 3.2 MHz and 3.4 MHz for the filter with f_C=4 MHz) $-$40 dB. This corresponds to an IIP3 (input 3rd-order intercept point of 1.45 mA$_p$.
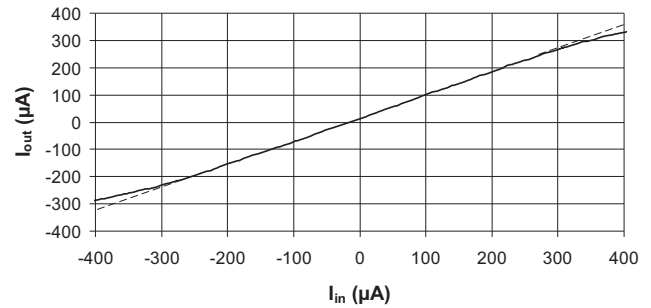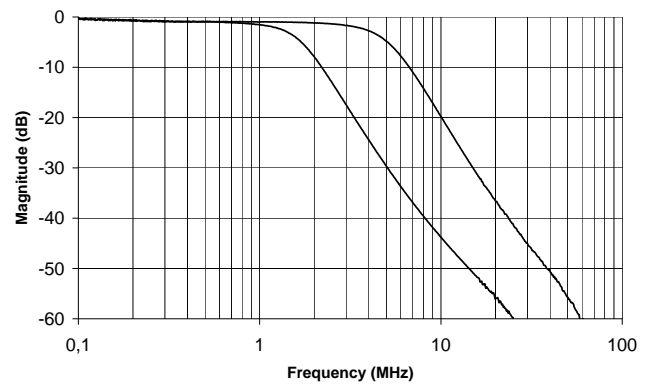
In Fig. 10 the measured noise spectral density at the filter output is shown. The noise is in the passband 100 pA/$\sqrt{Hz}$. To calculate the integrated noise, the spectral density in the passband is multiplied with the cut-off frequency. This gives a good approximation due to the fact that noise falls with $-$60 dB/decade in the cut-off region. This gives an integrated noise of 100 nA$_{rms}$ for the filter with f_C=1 MHz and 200 nA$_{rms}$ for the filter with f_C=4 MHz.

An important parameter to characterize analog filters is the dynamic range (DR). It is defined as the ratio of the maximum and minimum signal level which the circuit can handle at the same time. The minimum signal level is determined by the noise of the filter, the maximum level is mostly described by the level when the signal reaches a THD of 1%. So the DR can be expressed as

$$\text{DR} = \frac{\widehat{i}^2_{1\%\text{THD}}/2}{i^2_{\text{noise}}}. \tag{8}$$

With the above values we obtain now a DR of 65 dB for the filter with f_C=1 MHz and a DR of 59 dB for the filter with f_C=4 MHz
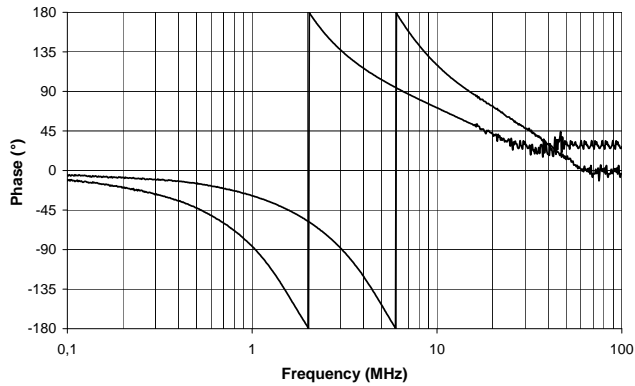
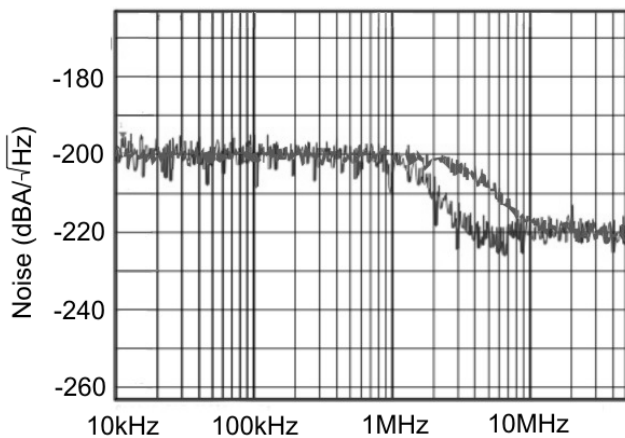**Fig. 9.** Phase frequency response.

Fig. 10. Noise spectral density.

4　Conclusion

A 3rd-order current-mode Butterworth filter was realized in a digital 120 nm CMOS technology. This filter is applied for the transmit path of a software radio system. The filter performance is summarized in Table 2.

For comparison, in Otin et al. (2006) a 3rd-order current-mode filter based on the G_m-C architecture in a 0.35 μm standard CMOS technology with a digital programmable cut-off frequency between 42 MHz and 215 MHz is presented which has a dynamic range of 53dB and consumes 3.7–18.6 mW per pole.

In Smith and Sanchez-Sinencio (1996) a current-mode filter based on current mirrors in 2 μm CMOS is described which has a cut-off frequency of 10 MHz, a DR of 52 dB and consumes 0.7 mW per pole. But it should be noted that an analog design in the deep-submicron technology causes an increase of power compared to micrometer or submicrometer CMOS, if the performance can be kept constant at all.

Table 1. Harmonic Distortions of the Output Current for an amplitude of 250 μA.

f_C	HD [dB] f_C=1 MHz f_{input}=200 kHz	HD [dB] f_C=4 MHz f_{input}=800 kHz
2·f_C	−55.7	−53.5
3·f_C	−48.0	−45.5
4·f_C	−71.5	−67.0
5·f_C	−56.5	−54.3

Table 2. Properties of the 3rd-order filter.

Technology	120 nm digital CMOS	
Voltage Supply	1.5 V	
Current consumption	4.5 mA	
Power consumption per pole	2.25 mW	
Input current for 1%THD	250 μA	
IIP3	1.45 mA	
Spectral noise density	100 pA/$\sqrt{Hz}$	
Area of the filter	350 μm×240 μm	
Area of the filter (including pads)	850 μm×400 μm	
Cut-off frequency	1.28 MHz	4.18 MHz
Integrated output noise	100 nA$_{rms}$	200 nA$_{rms}$
Dynamic range	65 dB	59 dB

References

Annema, A., Nauta, B., van Langevelde, R., and Tuinhout, H.: Analog Circuits in Ultra-Deep-Submicron CMOS, IEEE Journal of Solid-State Circuits, 40(1), 132–142, 2005.

Manhattanakul, J. and Toumazou, C.: Current-Mode Versus Voltage-Mode Gm-C Biquad Filters: What the Theory Says, IEEE Trans. Circuits and Systems II, 45(2), 173–186, 1998.

Otin, A., Celma, S., and Aldea, C.: A Design Strategy for VHF Filters with Digital Programmability, IEEE Symposium on Circuits and Systems, 1059–1062, 2006.

Ramirez-Angulo, J., Robinson, M., and Sanchez-Sinencio, E.: Current-Mode Continuous-Time Filters: Two Design Approaches, IEEE Transactions on Circuits and Systems-II, 39(6), 337–341, 1992.

Smith, S. L. and Sanchez-Sinencio, E.: Low Voltage Integrators for High-Frequency CMOS Filters Using Current Mode Techniques, IEEE Trans. Circuits and Systems II, 43(1), 39–48, 1996.

Zele, R. H. and Allstot, D. J.: Low-power CMOS continuous-time filters, IEEE Journal of Solid-State Circuits, 31(2), 157–168, 1996.