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A low-noise current preamplifier in 120 nm CMOS technology

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Abstract. In this paper we examine the impact of deep submicron CMOS technology on analog circuit design with a special focus on the noise performance and the ability to design low-noise preamplifiers. To point out, why CMOS technology can grow to a key technology in low-noise and high-speed applications, various amplifier stages, applied in literature, are compared. One, that fits as a current preamplifier for low-noise applications, is the current mirror. Starting from the basic current mirror, an enhanced current preamplifier is developed, that offers low-noise and high-speed operation. The suggested chip is realized in 0.12 μm CMOS technology and needs a chip area of 100 μm$\times$280μm. It consumes about 15 mW at a supply voltage of 1.5 V. The presented current preamplifier has a bandwidth of 750 MHz and a gain of 36 dB. The fields of application for current preamplifiers are, for instance, charge amplifiers, amplifiers for low-voltage differential signaling (LVDS) based point-to-point data links or preamplifiers for photodetectors.

1 Introduction

The heading towards high-speed circuits and low power dissipation combined with a cost-effective design in digital CMOS technology leads to lower structure sizes. As a result of mixed-signal design in System-on-Chips (SoCs), where analog and digital circuits are assembled on one chip, analog designers have to concern about this technology. New CMOS technologies open up some advantages but entail severe drawbacks as well. Short gate lengths, which simultaneously means small parasitic capacitances, boost the transit frequency of the CMOS transistors to a high level. Furthermore, circuit designs with low power dissipation and cheap fabrication costs are possible. The disadvantages have to be considered as well. A severe problem is the low supply voltage, that is defined by the break-through voltage of the transistors. The low supply voltage affects the signal headroom too, which is decreasing drastically. Further issues are the increase of 1/f-noise with smaller gate lengths and the dramatic decrease of the Early voltage (Chang, 1991). Another challenge is, that gate leakage and its mismatch are a serious problem in new technologies like 65 nm CMOS (Annema et al., 2005). The improvement of matching by increasing the gate area, results in an enhancement of the parasitic capacitances and thus in a limitation of the speed. The above mentioned characteristics of deep sub-micron CMOS technologies force a careful circuit design for a proper system performance.

Sometimes current-mode circuits can have some advantages compared to voltage-mode circuits in new CMOS technologies. Current-mode circuits provide the opportunity for low supply voltage, have a tunable input impedance and are less susceptible to power and ground fluctuations. Furthermore current-mode signal processing is a very attractive approach due to the simplicity in implementing operations, such as addition, subtraction and multiplication by a constant (Yuan, 2006).

Current amplification, as an essential part in analog circuit design is necessary for various devices and sensor interfaces, measurement equipment or signal-processing circuits. A reliable detection of currents in the range of nano-ampere to micro-ampere is a complex problem depending on the requirements of the target system. Small currents appear in various tasks, which may have many different specifications. Those specifications concern bandwidth, power consumption, supply voltage, linearity, noise, et cetera. Feasible applications for current amplifiers are preamplifiers for measurement systems, charge amplifiers, current-mode filters or optical sensors and amplifiers for low-voltage differential signaling (LVDS) based point-to-point data links or high-speed bus systems.

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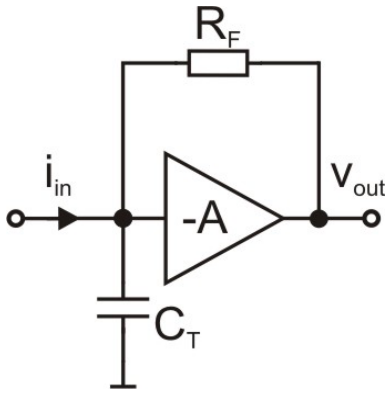

Fig. 1. General schematic of a transimpedance amplifier.

The possibilities that allow the transformation of low input-signal currents are presented in Sect. 2, the proposed circuit is described in Sect. 3 and measurement results are given in Sect. 4.

2 Current amplifiers

In literature, two common approaches of current amplification are mentioned. Both, the transimpedance amplifier and the current mirror, are compared to each other.

2.1 The common approach: transimpedance amplifier

A common approach to convert the current-mode input signal to a proportional voltage signal is the use of a transimpedance amplifier (TIA). A conventional TIA, as shown in Fig. 1, has the simplified transfer function

$$\frac{v_{\text{out}}}{i_{\text{in}}} = G(s) = -\left(\frac{A}{1+A}\right)\frac{R_F}{1+sC_T\left(\frac{R_F}{A+1}\right)}, \tag{1}$$

where A denotes the open-loop voltage gain, R_F and C_T give the feedback resistance and the total input capacitance, respectively. It easily can be seen, that the cut-off frequency can be increased by lowering the feedback resistance R_F. Unfortunately, R_F has an undesirable direct impact on the overall gain, that is also lowered.

An estimation of the equivalent input noise current is presented in Park and Papavassiliou (1999). The examination of the noise sources in the general transimpedance amplifier shows the influence of the circuit parameters on the noise performance (Eq. 2). The equivalent input noise current is given by

$$\left\langle \overline{i_{eq}^2} \right\rangle = \frac{(2\pi)^2 C_T^2 \overline{v_n^2} B_{eq}^3}{3} + \frac{(\overline{v_n^2} + \overline{v_f^2}) B_{eq}}{R_F^2}\,, \tag{2}$$

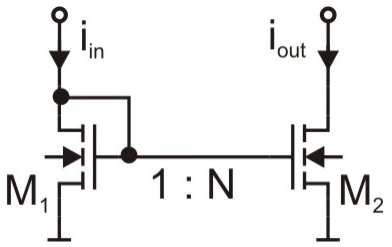

Fig. 2. Basic current mirror.

where B_{eq} is the noise bandwidth and $\overline{v_n^2}$ and $\overline{v_f^2}$ are denoted by (Γ=2/3 in the saturation region)

$$\overline{v_n^2} = \frac{4kT\Gamma}{g_m} \qquad \text{and} \qquad \overline{v_f^2} = 4kTR_F\,. \tag{3}$$

The first term of Eq. (2) is dominant for high frequencies, hence, C_T has to be as low as possible. The second term of Eq. (2) shows that a reduction of the feedback resistor R_F leads to higher noise. The above considerations show, that the value of R_F has to fit for the trade-off between bandwidth, gain and noise. The use of a current preamplifier offers a way out of these limitations (Yuan, 2006).

2.2 Current mirror

Besides various current-mode amplifier structures, the current mirror is a basic cell, that is commonly used for current amplification. A simple current mirror, as shown in Fig. 2, consists of two transistors. The ratio of their currents is given by

$$\frac{i_{\text{out}}}{i_{\text{in}}} = N = \frac{\frac{W_2}{L_2}}{\frac{W_1}{L_1}}\,, \tag{4}$$

assuming, that v_{GS} is equal for both transistors. To obtain good matching, the channel length L is usually kept equal for both transistors. Other important properties with a positive impact on current preamplifiers when using current mirrors are the low input resistance and the high output resistance (Laker and Sansen, 1994).

Current amplifiers are already topic in recent publications. The potential advantage of a current preamplifier circuit combined with a transimpedance amplifier compared to a classical transimpedance amplifier is shown in Sturm et al. (2005). An optoelectronic receiver IC for optical storage applications is presented. They suggest a two-stage design, consisting of a current preamplifier and a following TIA, which is called ITIA. The current preamplifier is a current mirror, that is made of two bipolar NPN transistors. A noise performance calculation, that compares a classical transimpedance amplifier with the proposed ITIA shows that the input referred current noise can be lower for the ITIA structure. For high-frequency operation the classical

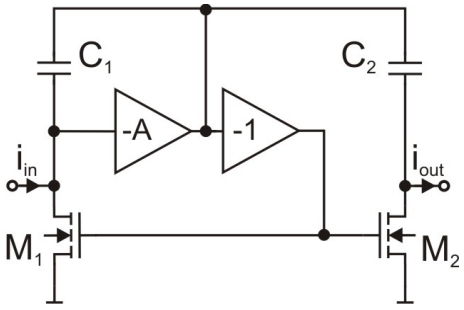

Fig. 3. A low-noise current preamplifier in CMOS technology.

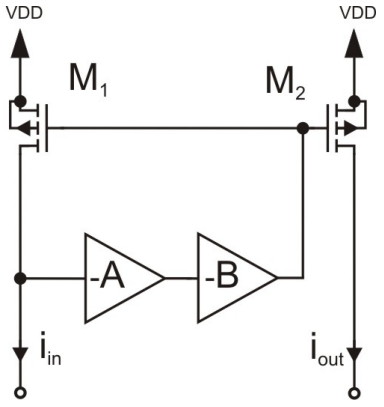

Fig. 4. Block diagram of the low-noise current preamplifier.

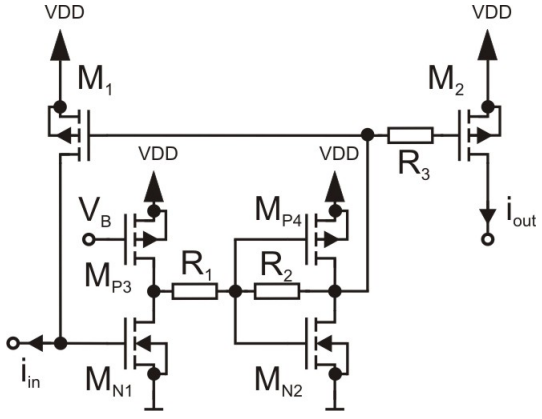

Fig. 5. Schematic of the current preamplifier.

TIA structure suffers from some poor properties concerning noise, as already mentioned. A high bandwidth needs a low feedback resistor, which increases the noise contribution and lowers the transimpedance gain. Especially for low input currents, that need a high gain for further signal processing and a high signal-to-noise ratio the ITIA shows a much better noise performance than the classical TIA. This comparison demonstrates, that current preamplifiers lead to a better noise performance than the classic TIA input stage, if low input-signal currents and high frequencies are demanded.

A low-noise amplifier (LNA) topology for Optoelectronic Integrated Circuits (OEICs) is shown in Fig. 3 using 0.18 μm CMOS technology by Giardina et al. (2006). The proposed LNA contains a current mirror, an amplifier stage and an inverting stage. The capacitors C_1 and C_2 are used to enhance the bandwidth of the amplifier. The inverting stage adds a phase shift of π to drive the gates of M_1 and M_2 in the correct phase. Beside the presentation of the OEIC preamplifier the benefits of decreasing gate lengths for OEICs were emphasized. They concluded, that decreasing gate lengths improve the noise performance of CMOS circuits at a given input capacitance, this means that the lowest noise level is limited by the minimal gate length.

3 Circuit design

In this paper, we propose a current preamplifier designed in 0.12 μm CMOS technology. The presented current-mode preamplifier is based on a current mirror as well. As shown in Fig. 4, the current mirror consists of transistors M_1 and M_2, whose width ratio leads to a current amplification. The injected input current i_{in} is mirrored to i_{out} as a result of the common gate-source voltage. For the enhancement of the speed of the current mirror preamplifier, additional voltage-mode amplifiers are used to regulate the gates of the current mirror transistors. For this operation the change of the potential at the input node, caused by the fluctuating input currents, is used. An increasing current in transistor M_1 causes a slight voltage reduction on the input node and vice versa. This current dependent voltage alteration is amplified and used in the feed-forward loop, consisting of stages A and B, to drive the gates. This technique rises the bandwidth and allows high-speed operation.

To keep an eye on the noise performance of the current preamplifier, another important item, that concerns the design of voltage amplifiers A and B, has to be observed. To obtain the highest signal-to-noise ratio, the first amplifier (amplifier A) should have maximum gain. The second amplifier (B), as depicted in Fig. 4, is used to change the phase of the voltage signal and to adjust the gain of the feed-forward circuit.

In Giardina et al. (2006) the circuit details for the blocks in Fig. 3 were not described. Here, we introduce a solution. In addition we exploit PMOS transistors (M_1, M_2) in the current amplifier (Figs. 4 and 5). The PMOS transistors allow the reverse current direction, that is needed in several sensor applications. Moreover a PMOS transistor, in the technology used, adds less noise to the preamplifier as well and affects the overall noise performance in a positive manner.

In Fig. 5 the detailed final circuit of the current preamplifier, except biasing, is shown. Above considerations are

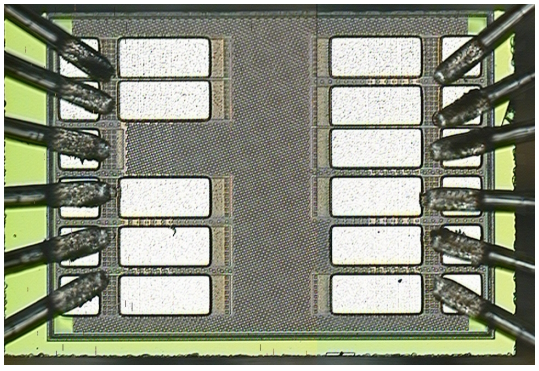

Fig. 6. Chip photo of the current preamplifier.

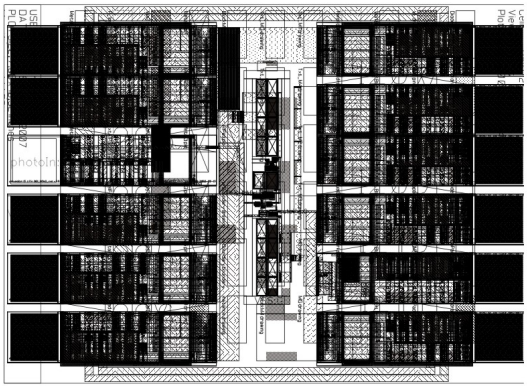

Fig. 7. Layout of the current preamplifier.

directly observed in the circuit design. To achieve high gain and to maximize the signal-to-noise ratio in the feed-forward path, a common-source amplifier is used for the first stage. The following amplifier has the structure of an inverter stage in feedback configuration with R_2. The ratio $\frac{R_2}{R_1}$ adjusts the overall gain of both voltage amplifiers, that has an impact on bandwidth and operation point of the current-mode preamplifier.

The cut-off frequency of the entire preamplifier is set by resistor R_3, as shown in Fig. 5. The resistor and the parasitic gate-source capacitance of the transistor M_2 build a first-order low-pass, whose bandwidth defines the cut-off frequency of the preamplifier. The circuit performance and measurement results are presented in the following section.

4 Measurement results

The above described current-mode preamplifier was simulated and fabricated in 0.12 μm CMOS technology. Since the chip photograph in Fig. 6 does not show any details due to the planarization and passivation layers, the layout of the chip is shown in Fig. 7. The measured power consumption

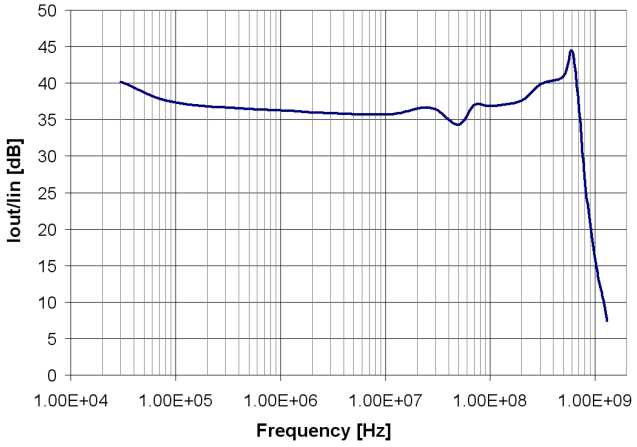

Fig. 8. Measured frequency response.

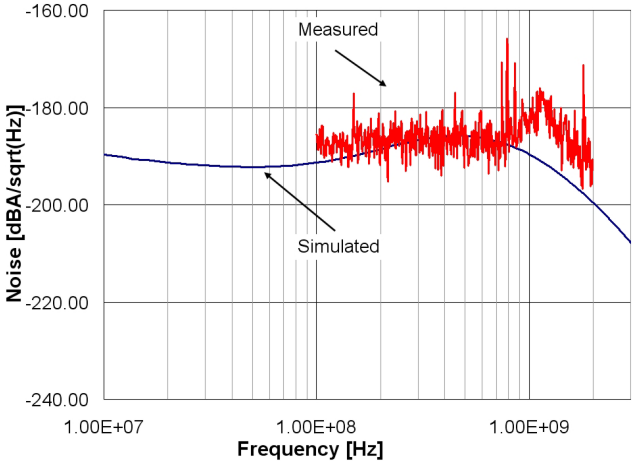

Fig. 9. Measured versus simulated spectral current noise density.

of the chip was 15 mW at a supply voltage of 1.5 V. The active area is 100 μm$\times$280 μm. The achieved gain is approximately 36 dB and the bandwidth is about 750 MHz. Figure 8 shows the measured frequency characteristic.

Figure 9 shows the simulated spectral noise density versus the measured spectral current noise density at the output. The measured output spectral current noise density matches to the simulated values very well, and results in 380 pA/$\sqrt{\text{Hz}}$. The output noise integrated over the bandwidth of 750 MHz is equal to 10 μA. The equivalent input referred current noise is 165 nA.

Table 1 shows a comparison of the presented current preamplifier to recent publications. Although the gain is not the highest, which is difficult to compare because of multistage amplifier design of Sturm et al. (2005) and de Jong et al. (2002), we achieved the highest bandwidth. We fabricated in the newest technology, which has only 1.5 V supply

Table 1. Comparison to other publications.

Publication	Sturm et al. (2005)[1]	Giardina et al. (2006)	de Jong et al. (2002)[2]	This Work
Gain	108 dB	48 dB	max. 66 dB	36 dB
Cut-Off Frequency	260 MHz	600 MHz	250 MHz	750 MHz
Technology	0.5 μm BiCMOS	0.18 μm CMOS	0.6 μm CBiMOS3	0.12 μm CMOS
Supply Voltage	5 V	1.5 V	5 V	1.5 V
Power Consumption	300 mW	12.5 mW	170 mW	15 mW
Active Area	n.s.[3]	360×260 μm^2	n.s.[3]	100×280 μm^2

[1] two stages
[2] four stages
[3] not specified

Table 2. Performance summary of the proposed current-mode preamplifier.

Gain	36 dB
Cut-Off frequency	750 MHz
Technology	0.12 μm CMOS
Supply voltage	1.5 V
Power consumption	15 mW
Active area	100×280 μm^2
Integrated In-Band Output Current Noise	10 μA
Equivalent Integrated In-Band Input Noise Current	165 nA

voltage. Furthermore we designed the chip with the smallest active area. Unfortunately Sturm et al. (2005) and de Jong et al. (2002) did not mention their active area, but it can be estimated that a multistage amplifier design occupies a larger area. In Table 2 the performance of the proposed current preamplifier is summarized.

5 Conclusions

In this work we present a low-noise current preamplifier based on a current mirror in 0.12 μm CMOS technology. It can be used for current-mode circuits, measurement systems, charge amplifiers, optical sensors, et cetera. Furthermore the classical transimpedance amplifier is compared to this new approach. Motivations to realize a low-noise current-mode amplifier in deep sub-micron CMOS processes are highlighted. The obtained observations were used to realize a low-noise preamplifier employing a feed-forward path to broaden the bandwidth. The insertion of PMOS transistors as current mirror has a positive impact on the noise performance. The designed preamplifier stage has a gain of 36 dB and a bandwidth of 750 MHz. The amplifier with the size of 100 μm×280 μm consumes about 15 mW at 1.5 V power supply.

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