

# Physical IC debug – backside approach and nanoscale challenge

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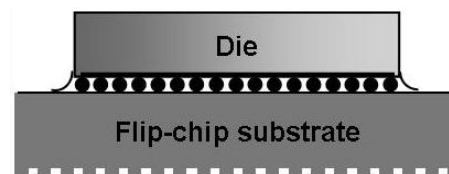
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**Abstract.** Physical analysis for IC functionality in sub-micron technologies requires access through chip backside. Based upon typical global backside preparation with 50–100  $\mu\text{m}$  moderate silicon thickness remaining, a state of the art of the analysis techniques available for this purpose is presented and evaluated for functional analysis and layout pattern resolution potential. A circuit edit technique valid for nano technology ICs, is also presented that is based upon the formation of local trenches using the bottom of Shallow Trench Isolation (STI) as endpoint for Focused Ion Beam (FIB) milling. As a derivative from this process, a locally ultra thin silicon device can be processed, creating a back surface as work bench for breakthrough applications of nanoscale analysis techniques to a fully functional circuit through chip backside. Several applications demonstrate the power and potential of this new approach.

## 1 Introduction

It has become common practice with recent IC technologies that the physical techniques to support functional circuit analysis have to access the active information through chip backside (see Fig. 1) (Barton et al., 2004). For this purpose, the device receives typically a global polishing preparation. In most cases, mechanical stability and / or heat sink requirements limit the minimum remaining silicon substrate thickness to 550–100  $\mu\text{m}$ , which will be categorized here as moderate silicon thickness.

The penetration depth of particle beams is orders of magnitude smaller, so the previously very successful electron or ion beam microscopy derivatives using voltage contrast like E Beam Probing are not applicable under these circumstances. But bulk silicon is transparent to light of photon energies smaller than the Si band gap of 1.1 eV, i.e. the near infrared (IR) regime. A survey of the analysis techniques



**Fig. 1.** Flip chip package. Structured side of IC (die) is turned to substrate (image from [1]).

available for backside access of moderate silicon thickness is presented in chapter 2.

Circuit edit also needs to be performed through chip backside. The creation and optimization of FIB-based processes for this purpose is subject of the following chapter 3. The key of backside circuit edit is the milling of local trenches to the bottom level of the STI, leaving an SOI (Silicon on Insulator) – like ultra thin layer of silicon (ca. 300 nm) for active device function. This preparation technique, expanded to planes of up to 0.03 mm<sup>2</sup>, offers a new breakthrough approach of physical functional analysis techniques: While the circuit will be remaining fully functional, the active volume then is small enough to interact with high energy photons or particle beams applied through chip backside. The 4th chapter will discuss the opportunities of such a concept for nanoscale resolution of functional analysis techniques and demonstrate how powerful it is in use.

## 2 Backside access functional analysis on devices of moderate bulk silicon thickness

Global polishing of bulk silicon is a high yield process as long as a moderate thickness of 50–100  $\mu\text{m}$  remains. The preferred interactive medium of functional analysis techniques in this case is near IR optics with photon energies smaller than silicon energy band gap of 1.1 eV, corresponding to wavelengths of 1.1  $\mu\text{m}$  and higher. Three main dynamic approaches have been established: Time resolved photon emission (TRE), laser voltage probing (LVP) and laser



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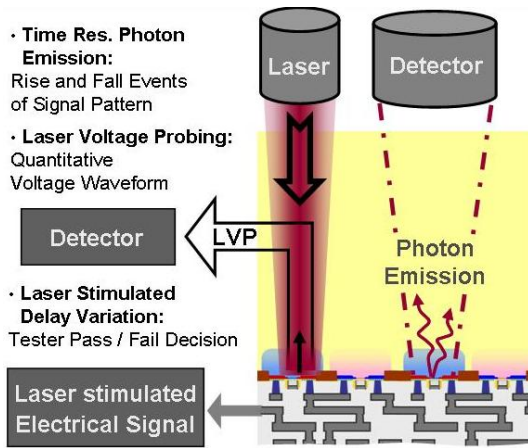


Fig. 2. Optical probing and stimulation techniques.

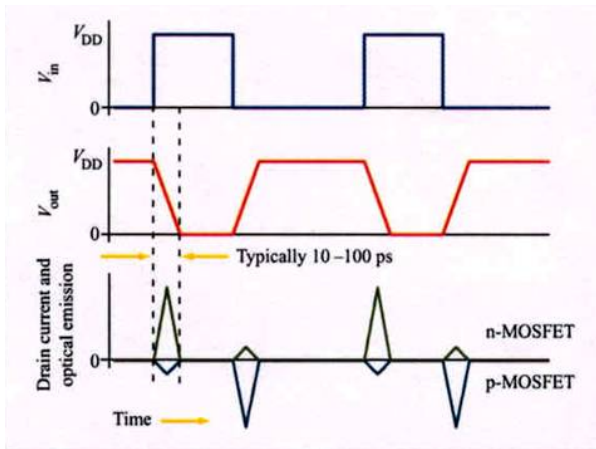


Fig. 3. TRE and signal pattern (from [24]).

stimulation (LS) techniques (Fig. 2). Time resolution and signal pattern response characteristics of these techniques will be discussed shortly in this chapter, before the critical resolution potential of the general approach using moderate silicon thickness will be assessed.

### 2.1 Time resolved photon emission (TRE)

Photon Emission is the standard functional analysis technique of semiconductor devices as it occurs in a MOS Transistor without any further stimulus when a considerable number of carriers gain kinetic energy high enough to relax by emitting photons (Boit, 2004). This is happening in CMOS digital circuits mainly during rise and fall time of the signal pattern (Fig. 3). Although this dynamic light signal is faint, TRE is a very powerful, reliable and easy to interpret technique with low risk of artifacts and time resolution in 10 ps regime (Vallett, 2004). Due to the low signal level, sampling of the signal is necessary. As the waveform is not reproduced in full but the signal only represents the short switch-

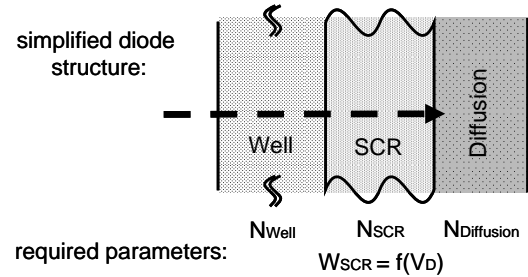


Fig. 4. Simplified diode structure for simulation (from [8])

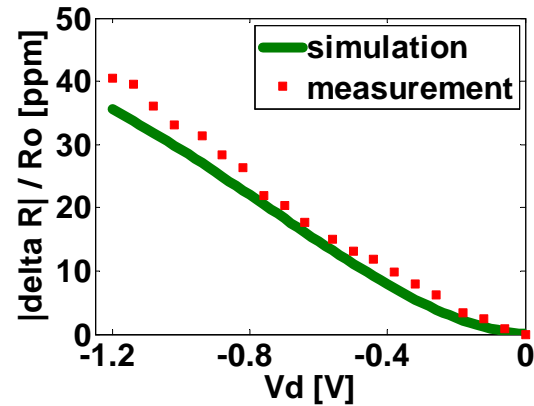


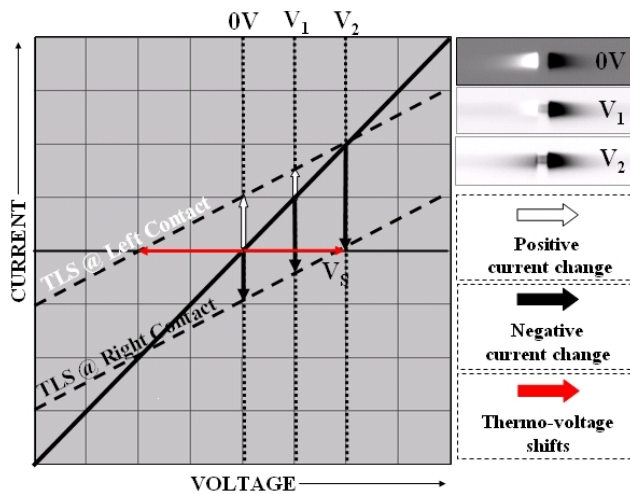
Fig. 5. Comparison of simulation results from model in Fig. 4 with measurement on PFET drain area.

ing pulses, trigger stability and jitter are critical (Kasapi and Woods, 2006). TRE emission intensity decreases nonlinearly with supply voltage (Rowlette and Eiles, 2003). The resulting SNR challenge of recent IC technologies may not be overly severe as recent studies indicate (Tosi et al., 2006).

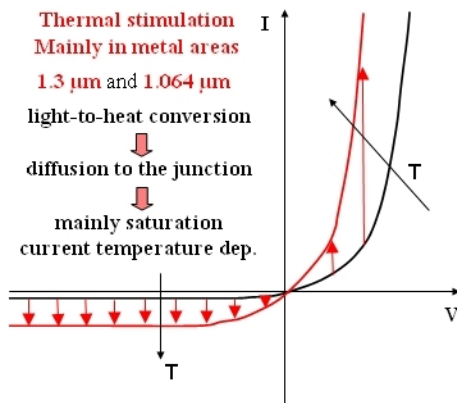
Spectral information of the emission has so far only marginally been used in analysis. Detailed understanding of device physics and the mechanisms of photon emission may change this in the future.

### 2.2 Laser Voltage Probing (LVP)

When an IR laser illuminates the active devices through chip backside, the reflected light is modulated by active device operation in the ppm (parts per million) range. This signal has been proven to be linearly correlated to the voltage applied to the device and the waveform of a signal pattern passing the node can be reproduced, very similar to E Beam Probing (EBP) (Panizza et al., 1998). Originally, the signal has been attributed to electrical fields in the device due to free carrier dynamics (Franz-Keldysh-Effect). Recent investigations using device simulation succeeded to correlate the signal to the dynamics of absorption and refractive index due to the presence or absence of free carriers by space charge modulation (Kindereit et al. 2007), which allow simpler modeling



**Fig. 6.** Illustration of SEI and OBIRCH influence on I/V characteristic (from[10]).



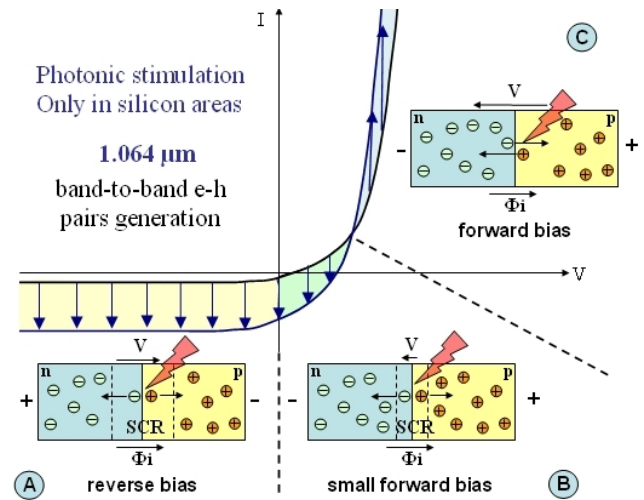
**Fig. 7.** p-n junction IV characteristic at TLS (from[10]).

of the effect (see Fig. 4 and 5). In this example, a qualitative and even a quantitative fit has been successful using well doping level of  $10^{17} \text{ cm}^{-3}$  and a diffusion doping level of  $10^{21} \text{ cm}^{-3}$ .

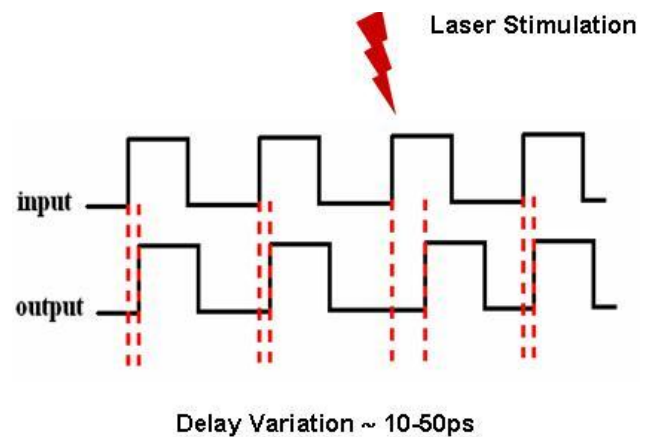
Time resolution is in the same range as TRE. Due to the waveform reproduction, the signal pattern information can still be obtained when trigger stability is problematic.

Probe placement may not be trivial when local interference is affecting the signal level.

Although available for a long time, in recent past LVP stood in the shadow of TRE. But the power of this technique has been improved by the mentioned in depth investigation of the interaction mechanisms, and a new product generation using polarized light, and seems to become increasingly attractive again, especially as it offers some robustness to IC clock instabilities.



**Fig. 8.** p-n junction IV characteristic at PLS (from[10]).



**Fig. 9.** Delay variation with laser stimulation.

### 2.3 Laser stimulation

Scanning IR lasers with several hundred mW can stimulate electrical signal alteration either by local heat conversion of the absorbed light modulating electrical parameters (TLS = Thermal LS, Beaudoin, 2004), or by photocurrent induced into the signal path if photon energies reach silicon band gap level and electron hole (e-h) pairs are generated (PLS=Photoelectric LS).

As the electrical circuit behavior can be altered in a wide variety, many techniques have been invented that are based on the LS principle. Table 1 gives an overview of the most common abbreviations used in LS of statically and dynamically driven circuits.

The transformation of the stimulating effect into an electrical signal that can be read out over IC terminals occurs on the four paths resistivity change, thermoelectric voltage generation, temperature coefficient of pn junction and photocarrier generation. In the Figs. 6–8, the corresponding influence

Table 1. Laser Stimulation techniques.

Stim.	Effect	Technique	Device Analysis
1300 nm	Thermal Laser Stim.	<b>OBIRCH</b> Optical Beam Induced Resistivity Change	Identify areas of high local resistance
		<b>TIVA</b> Thermally Induced Voltage Alteration	
		<b>TLS</b> Thermal Laser Stim.	
		<b>RIL</b> Resistive Interconnect Localization	Test vectors: Identify area of highest pass-fail sensitivity (Shmoo Variation)
		<b>SDL</b> Soft Defect Localization	
		<b>SEI</b> Seebeck (Thermoelectric) Effect Imaging	
			Identify sensitive material interfaces
1064 nm	Photo -electric Laser Stim., parasitic TLS	<b>PLS</b> Photo -electric Laser Stim., parasitic TLS	
		<b>OBIC</b> Optical Beam Induced Current	Localize p-n junctions – Space Charge Region (SCR)
		<b>LIVA</b> Light Induced Voltage Alteration	Read out signals sensitive to logical state
		<b>LADA</b> Laser Assisted Device Alteration,	
		<b>Dynamic LS</b>	Signal Pattern in IC: Delay Variation As parasitic effect
		<b>OBIRCH, SEI</b>	

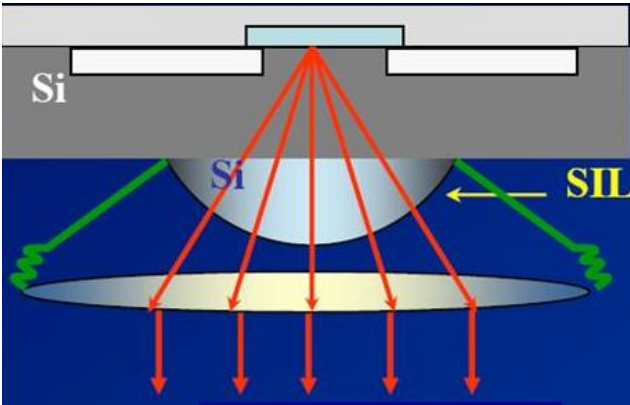


Fig. 10. Principle of Solid Immersion Lens (from [23]).

of the stimulation on equivalent device i-v characteristics is presented. All static and dynamic properties of devices and circuits can be derived from these models. In case of TLS in an FET, typically the channel conductivity will be modulated like OBIRCH, but in two competitive mechanisms, change of

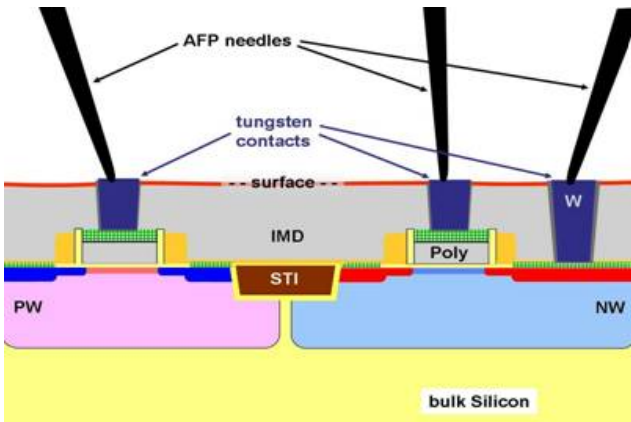


Fig. 11. Principle of Nanoscale Atomic Force Probing (AFP) on parallel polished sample.

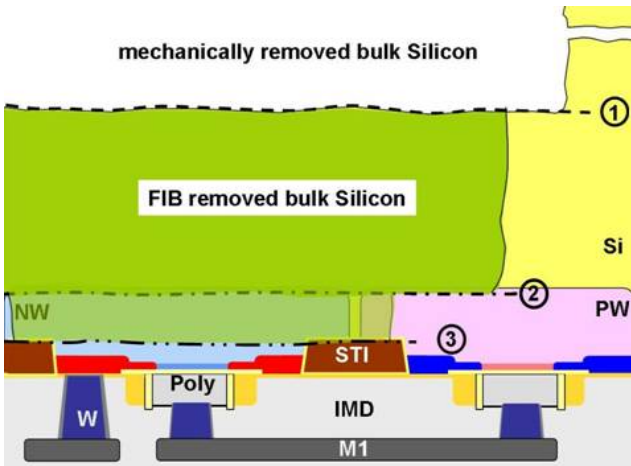


Fig. 12. FIB preparation for backside circuit edit.

mobility and threshold voltage. But to understand the readout properly, several side effects like local conversion efficiencies, heat or carrier diffusions and distant Seebeck voltages may contribute to the final signal. A detailed description of all those effects is given in (Glowacki, 2007).

In a dynamically driven IC, LS will influence the timing. The results of dynamic LS can be read out either by pass/fail condition of the tester under stimulation (Shmoo variation) or direct evaluation of the signal pattern variation (Fig. 9). A systematic overview on the LS at dynamic circuit operation like in (Bruce et al., 2002) for static techniques is nor yet available, so in Table 1 some of the techniques seem to be overlapping and some possible options have not been published yet.

A very effective analysis uses an already established test signal path of a soft failing device that is driven below a critical temperature, and the laser is raising the illuminated area above the critical level. Such a Shmoo variation using TLS is RIL if the soft defect is located in interconnect levels or SDL



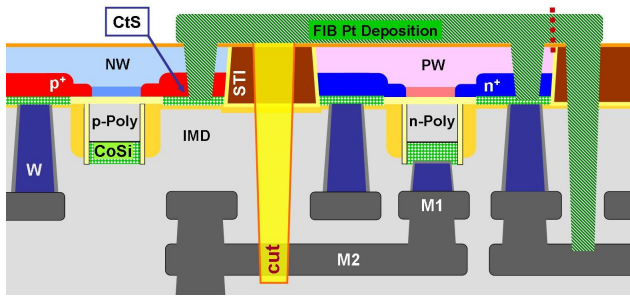


Fig. 13. Variety of FIB contacts using UTS.

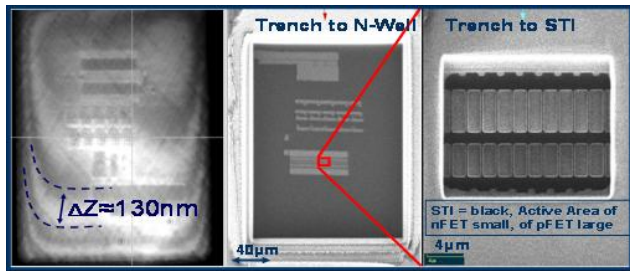


Fig. 14. Image of FIB trench location (left: IR-optics, middle: FIB n-well end point, right: FIB STI opening).

(Bruce et al., 2002), when active devices are affected. PLS causes similar effects.

The other group of techniques read out the signal pattern directly like LADA or Delay Variation (Sanchez et al., 2006a,b). In a transistor, the effects of PLS and TLS on the output current must be studied in detail for correct evaluation (Glowaki et al., 2007). In general, if PLS is enabled by selection of the proper laser wavelength, it usually prevails over TLS.

Time resolution and required trigger quality of LS is very much a question of the signal extraction procedure.

As in LS a large variety of stimulation and readout opportunities can be applied, the overall potential of this approach is by far not exhausted yet.

#### 2.4 Nanoscale potential of IR analysis techniques

Maximum microscopic resolution is the light wavelength referring to the length of a repeating structure, the so called pitch. A pitch consists of minimum 2 features, so the minimum resolved feature is  $2 \times$  smaller. Realistic pitch resolution is ca. 800 nm, respectively 400 nm feature size. But feature sizes are rapidly shrinking with technology innovation. Solid Immersion Lenses (SIL, Fig. 10) have been introduced, making bulk silicon a part of the microscope and increasing resolution theoretically by the refraction index of silicon  $n_{Si}=3.5$ . A resolution of 200 nm has been achieved.

As technologies progress further into the nanometer range, IR techniques even with SIL can localize only the area of in-

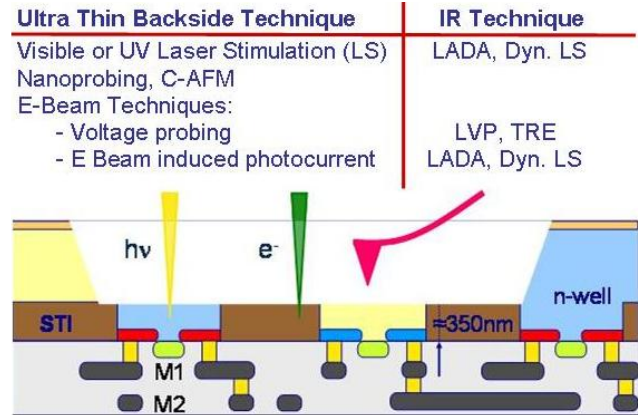


Fig. 15. Probing on Ultra Thin Silicon.

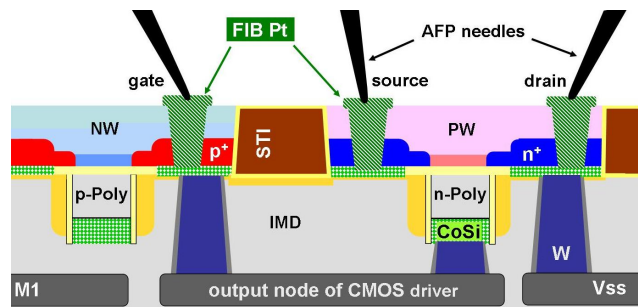


Fig. 16. Nanoprobe on FIB edited contacts to Silicide.

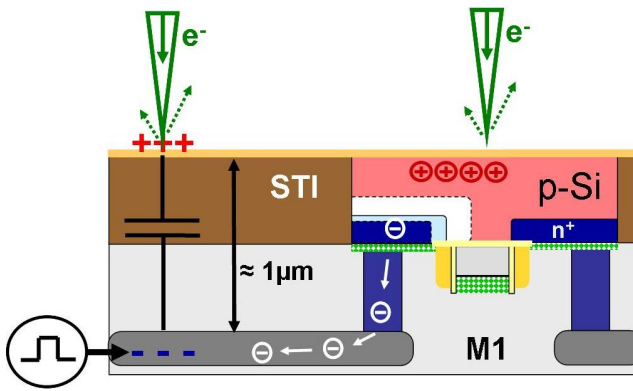
terest but not anymore the exact device. In addition, scanning probe techniques and derivatives are increasingly inevitable to identify the critical node in nanoscale regime. Nanoprobe makes use of the contacts to the active structures under investigation (Fig. 11) (Lin et al., 2006; Mulder et al., 2006). Planar polishing techniques need to be applied from chip frontside, finally removing all interconnect

layers to reveal the tungsten contacts of multiple devices in the suspected fail area.

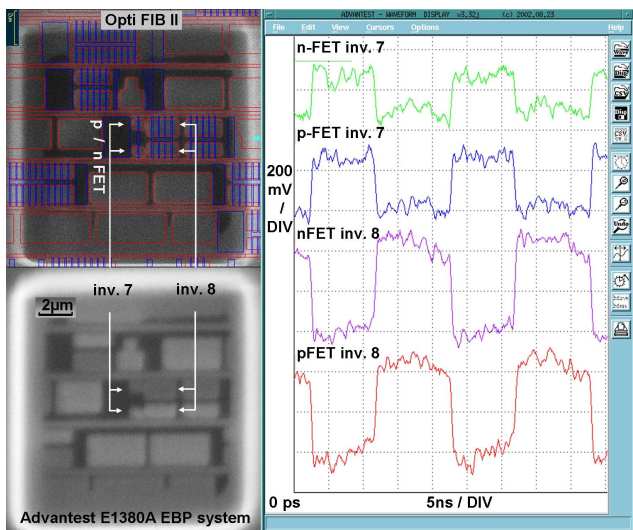
This process is time consuming and full of risks: If the failing transistor cannot be found in the final measurement the problem might have been removed with the backend, leaving no second chance for other FA techniques.

### 3 Circuit edit through chip backside

The challenge for focused ion beam (FIB) based circuit edit (CE) today is access through chip backside, requiring circuit cut and paste operations much closer to the active layers than global preparation techniques can provide. A trenching process using a FIB with coaxial IR optical microscope has been established that removes bulk silicon down to the bottom level of shallow trench isolation (STI). This process is performed in three steps as indicated in Fig. 12: After a global



**Fig. 17.** Backside E-Beam Probing targeting M1 or directly measuring on the FET floating body.



**Fig. 18.** EBP results measured directly of FET body of 90 nm bulk CMOS after FIB backside prep down to STI level.

polishing technique as applied in chapter 2, the region of interest is identified by the IR microscope. Then, after a special FIB cleaning procedure, a  $200 \times 200 \mu\text{m}^2$  wide trench is milled until the operator stops on n-well level. The endpoint becomes visible because of a voltage contrast between the n-wells and the substrate due to the built-in potential of the pn-junction (Boit et al., 2003). Next, a smaller local trench will be milled until the STI becomes visible as imaging contrast - lower secondary electron emission of  $\text{SiO}_2$  - and the preparation is ended.

By this approach, the active device material is reduced to 300 to 400 nm (the depth of the STI trenches) and the chip is ready for the actual edit process, the milling of narrow trenches for the cuts and contact holes (Boit et al., 2005).

This backside FIB process is offering several more opportunities to edit the circuit than the frontside process: The technique to endpoint the contact trenches on the Silicide

interface, which is only 300 nm below the trench to STI, is meanwhile established (Schlangen et al., 2006a), allowing to contact any source/drain area on the chip, even those that have not been contacted on IC interconnect level. All the functional nodes are represented on the active device level. A typical backside CE is illustrated in Fig. 13. Any CE contact can be performed using the contact to silicide (CtS) process, only cut operations still have to be performed by trenching deeper into metal interconnects. The lower aspect ratio for CtS compared to contacts to metal lines (right part of Fig. 13) is very fortunate for the contact resistance, being the critical parameter for nanoscale application. With current platinum deposition, contacts on silicide have resistivities below  $60 \Omega/\mu\text{m}^2$ . Typical contact sizes of  $1 \times 0.2 \mu\text{m}^2$  end up with  $300 \Omega$  resistance per contact, considerably lower than FET- channel resistances of several k $\Omega$  (Schlangen et al., 2007a) and acceptable for most CE and probing tasks. When SOI technologies are considered, the contact height will be reduced by a factor of 3, reducing resistance further. The utilization of advanced conductor deposition materials as Molybdenum may offer further improvement potential.

Taking into account state of the art FIB resolution performance, this backside CE technique can be rated as fully suitable for technologies scaling well into the nanometer regime.

An invasiveness study of backside CE processing using intentionally enlarged trench sizes down to STI level (Fig. 14), resulted in almost unchanged single device- and circuitry-performance at regular processing (Boit et al., 2005).

This study showed also that a wide FIB trench to n-well level can be performed with remarkable co-planarity to the chip levels. In Fig. 14, the coaxial IR microscope image of the trench shows Newton rings indicating the slope of silicon thickness. A planarity mismatch less than 200 nm on  $250 \mu\text{m}$  trench expansion or 0.08% deviation is state of the art. With such a process, a new base plane can be created for the application of analysis techniques through the backside of ultra thin silicon.

#### 4 Functional IC analysis through the backside of Ultra Thin Silicon (UTS)

The FIB preparation routines developed for circuit edit through chip backside (chapter 3) produce a back surface of an ultra thin active device volume maintaining full IC functionality. The back surface of the remaining ultra thin active volume can now be regarded as a completely new work bench for physical techniques to access fully functional circuits. This innovative concept opens a very short path to device interaction for analysis techniques with improved resolution potential (Fig. 15), which is summarized in Table 2.

Nanoprobing can now be performed on a fully functional circuit, avoiding the risks of parallel polishing from IC frontside that are pointed out in chapter 2. Particle beam techniques like E Beam Probing with the resolution potential

of an electron microscope, can be reconsidered for IC analysis on a higher technical level again. Optical techniques may be shifted to much smaller wavelengths with the respective resolution improvement as no bulk silicon has to be passed anymore.

In case of substantial power consumption in the IC's area of interest, solutions for proper heat dissipation paths need to be developed.

#### 4.1 Nanoprobing on UTS

Nanoprobing on UTS can be done on edited contacts because of their low resistance, taking advantage of the full circuit function (Fig. 16). For characterization of single devices, some cuts might be necessary to separate the transistors from their environment (Schlangen et al., 2007a), but full circuit functionality can be reestablished easily afterwards by simple conductor deposition.

#### 4.2 E-Beam Probing on UTS

The interaction opportunities through UTS are expanded to particle beams as well. Then, high resolution probing or stimulation with electron beams return to the IC debug toolkit. In (Schlangen et al., 2006b) it is demonstrated, that switching information on lower metal lines is transferred to the back surface (capacitive coupled voltage contrast, CCVC). Additionally, the full active device area can be used to pick up node waveforms (Fig. 17), based on the modulation of the floating body potential. In this way, the spot size of the pulsed e-beam can be as big as the full transistor body (always by a factor of 3–5 bigger than the smallest metal lines) and the resolution requirements become more relaxed. Furthermore, this method offers all advantages frontside EBP did: fast signal acquisition, linear Vdd signal scaling and superior signal to noise ratio (Jain et al., 2007).

Figure 18 shows first results measured with a 10 year old EBP, clearly resolving 90 nm technology (Schlangen et al., 2007b). Regarding latest improvements in low keV SEM development, this technique should be suitable for scaling further into nanometer regime.

#### 4.3 Optical Techniques on UTS

On UTS, visible and even UV light may be used to stimulate the devices. This way, optical resolution would be instantly improved even without SIL. In addition, short wavelength SIL solutions are within reach. Efficient PLS in small active volumes like SOI devices requires light of short absorption ranges. Only UTS provides the condition for such a stimulation.

Another problem is the stimulation character in multi-material active volumes as it is used more and more in strain technologies. Stimulation as performed today with photon energies near the Si band gap, has hardly predictable absorption properties for Ge compounds used for straining and mo-

**Table 2.** Comparison of Feature resolution potential of Functional Analysis Techniques though moderate and ultra thin silicon.

Technique	Resolution	Potential	Status
(IR) Optical bulk Si	400 nm	200 nm (SIL)	standard technique
(IR) Optical UTS	200 nm	100 nm (SIL)	future concept
UV UTS	100 nm	<50 nm (SIL)	future concept
E Beam UTS	100 nm	10–20 nm	demonstrated
Nanoprobing UTS	50 nm	10 nm	demonstrated

bility enhancement. With shorter wavelengths, absorption properties are clearly defined independent of the semiconductor material. If laser stimulation can be blanked over actives and only performed over STI, it may be possible to suppress photocurrent generation and thermal stimulation could then be accomplished with high resolution.

To gain resolution beyond all optical limits though, backside E-Beam Probing and E-Beam stimulation seem to be most promising.

## 5 Summary

The IR analysis techniques for IC debug are very powerful and offer a huge potential to localize circuit problems which is not fully exhausted yet. The only drastic disadvantage is the increasing optical resolution mismatch in nanoscale technologies.

For circuit edit (CE), a process for access through chip backside is established as well with a FIB preparation technique processing towards STI level.

The back surface of the ultra thin silicon (UTS) produced for backside CE is full of opportunities for functional analysis of nanoscale devices because this preparation technique offers for analysis techniques with nanoscale resolution the unique option to keep the Integrated Circuit fully functional. UTS analysis potential matches the requirements for several technology generations to come. The utilization has just begun.

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