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CMOS low noise amplifiers for 1.575 GHz GPS applications

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Abstract. This paper presents Low Noise Amplifier (LNA) versions designed for 1.575 GHz L1 Band Global Positioning System (GPS) applications. A 0.35 μm standard CMOS process is used for implementation of these design versions. Different versions are designed to compare the results, analyze some effects and optimize some critical performance criteria. On-chip inductors with different quality factors and a slight topology change are utilized to achieve this variety. It is proven through both on-wafer and on-PCB measurements that the LNA versions operate at a supply voltage range varying from 2.1 V to 3.6 V drawing a current of 10 mA and achieve a gain of 13 dB to 17 dB with a Noise Figure (NF) of 1.5 dB. Input referred 1 dB compression point (ICP) is measured as −5.5 dBm and −10 dBm for different versions.

1 Introduction

The demand on current GPS applications forces the design of high performance, low cost L1 frequency band (1.575 GHz center frequency) receivers. Galileo/GPS combined system is under development and this will allow the realization of much higher precision applications (Alvarado et al., 2007). On the other hand, the Assisted GPS (A-GPS) concept necessitates the integration of GPS receiver into the mobile phone requiring improvement in receiver sensitivity, linearity and power consumption (Bokinge et al., 2006; van Diggelen, 2002). The demand is more intensive on highly integrated, compact solutions. Therefore, the GPS receiver building blocks should be convenient for SoC or possibly SiP implementation with a small amount of off-chip circuit components as possible. The target is to design an LNA with an optimum layout to be integrated in a receiver chip. The input and output of LNA is optimized for 50 Ω terminations making it suitable for integration into heterodyne receiver structures with external Image Reject Filter. A block diagram of a possible application is depicted in Fig. 1.

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LNA is a critical building block on the received signal path. Important parameters of the performance of a receiver such as Noise Figure (NF), input impedance matching, reverse isolation, stability and linearity performance are mainly determined by the LNA (Razavi, 1998). The circuit topology and component selections to improve LNA performance in one criterion do not usually work in favor of all other performance criteria. Thus, a compromise is to be done during the decision for circuit topology and components. One of the performance criteria may take the priority depending on the application needs. Different versions are designed for this purpose through utilizing different Q on-chip inductors and a slight topology change. A highly integrated solution implemented in a standard CMOS technology with lower mask costs is a critical design target.

Different versions of LNA are designed and fabricated with a 0.35 μm standard CMOS technology and measurements are performed on-wafer and on-PCB. The design procedure and experimental results with comparisons are presented in this paper.

2 LNA circuit design

As mentioned in the introduction part, the NF of LNA has the most critical effect on the overall NF of the system. In order to have an overall NF of less than 2 dB for high precision GPS applications, the LNA NF should be kept well below 1.5 dB. 1.2 dB NF for the impedance-matched LNA in package could relax the noise requirements of cascaded components. A summary of the requirements are given in Table 1.

Different topologies are considered to achieve the performance targets. The LNA should provide sufficient gain at a bandwidth of 20.46 MHz for GPS L1 band applications. An amplifier topology with an inductive-capacitive load can achieve this requirement. Furthermore such a load selection keeps the NF at a low level. An ideal LNA should provide isolation of the signals at the input and output very well. The parasitic signals at the output of the LNA should not couple to the LNA input, possibly resulting in parasitic signal

Table 1. Target requirements.

Supply voltage	2.1 V ... 3.6 V
Supply current	10 mA
Center frequency	1.575 GHz
Input/output impedance	50 Ω
S11, S22	<-10 dB
S21	>15 dB
S12	<-25 dB
NF	<1.5 dB
ICP	-10 dBm

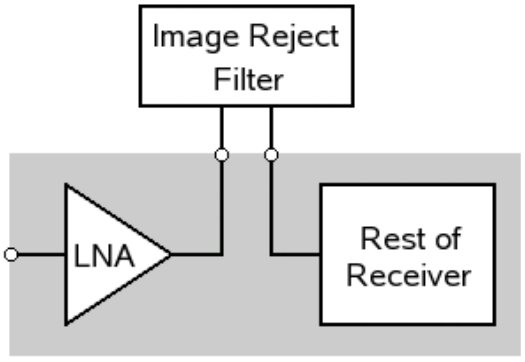

Fig. 1. Integration of LNA in a GPS receiver.

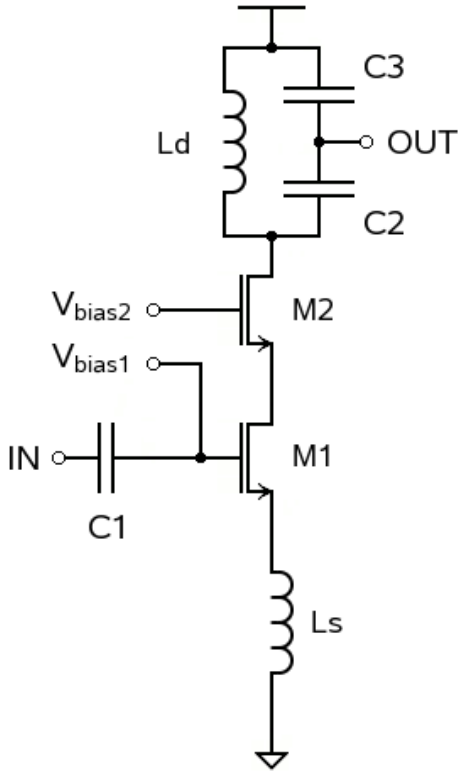

Fig. 2. Simplified core circuit of LNA.

transmissions from the antenna. This performance specification can be optimized through minimizing S12 parameter of the LNA. This attenuation in the reverse signal path, in other words reverse isolation is very critical for the overall receiver performance as well. In addition to this fact, a low S12 value provides the stable operation of an LNA. As well as providing reverse isolation and stability which are very critical, good isolation of input and output stage of the LNA brings the advantage of treating input and output impedance matching separately, performing some changes at the input stage of LNA for better impedance matching does not disturb the impedance seen at the output drastically. Using a cascode amplifier topology provides adequate reverse isolation and stability. The inductive degeneration topology provides the amplifier to achieve real input impedance. This is critical for input impedance matching with 50 Ω. Regarding these considerations, an amplifier topology with cascode n-MOS transistors, inductive capacitive load and a source degeneration inductor is selected for core circuit of LNA. This circuit is depicted in Fig. 2.

The inductive source degeneration proves good results when input impedance matching is considered. It provides creating a resistive part in addition to the reactive part seen at the gate of the input n-MOS transistor. This fact can be mathematically expressed with the following Eq. (1) where C_{gs} is the gate-source capacitance of input transistor M1 and g_m is its transconductance.

$$Zin = jwL_s + \frac{1}{jwC_{gs}} + \frac{g_m L_s}{C_{gs}} \quad (1)$$

It is a hard task to fix the input impedance exactly to 50 Ω using only a degeneration inductor. Trying to increase the transconductance through increasing the width of the transistor does not help to improve the resistive part of input impedance. In addition, the possibility of increasing transconductance through increasing the current is also limited since there is a maximum limit for the current consumption. Increasing the value of L_s helps to increase the resistive part of impedance, however, when small signal analysis is considered, it is obvious that increasing the source degeneration inductance results in lower gain. Due to technology and design limitations, the real part is lower than required 50 Ω. There is also a capacitive part of input impedance. To balance this and achieve a good input matching, an inductor should be placed on the signal path prior to the gate of input transistor. The Noise Figure considerations indicate that an inductor on the signal path should have a high quality factor in order to contribute less to the NF. On-chip inductors do not have a high enough quality factor for this application in the circuit with the given technology. Due to these facts, the inductor used for matching (L_{match}) is implemented as a high Q off-chip component. The bond wire inductance, effect of package and PCB parasitic circuit elements should

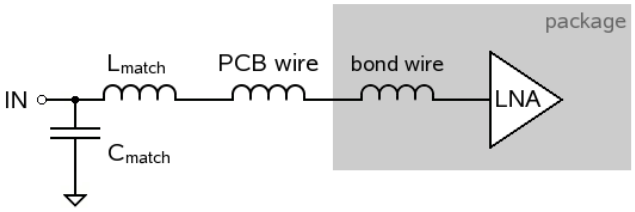

Fig. 3. Input impedance matching and parasitics of package and PCB.

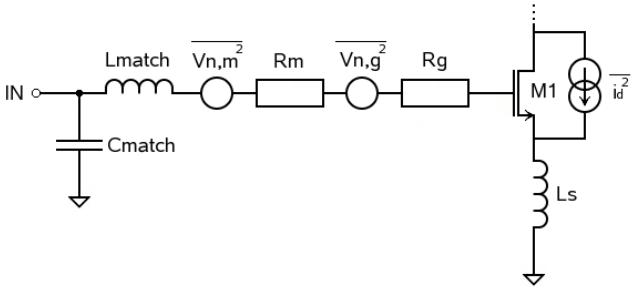

Fig. 4. Noise equivalent circuit of LNA.

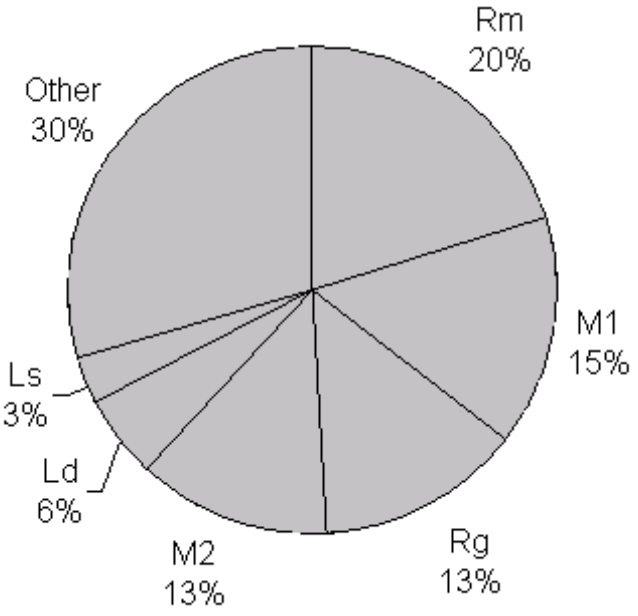

Fig. 5. Contribution of noise sources in LNA circuit.

be modeled accurate and taken into account for a good input impedance matching at the desired frequency range. To compensate the inductive impedance and to fix the resistive part exactly to 50 Ω, a matching capacitor C_{match} is also utilized. The circuit showing the off-chip components placed on the input signal path and the parasitic inductive effects of package and PCB are depicted in Fig. 3.

The main noise sources of a LNA with such inductive degeneration topology are the intrinsic thermal noise of input transistor M1, the gate resistance associated with it (R_g) and the resistance dependent to the Q of off-chip inductance for matching and the bond wire and conductor on PCB (R_m). The noise equivalent circuit for the LNA at the input transistor side is shown in Fig. 4.

As long as there is a good input matching, the LNA can be treated as a voltage amplifier for noise calculations and its noise factor F can be taken into consideration (Shaeffer and Lee, 1997). The noise considerations given in Shaeffer and Lee (1997) state the following Eq. (2) for the noise factor F;

$$F = 1 + \frac{R_m}{R_s} + \frac{R_g}{R_s} + \gamma \cdot R_s \cdot g_{d0} \cdot \left(\frac{w_0}{w_T}\right)^2 \qquad (2)$$

This assumption is valid as long as the resonance of amplifier with the input circuit is achieved and w_0 is the resonant frequency. The resonant frequency should be fixed at the desired center frequency, 1.575 GHz. The n-MOS transition frequency is w_T which is equal to g_m/C_{gs}. R_s is the source resistance which is 50 Ω, R_m is the resistance due to off-chip inductor, bond wire and wiring on application board. R_g is the resistance associated with the gate of input n-MOS transistor. γ is a bias dependent factor and $g_{d0}$is zero bias drain conductance (Bokinge et al., 2006; Shaeffer and Lee, 1997).

Optimum values for zero bias drain conductance, gate resistance and the resistance of matching inductor should be achieved for a better noise performance. Gate width of n-MOS transistor and the inductance L_{match} are decided through a set of simulations to optimize noise parameters. The simulation results for the sources of noise in the LNA circuit are shown in the diagram above. The contribution of input transistor thermal noise and noise due to resistances on signal path can be compared.

The noise model for on-chip components and the estimated series resistance for off-chip discrete matching inductor are used for this simulation. It can be concluded that using an on-chip inductor instead would have contributed much more on the overall NF.

The load inductor L_d and the source degeneration inductor L_S are implemented as on-chip inductors to have a more compact solution. For such an implementation, the inductor modeling should be completed before the necessary simulations. The inductor values and their quality factors should be known and the parasitic extractions should be performed. The load inductor resonates with two capacitances and maximizes the gain at a resonant frequency. The output impedance seen at this frequency is ideally only resistive and 50 Ω for a good matching at the output. The capacitors, C_2 and C_3 have much higher quality factor compared to the inductor. Therefore, the overall Q of the load is mainly determined by the Q of the inductor. Utilization of a higher Q inductor will generate a sharper resonance characteristic and as a result a sharper gain (S21) characteristics at the frequency range of interest with a high maximum value of S21.

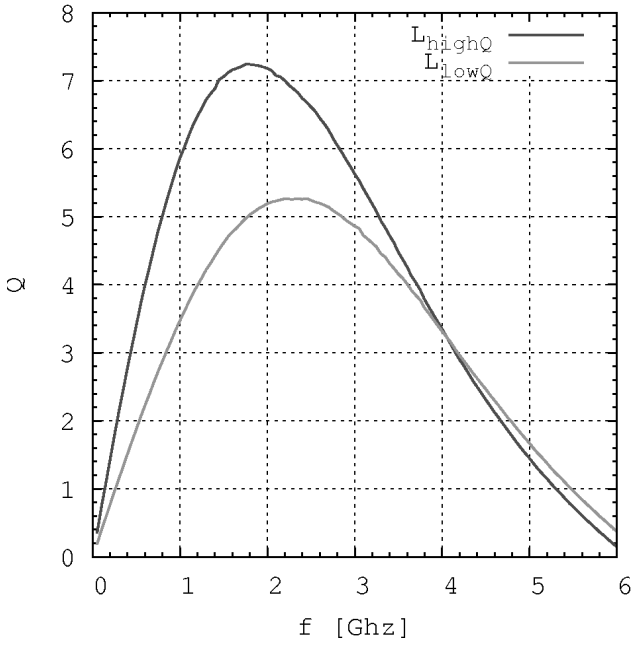

Fig. 6. Quality factors of 7 nH inductors L_d.

On the other hand an inductor with a low Q at the operation bandwidth will cause a smoother S21 characteristic, providing a higher available bandwidth but with a decreased value of maximum S21. The process variations should be taken into account during the simulations for deciding component values. A gain characteristic with a high maximum value and a bandwidth fitting the requirement can be fixed at the center frequency of 1.575 GHz. However, the process variations may alter the component values and shift the resonant frequency. The absence of a perfect package modeling may cause a more serious problem. Designing a higher bandwidth LNA with a decreased maximum gain provides more flexibility against these problems. It is decided to investigate the optimum Q of the available on-chip inductors to have an optimized S21 response. Two different 7 nH inductors with different quality factors are used for this purpose. Two different versions of LNA with the same topology are designed. The capacitor values to resonate with the inductor are also slightly different for the two versions as well to achieve resonance at the desired frequency and to obtain good output matching (S22 characteristic). The Q of two 7 nH inductors used for this design can be viewed in Fig. 6.

A third version of LNA for this investigation is also designed. The high Q inductor is used as load inductor. The source degeneration inductor L_s is not implemented on-chip. The gain can be increased by more than 3 dB by eliminating the source degeneration inductor. For this purpose, the source of input transistor is directly connected to the ground of the chip. The bond wire inductance acts as a degeneration inductor in this condition. A perfect modeling of such inductance realized by the bond wire effects in the package is difficult. However, it provides the presence of resistive part of input impedance. Different matching inductor and capacitor should be used on the application board compared to the first two versions. It is difficult to predetermine these values through simulations unless there is a very realistic model for package effects. This configuration can be utilized to maximize the gain despite having a complicated input matching and possibly stability problems. Small signal analysis on the circuit indicates that removing L_s results in a worse reverse isolation and hence stability problems.

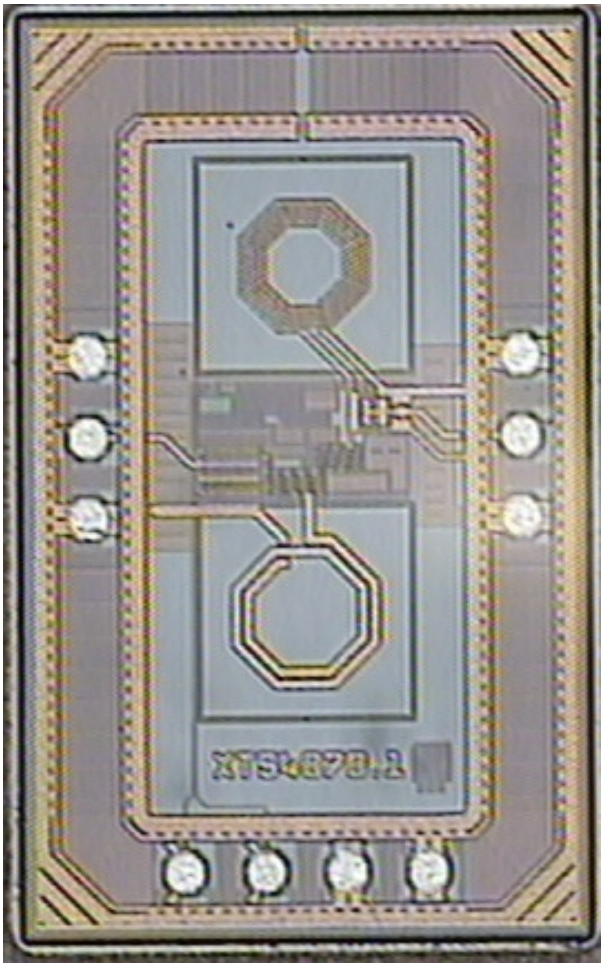

Fig. 7. IC photo of one LNA version.

3 Results

The LNA is encapsulated in a SOIC16 Ceramic Package. Measurements are performed on-wafer and on application board. Measurements are performed for the three design versions with different load and degeneration inductor implementations. The chip microphotograph of the design version

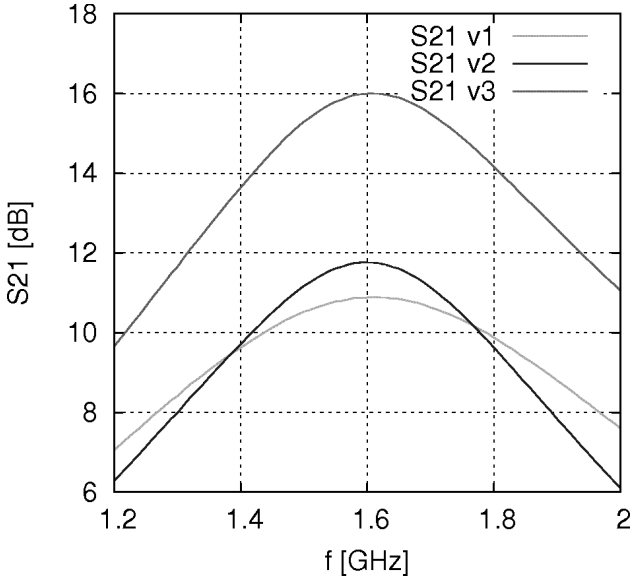

Fig. 8. S21 comparison of three design versions.

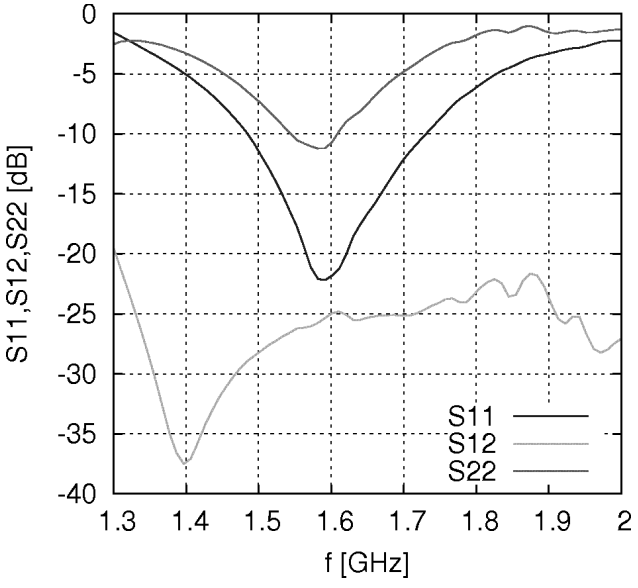

Fig. 9. S11, S12 and S22 of packaged LNA version 2.

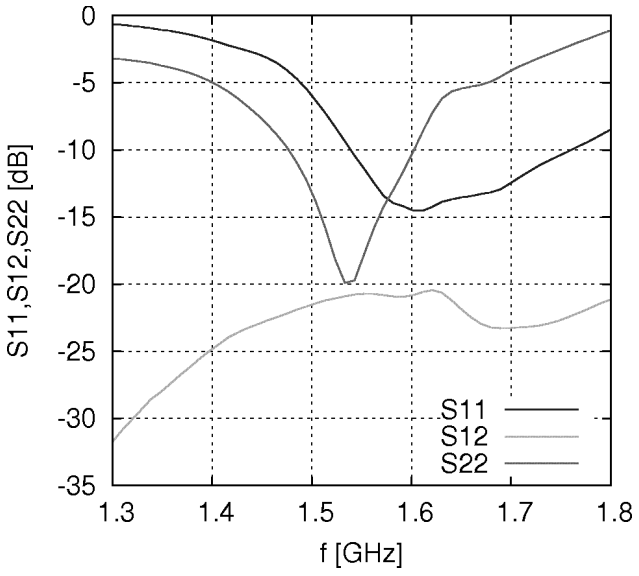

Fig. 10. S11, S12 and S22 of packaged LNA version 3.

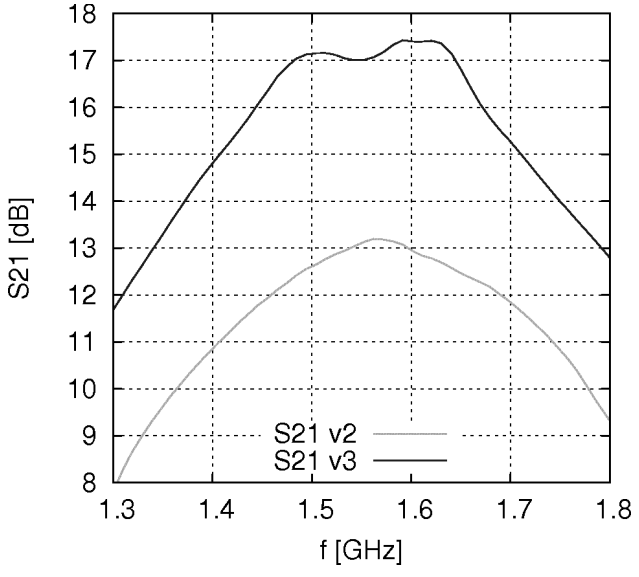

Fig. 11. S21 Comparison of packaged LNA versions 2 and 3.

with high Q on-chip inductor and on-chip degeneration inductor is shown in Fig. 7.

The set of investigations are performed on three different LNA versions with different load inductors and a slight topology difference. The comparison of S21 curves are shown in Fig. 8.

The figure shows the comparison of on-wafer measurements on the three versions. Version 2 with a high Q load inductor has a sharper response compared to first version as expected. In addition, the third version which includes no on-chip degeneration inductor has an upwards shifted response as expected. The output matching and noise figure measurements on-wafer fits to the simulated results well.

The S-parameter and NF measurements on the application PCB for version 2 and version 3 are shown in Figs. 9, 10, 11 and 12.

A good impedance matching at the input and output is achieved for both versions with S11 and S22 less than -10 dB at the frequency range of interest. The values of off-chip components are optimized to have a good input matching and noise figure. Although the on-wafer measurements fit the simulated results well, the measurement on the application board does not fit to the simulation results due to

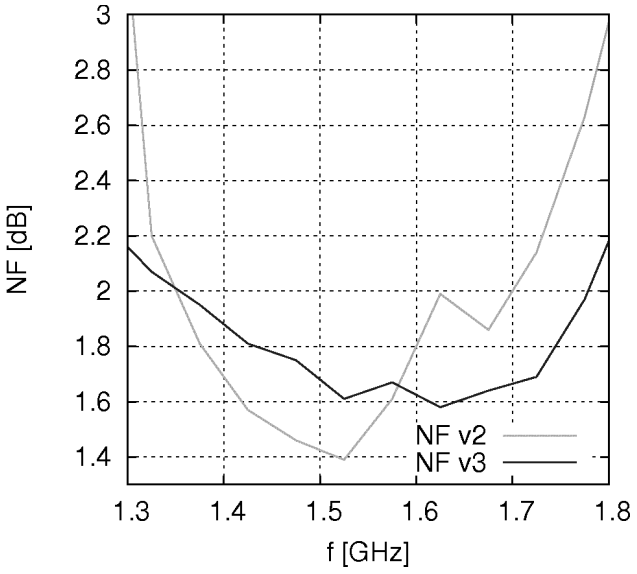

Fig. 12. NF Comparison of packaged LNA versions 2 and 3.

incomplete modeling of package and PCB parasitics. A reverse isolation (S12) better than 25 dB and 20 dB and S21 of 13.5 dB to 17 dB at the frequency range of interest is achieved. The NF is higher than expected 1.3 dB from the simulations. However the later narrowband noise measurements prove better results with a NF of 1.5 dB for both versions. Input referred 1 dB Compression Point (ICP) is measured as −5.5 dBm whereas the input referred third Intercept Point (IIP3) is measured as 3.3 dBm for version 2. ICP and IIP3 for version 3 are measured −10 dBm and 1 dBm, respectively. These results indicate a very good linearity performance of the device. The measurements are performed for supply voltage range varying from 2.1 V to 3.6 V and only negligible changes are observed. When stability issues are considered, it can be concluded that a stable operation for version 1 and version 2 is achieved. On the other hand version 3 has some stability problems at a frequency range of 200 MHz close to the frequency band of interest. This is again due to the incomplete modeling of parasitic effects.

A better performance for this application can be provided with more accurate modeling of package and PCB. The LNA IC can be integrated into a SiP environment. The matching elements can be implemented as components on a ceramic substrate and can be packaged together with LNA IC. A good performance can be achieved with an accurate 3-D substrate and package modeling for such application. Utilizing bond wire inductance as a circuit component in the design is a very strong motivation for these investigations since it obligates a prefect 3-D modeling for more realistic simulations.

4 Conclusion

Three 1.575 GHz low noise amplifier versions implemented with a 0.35 μm CMOS technology were presented. The experimental results indicate 17 dB gain and 1.5 dB noise figure. A high linearity with an IIP3 of 1 dBm is achieved. Further investigations to integrate this IC to a SiP environment are in progress. The performance can be improved with a SiP solution.

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