System considerations and RF front-end design for integration of satellite navigation and mobile standards

A. Miskiewicz^{1,2}, A. Holm¹, and R. Weigel²

Abstract. The paper presents the challenges involved in a system design of a robust reconfigurable RF front-end for navigation and mobile standards. Receiver architecture is chosen from the point of view of inter-system interference and 130nm CMOS process characteristics. System concept covers the implementation of GPS, Galileo, UMTS, GSM and CDMA2000 using a Zero-IF architecture with reconfigurable analog and digital path. Feasibility studies of the system cover analysis of the wireless regulations and performance criteria, such as overall gain, noise figure (NF), and 1dB compression point (P1dB) of the RF chain, phase noise requirements and VCO tuning range [1]. The presented chip was fabricated in 130 nm CMOS technology. System considerations are confirmed with the chip measurements of gain, noise figure, and linearity. Prospects for the future work are presented including technology shrink.

1 Introduction

Current market of mobile handsets with navigation capabilities is driven by two main factors: government regulations and commercial demand. With introduction of E-911 mandate by the United States, mobile operators are required to provide localisation of mobile subscribers calling an emergency service. On the other hand, there is a demand for enhancing the penetration of Location Based Services (LBS), which provide users with a wide variety of geographically-referenced information. Both of these functions require precise positioning information, which cannot be derived from classical network solutions (such as triangulation in mobile networks). The use of navigation services is inevitable if the quality of the service needs to be high, especially in urban environment, where the signals are weak.



Correspondence to: A. Miskiewicz (anna.miskiewicz@infineon.com)

With the agreement between the government of the United States and the European Union, which leads to a full interoperability of GPS and Galileo, a new market for combined navigation receiver has been created. Integration of both systems into a Global Navigation Satellite System (GNSS) should supply users with highly precise and reliable positioning service. As market demand for integrated mobile phones with GPS (and Galileo) functionality is already a fact, it is desirable to account for that expansion now and develop a highly competitive multifunctional hand-held receiver. Such a receiver should support both navigation and mobile standards, not only those already widely used, but also those under development. On the other hand, a low-cost production, low current consumption, and small chip size require a highly-reconfigurable architecture. Implementation of both GPS and Galileo has been the core task of chip development. Mobile communications standards increase the competitiveness of the receiver in terms of operation capabilities, as long as cost, chip size and current consumption are acceptable. Therefore, a trade-off between the number and type of implemented standards and chip overall performance has been made. Considering the above requirements, the standards presented in Table I have been selected for the multi-mode receiver.

2 Satellite navigation receiver overview

Both GPS and Galileo are spread-spectrum systems, where the navigation message is multiplied with the pseudo-random noise (PRN) code specific to the satellite transmitter. The PRN codes are orthogonal, therefore all satellites can send the signals using the same centre frequency and bandwidth. For Galileo signal, the result of navigation message and PRN code multiplication is additionally multiplied with a subcarrier frequency of 1.023 MHz (Fig. 1). The last stage of the signal generation for both GPS and Galileo

¹Infineon technologies AG, Neubiberg, Germany

²University of Erlangen-Nuremberg, Erlangen, Germany

Table 1. Implemented standards.

A-GPS	Galileo	UMTS	CDMA2000	GSM
L1	E1	II-III V-VI VIII-IX	PCS 1900 Cell 850	850 900 1800 1900

Table 2. Satellite navigation standards.

	GPS L1 [3]	Galileo E1 [4]
Centre frequency	1575.42 MHz	1575.42MHz
Modulation type	DSSS-BPSK	DSSS-MBOC(1,1)
Spreading code chip rate	1.023 Mcps	1.023 Mcps
Spreading code length	1023 chip	4092 chip
Data rate (nav. message)	50 sps	250 sps
Bandwidth (RF)	2.046 MHz	4.092 MHz
Nominal S/N @GPS antenna	$-19 \mathrm{dB}$	$-19 \mathrm{dB}$
Max. sensitivity (indoor/outdoor)	$-130/-155\mathrm{dBm}$	-127/-152dBm

is an up-conversion using a multiplication with a carrier of 1575.42 MHz.

Maximum power level of signals arriving from the satellite to the receiver on the Earth surface is around -130dBm for GPS and $-127 \, dBm$ for Galileo signals. For the case where no direct Line-of-Sight (LoS) between transmitter and receiver is available, the signals can be further attenuated by more than 20dB due to tree foliage, multipath propagation in urban canyons or attenuation through walls and roofs for in-door navigation [2]. Therefore, the GPS and Galileo specifications define only maximum available signal power at the Earth surface and not the minimum sensitivity, as it is the case for mobile standards. For state-of-the-art low-cost receivers integrated in a mobile platform the bandwidth of the GPS and Galileo signals is limited to the first main lobe for GPS signal and two main lobes for Galileo standard. The bandwidth is mainly defined by the off-chip SAW filtering. Tab. II presents overall RF specification of GPS standard in L1 band and Galileo standard in E1 band.

Chip cost and size considerations suggest a re-use of an already existing processor to run GPS algorithms, rather than to add another processor on the positioning chip. Based on the system integration requirements, a host-based hardware solution has been suggested. Figure 2 presents the proposed navigation chip partitioning.

3 RF front-end

According to Galileo and GPS specification documents, there are no specific test cases to be considered in GNSS receiver design. However, multimode receiver application requires consideration of test cases, which are relevant for the

Table 3. Out-of-band blockers.

Blocker	Freq (MHz)	P_B (dBm)
UMTS b3 UL	1710	10
GSM 900 UL	915	10

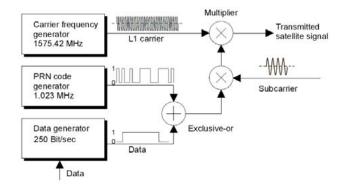


Fig. 1. Simplified diagram for Galileo signal generation.

definition of RF front-end blocks, such as amplifiers, interstage filters and mixers [5]. These requirements are imposed by large blocker levels and possible intermodulation products, which may fall into GPS and Galileo receive band.

Based on the specifications for mobile standards implemented in the chip, a set of GNSS-signal specific test cases has been created and simulated (Table 3–5).

The purpose of the Zero-IF RF front-end is to receive, amplify, filter, down-convert and sample the signal to enable further baseband signal processing.

As presented in Fig. 3, a configuration with two separate antennas is proposed. There are two paths – one for GNSS reception and one reconfigurable chain for proposed mobile standards. After the second amplifier, an integrated switch is implemented, which enables choosing the type of received signal. Further blocks are common for both mobile and navigation standards. This solution offers high reconfigurability and lower cost of implementation for multiple standards.

After the signal is received in the antenna, it is filtered and amplified in a low-noise amplifier, which is followed by RF filtering. These steps are performed off-chip. The main target of the navigation path is low noise figure of the chain and a RF bandwidth of at least 4MHz [6]. For mobile standards the reconfigurability was the main focus in the design process. The analog part is short, featuring only the second LNA, mixer and analog baseband filter. Due to moderate analog gain in the front-end, the requirements for DC offset are relaxed. Further, the baseband filter attenuation of the adjacent channels is moderate. Additional filtering is integrated in the digital front-end, where DC offset compensation is also implemented. For the common path, mixer of a high

Table 4. Second-order intermodulations.

Blocker 1	Freq (MHz)	P_B1 (dBm)	Blocker 2	Freq (MHz)	P_B2 (dBm)
GSM 900 DL GSM 850 UL		-25 10	802.11b, g 802.11b, g		-10 -10

Table 5. Third-order intermodulations.

Blocker 1	Freq (MHz)	P_B1 (dBm)	Blocker 2	Freq (MHz)	P_B2 (dBm)
UMTS b2 UL	1850	10	UMTS b1 DL	2124	-25
UMTS b2 DL	1990	-25	802.11b, g	2412	-10
UMTS b3 DL	1805	-25	802.11a	5190	-10

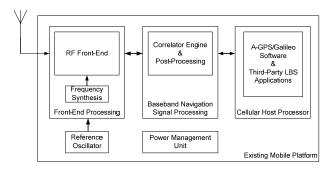


Fig. 2. GPS/Galileo chip partitioning.

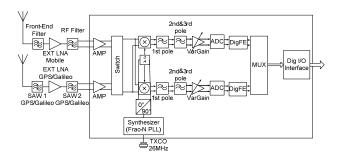


Fig. 3. Implemented receiver front-end.

linearity has been implemented, which allows relaxed frontend filtering. Due to constant gain approach in the frontend no switching transients are present in the chip, however external gain steps are necessary for mobile standards. The setup is finalized with a high-resolution continuous-time Sigma-Delta ADC, which is immune to high level interferers and enables low-gain analog front-end implementation. Proposed front-end architecture implements additional baseband digital processing, including filtering, decimation, fractional sample rate conversion, and compensation of unwanted RF-FE effects.

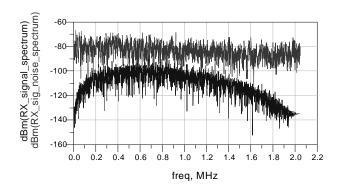


Fig. 4. Simulated Galileo signal spectrum and signal plus noise spectrum after the receiver front-end.

The front-end has been simulated for GPS and Galileo signals. Figure 4 presents the typical Galileo spectrum at the output of the analog front-end part. The influence of the front-end has been determined by comparison of the input spectrum at the antenna and the spectrum after down-conversion and filtering.

The simulated signal-to-noise deterioration in the frontend is acceptable for the satellite navigation signal reception. Based on the level-plan calculation appropriate values of gain, NF, and P1dB have been selected for RF blocks in the chain. Table 6 presents an overview of typical block performance.

4 Measurements

The chip was fabricated in $130\,\mathrm{nm}$ CMOS technology and packaged in $5\times5\,\mathrm{mm}^2$ WFBGA package. The analog performance for GPS and Galileo was measured including off-chip filters and LNA. The gain results were corrected for the additional gain in digital front-end. The input match-

Table 6. Block performance for gps/galileo path.

	Gain (dB)	NF (dB)	IIP3 (dBVrms)
SAW1	-0.8	0.8	N/A
EXT LNA	20.2	2.0	-15.2
SAW2	-1.1	1.1	N/A
AMP	10.5	4.5	-7.7
Mixer+1st pole	32.0	19.9	-6.3
2nd & 3rd pole	6.0	42.4	21.0
Overall	66	3.2	-45.3

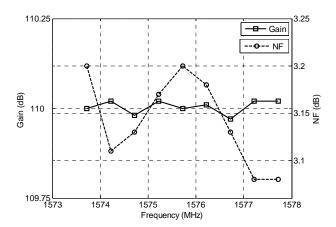


Fig. 5. Measured gain and noise figure for GPS/Galileo path.

ing, gain, noise figure, and linearity conform to the simulated results. For a setup with an external low-noise amplifier, the noise figure is 3.2 dB. Due to the fact, that the amplifier and mixer blocks are wideband, the measured out-of-band 1dB compression point is comparable to the in-band value. The measured current consumption equals 60 mA and 58 mA for 1.5 V and 2.85 V domains respectively. The current consumption may be optimized by the adjustment of the digital front-end settings and lower the linearity of the analog blocks, at the cost of additional required selectivity in the off-chip components.

5 Summary

Highly reconfigurable multimode, multiband receiver integrated in 130nm CMOS technology has been presented. The chip enables implementation of assisted-GPS and future assisted-Galileo standards using only one receiver chip. The reconfigurability is possible because of the wideband analog blocks, high dynamics ADC and flexible digital front-end. The further steps include integration of mobile transmitter paths in the chip and technology shrink to the next node of 65nm CMOS technology.

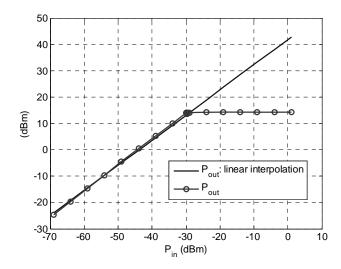


Fig. 6. Measured 1 dB compression point.

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