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Impact of negative and positive bias temperature stress on 6T-SRAM cells

S. Drapatz[1,2], **G. Georgakos**[2], **and D. Schmitt-Landsiedel**[1]

[1]Lehrstuhl für Technische Elektronik, Technische Universität München, Germany
[2]Infineon Technologies AG, München-Neubiberg, Germany

Abstract. With introduction of high-k gate oxide materials, the degradation effect *Positive Bias Temperature Instability* (PBTI) is starting to play an important role. Together with the still effective *Negative Bias Temperature Instability* (NBTI) it has significant influence on the 6T SRAM memory cell. We present simulations of both effects, first isolated, then combined in SRAM operation. During long hold of one data, both effects add up to a worst case impact. This leads to an asymmetric cell, which, in a directly following read cycle, combined with the generally unavoidable production variations, maximizes the risk of destructive reading. In future SRAM designs, it will be important to consider this combination of effects to avoid an undesired write event.

1 Introduction

The ongoing miniaturization in semiconductor industry has already led to decananometer transistors (ITRS roadmap). As the voltage cannot be scaled according to geometry and gate oxides are getting thinner, electric fields and tunneling currents in the devices are increasing. This was exacerbating *Negative Bias Temperature Instability* (NBTI) and leakage in the past years. In order to reduce these harmful effects (especially leakage), thicker gate oxide materials are needed. To keep the ability to store charges and control the MOSFET channel, the dielectric constant must then be higher than in conventional SiO_2. This is done with the introduction of high-k gate oxide materials.

One disadvantage of these new materials is an upcoming effect similar to NBTI: *Positive Bias Temperature Instability* (PBTI), which occurs predominantely on nMOS transistors, while NBTI is effective mainly on pMOS transistors. In the past, NBTI alone fortunately did not have huge impact on the SRAM memory cell performance (Fischer et al., 2007). But does the additional effect PBTI together with the still effective NBTI have a significant influence on SRAM core cell performance?

The following section gives a brief overview on the degradation mechanisms NBTI and PBTI. To quantitatively measure the influence of these effects on the SRAM 6T core cell, a benchmark is required. This is done with some metrics to describe the quality of the memory cell, introduced in Sect. 3. Using these metrics, the impact of NBTI and PBTI on SRAM is simulated in Sect. 4. Next, it is examined to what extent normal usage of the memory cell, i.e. hold, read and write, leads to BTI stress conditions of the single transistors. The worst use case will then be isolated and considered in the last section separately together with variation and yield considerations.

2 NBTI and PBTI

In this section, both degradation effects *Negative Bias Temperature Instability* and *Positive Bias Temperature Instability* are introduced.

2.1 NBTI degradation

NBTI is an effect only influencing pMOS transistors. It is caused by the following scenario: negative potential at the gate relative to higher potentials on source and drain. For standard CMOS circuits this means gate connected to V_{SS}, source and drain connected to V_{DD}. This leads to a conducting transistor without current in the channel (Fig. 1).

The failure mechanism NBTI is still under discussion, but it seems to be clear that the stress condition breaks silicon-hydrogen bonds, and the hydrogen ions diffuse away. These vacant positions, acting as traps, can bond holes. These additional holes in the gate oxide cause a decreasing threshold

Correspondence to: S. Drapatz
(stefan.drapatz@tum.de)

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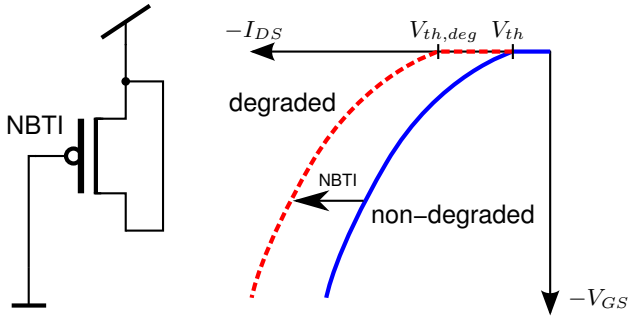

Fig. 1. Stress conditions and impact of NBTI to pMOS transistors

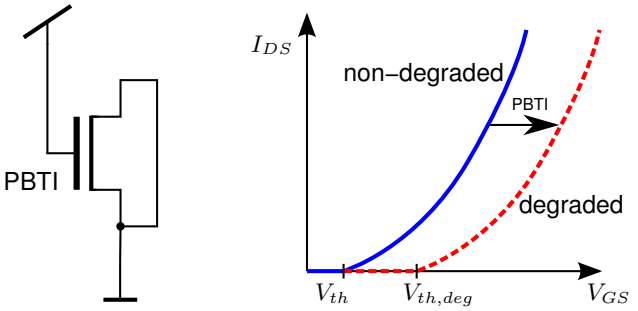

Fig. 2. Stress conditions and impact of PBTI to nMOS transistors.

voltage, e.g. from -0.5 V it goes down to -0.55 V. This makes the transistor weaker over time, and a circuit built of this transistor is getting slower (Fig. 1). Typical threshold voltage drift values in 65 nm technology: after 8 years of stress at $V_{DD,\mathrm{nom}}$ and 125°C there will be a mean drift value of approx. 60 mV.

2.1.1 NBTI distribution

NBTI is a statistical process. There is a distribution of single drift values, but the simulation tools so far can only handle and predict the mean value of this distribution. Analyses have shown that a stress of 10 000 s at 125°C lets the mean value drift for approx. 45 mV, but single devices have shown a drift of up to 150 mV (Fischer et al., 2007). Especially for SRAM with a huge number of cells in an array, this means that single memory cells will experience big drifts.

2.1.2 NBTI annealing

Additionally, NBTI shows a recovery effect: directly after end of stress, the threshold voltage drift is worst, but is annealing with a short time constant, depending on the duration of the stress (Heinrigs et al., 2007). This means that for a circuit it would be worst to work with this high amount of threshold voltage drift during or very shortly after stress. If the circuit only experiences the annealed drift values, the impact would be much less. It is not analysed so far how strong relaxation effects influence the SRAM circuits.

2.2 Expected PBTI degradation

Contrary to NBTI that is relatively well-known in the meantime, PBTI was not much researched in the past. Many papers are available for NBTI, but PBTI is just coming up. The reason is clear: up to now, it did not occur on semiconductor chips without high-k gate oxide.

Only with the introduction of these new materials, the PBTI effect appears. This is because NBTI is based on traps for holes, which only happens at the interface states. PBTI, however, is based on electron trapping, which mainly happens in high-k bulk as well as in high-k SiON interfacial layer. PBTI only works on nMOS transistors, and according to that the stress condition is contrary to NBTI: positive potential on the gate, zero potential on source and drain. This lets the threshold voltage drift to higher values, so both NBTI and PBTI weaken the devices over time (Fig. 2).

In summary, PBTI is not yet as good analyzed as NBTI, but the behavior seems to be very similar (Zafar et al., 2006). Within the scope of this work, we therefore assume the PBTI threshold voltage drift to behave like NBTI in terms of absolute value, distribution and annealing.

3 Modeling and SRAM metrics

For modeling, we use the following approach: ΔV_{th} together with $\mathrm{Sensitivity}_{\mathrm{SRAM}}$ results in $\mathrm{Degradation}_{\mathrm{performance}}$.

The transistor parameter drift ΔV_{th} is the direct result of the NBTI and PBTI effects, as described in the previous section. Together with the sensitivity of the SRAM circuit $\mathrm{Sensitivity}_{\mathrm{SRAM}}$, it results in a degraded performance of the SRAM cell $\mathrm{Degradation}_{\mathrm{performance}}$. The schematic of the 6T-SRAM cell that is used for this work is shown in Fig. 3.

While "performance" at e.g. logic gates would refer to delay, in memories it refers to some metrics that describe the "quality" of the memory cell. Three standard metrics are described in the next sections.

3.1 "Static Noise Margin (SNM)" or "Is it safe to read?"

When a data is read from memory, it is important that the cell does not flip because of this read cycle. The metric determining how safe is the read operation is called SNM(read). It is measured in Volts and determines how much additional noise voltage is necessary to flip the cell. The smaller this metric, the less stable the cell. SNM is also available for hold case and determines how much additional noise voltage is necessary to flip the cell under hold conditions. Under hold conditions, the cell is much more stable than under read conditions, which would make this SNM(hold) metric dispensable. The reason to keep this metric is that under hold conditions, it is common to reduce V_{DD} in order to minimize

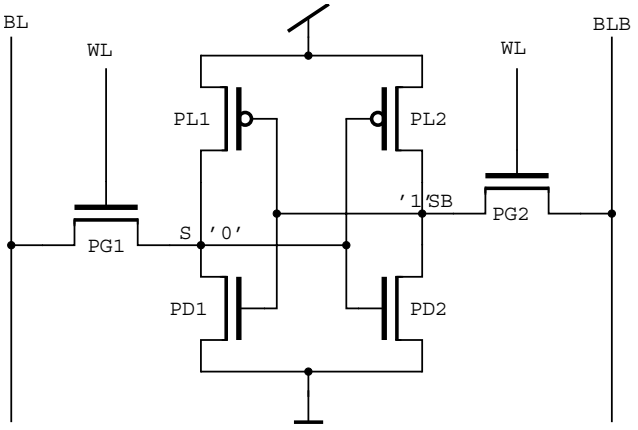

Fig. 3. Schematic of 6T SRAM circuit with naming conventions and assumed memory state: "0"on left side.

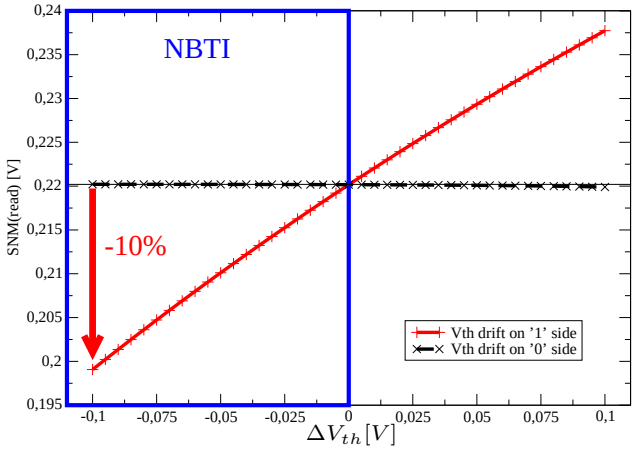

Fig. 4. Impact of threshold voltage drift of pullup transistor on read stability: 10% loss at −100 mV Vth drift

static power dissipation, which on its part reduces read stability as well. In this work, the focus is on SNM(read), because it is the most critical memory cell parameter.

3.2 "Write Margin" or "Is writing possible?"

Besides reading, it is also necessary for a memory cell that safe writing is possible. When writing conditions are applied to the memory cell, it must be sure that the cell will flip accordingly. This metrics called "Write Margin" determines how easy is writing, i.e. at which voltage applied to the according bitline the cell will flip. The higher the flip-voltage, the easier a zero can be written into the cell from the "low" BL.

3.3 "I(read)" or "How fast is reading?"

Speed, or in other words access time, is mainly determined by the current flowing in the channel of the access transistors. If it allows big current during the read cycle, faster discharging of the bitline capacity is possible. The bigger this metric "I(read)", the faster a memory cell can be read.

3.4 Safe reading or fast and writable?

All the mentioned SRAM metrics have opposite requirements. Either a cell can be optimized to safe reading or fast and easy writing, both optimizations are not possible together. For example, a cell which is optimized to safe reading will be characterized by a small access transistor and a big pulldown transistor to keep the output of the voltage divider (formed by the access and pulldown transistor) low. But this automatially slows down the cell, because fast access would require a wide access transistor. Additionally, it is getting harder to write, because this would require a small voltage drop across the access transistor.

In summary, the critical point in SRAM design besides minimizing the cell area is adjustment of the bias point as a tradeoff between readable, writeable and speed. Ongoing downscaling, especially in SRAM design, lets the margin get smaller. A back door for this increasing problem would be alternative SRAM circuit design, e.g. with more than 6 transistors, which of course needs more area per cell.

4 Sensitivity of SRAM circuit to BTI degradation

In this section, the sensitivity of the 6T SRAM circuit (Fig. 3) to BTI degradation of single transistors is examined. Since BTI degradation mainly causes V_{th} shifts, the impact of drifted threshold voltages is examined. The following analysis is based on hypothetical V_{th} drifts.

4.1 Sensitivity to NBTI-degraded pullup transistor

We present the consequence of ±100 mV V_{th} drift of one of the pMOS pullup transistors to SNM(read). This, as well as all following simulations, is done with a Spice-based simulation tool. DC simulations were performed with varying threshold voltage of PL1 or PL2. We see that −100 mV V_{th} drift result in approx. 10% SNM loss (Fig. 4). Two curves exist in the graph because of two states of the memory cell: if the threshold voltage drift is applied to the transistor on side where the "0" is stored (PL1), the dashed line results: no influence on the read stability. On the other hand, if the threshold voltage drift is applied to the side where the "1" is stored (PL2), the solid line results, which means reduction of the read stability. Of course, one cannot choose the better memory state, because the user operation is deciding. As a consequence, the worse result has to be chosen in these graphs.

Altogether, NBTI in the pullup transistor makes an SRAM cell more vulnerable to destructive reads, but better writeable

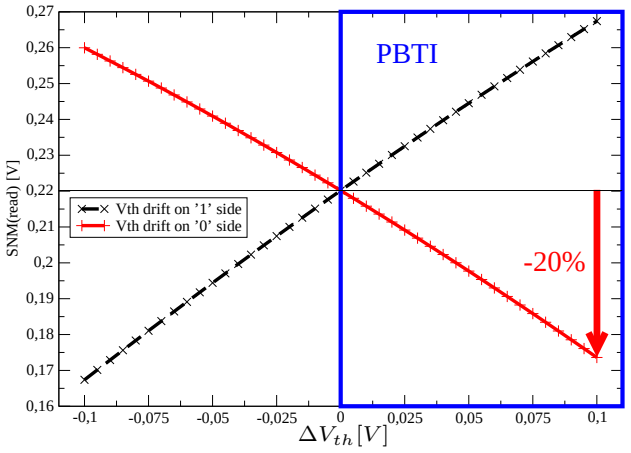

Fig. 5. Impact of threshold voltage drift of pulldown transistor on read stability: 20% loss at +100 mV V_{th} drift.

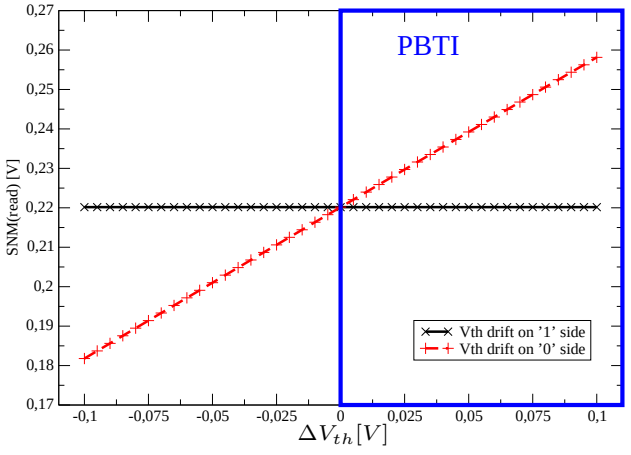

Fig. 6. Impact of threshold voltage drift of access transistor on read stability: no change for worst case.

in one memory state. It has no effect on access time since it does not change the read current.

4.2 Sensitivity to PBTI-degraded pulldown transistor

Again, V_{th} drifts up to $\pm$100 mV are applied. This time, one pulldown transistor (PD1 or PD2) gets varied, and +100 mV V_{th} drift result in 20% SNM loss. So the influence of V_{th} on read stability is approx. double for pulldown compared to pullup, i.e. if PBTI will be in the same range of V_{th} drift, the effect on read stability will be twice as high (Fig. 5).

4.3 Sensitivity to PBTI-degraded access transistor

Analysis of threshold voltage drift of the access transistor showed improvement of read stability for one memory state, but no worst case change (Fig. 6).

However, a weak access transistor decreases both the write level as well as the read current.

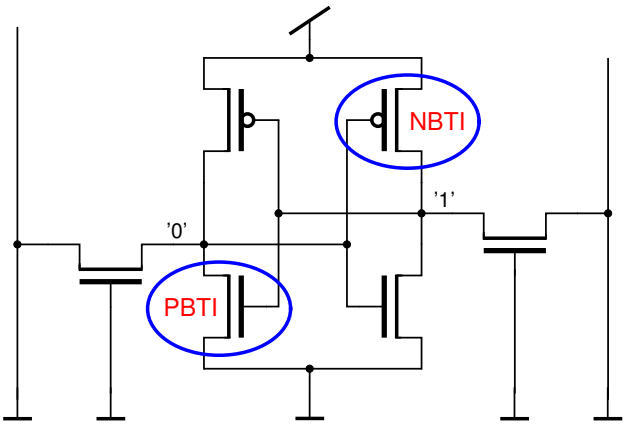

Fig. 7. NBTI stress on pullup and PBTI stress on pulldown during hold results in an asymmetrical cell.

5 BTI stress during normal SRAM operations

Now it is examined what BTI stress effects arise from normal SRAM operations that are namely hold, read and write.

5.1 Hold

During hold, data is kept in the feedbacked inverter-pair. During this period, PL2 experiences NBTI stress conditions (compare Figs. 1 and 3). Furthermore, the pulldown transistor on the opposite side (PD1) experiences PBTI stress conditions (compare Figs. 2 and 3). The access transistors do not see PBTI stress conditions, since they are in non-conducting state. Summing up, this means that for the complete time of data hold, one pullup and its opposite pulldown are affected by BTI (Fig. 7), and this state can last for years!

5.2 Read

In a read cycle, data is extracted from the memory cell and transferred to the bitlines via the access transistors. During this cycle, the situation is almost the same as during hold. Additionally, there might be a time when the access transistor on the "0" side experiences PBTI stress conditions, after the bitline got discharged, and the wordline is still open. But this is not regarded to be critical for the access transistor.

5.3 Write

During a write cycle, two cases must be distinguished: either the same data is written to the cell that was in memory before. Then the access transistor on the "0" side of the cell experiences PBTI stress for the cycle time, additionally to the hold stress for the pullup and pulldown. Or the cell flips because of the write, then the access transistor on the newly written "0" side only sees PBTI stress for the time after the cell has flipped. The pullup and pulldown stress are changing

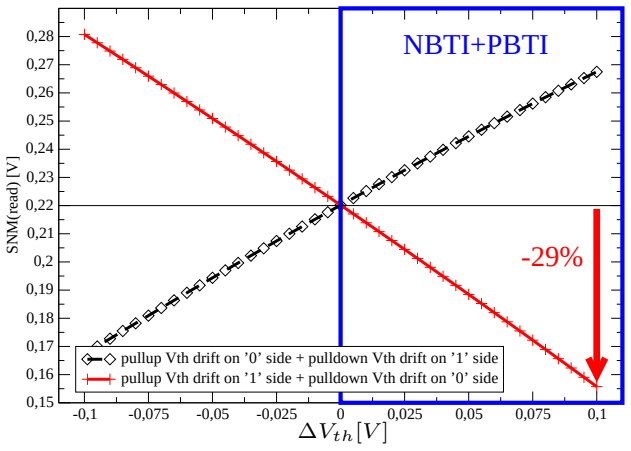

Fig. 8. Impact of threshold voltage drift of pullup- and opposite pulldown-transistor on read stability: 30% loss at ±100 mV drift.

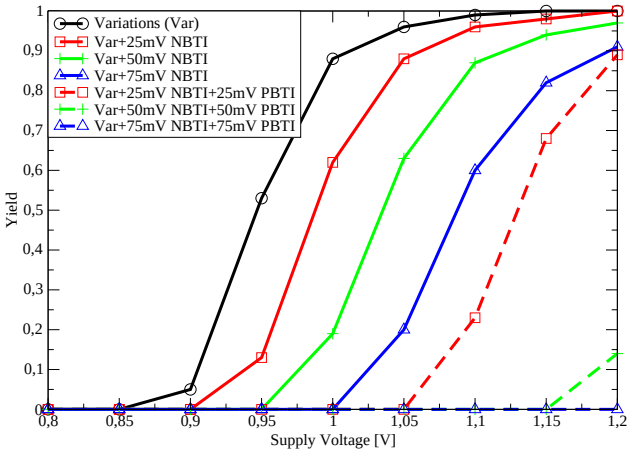

Fig. 9. Yield including global and local variations after long hold of one data with NBTI and PBTI degradation for 256 kBit cell array.

to the other pullup/pulldown pair, respectively. In summary, the write cycle also is not considered to be critical.

6 Long hold followed by direct read: the worst case BTI scenario for SRAM

The last section was pointing out: the hold state is the most critical one for BTI impact on 6T SRAM, because during the complete data hold phase, one pullup and one pulldown both experience full BTI stress conditions. It is now additionally taken into account that threshold voltage drift during or directly after stress is maximal, as there is no time for BTI annealing. The conclusion is that long hold of one data, followed by direct read, is the most critical BTI scenario: during this read, there is the biggest threat of destructive reading.

6.1 NBTI and PBTI effects are adding

Simulations have shown 10% and 20% loss of read stability for pullup/pulldown drifts, respectively. Now what happens during "hold" state, when both pullup and pulldown experience BTI stress? In Fig. 8 one can see that both impacts are adding! In other words: −100 mV pullup drift together with +100 mV pulldown drift result in almost 30% loss of read stability. This addition of the two effects can be explained with the small threshold voltage drifts relative to V_{DD}, which makes linearizing and therefore addition possible. If it is now additionally taken into account that

1. single devices can have more than 100mV V_{th} drift due to the wide BTI distribution and that
2. all devices can have more than 100mV V_{th} drift due to a direct read access without time for BTI annealing,

then it gets clear that these both effects together might result in a yield deterioration of SRAM over time.

6.2 Variations in manufacturing

One additional item was completely neglected so far: the unavoidable variations during manufacturing, which can be divided into global and local variations. While the degradation effects occur over long time of usage, the variations exist right after the production process. Global variations occur because the wafers cannot be treated exactly identically: they have slightly different doping, the mask will be slightly misaligned in the stepper etc. But modern processing technologies allow reducing these irregularities. In the scope of this work we regard a global variation according to the width of 2σ.

Local variations, however, are more severe for SRAM because of the huge number of memory cells in one array. For 1MBit (2^{20}=1 048 576 cells), the variation corresponds to approx. $5{,}2\sigma$. This is why in the scope of this work, we regard a local variation with a maximum value according to the width of 5σ.

6.3 Yield considerations

The global variations of 2σ and the local variations of 5σ described in Sect. 6.2 are now additionally applied to the 6T core cell. In some devices, the NBTI and PBTI drifts will be reduced because of the variations, i.e. the threshold voltage drifts due to variations and degradation effects will eliminate each other. But in some cells, the threshold voltage drifts will be boosted. These cells are best candidates for destructive reads, because their SNM(read) value will drop dramatically. In this yield consideration, cells with SNM(read)<5% V_{DD} are considered as failing cells.

These calculations were done with the "Worst Case Distance" algorithm (Antreich et al., 1994), which gives the same result as Monte Carlo simulations, but with less computing effort. Figure 9 shows the yield in terms of "all

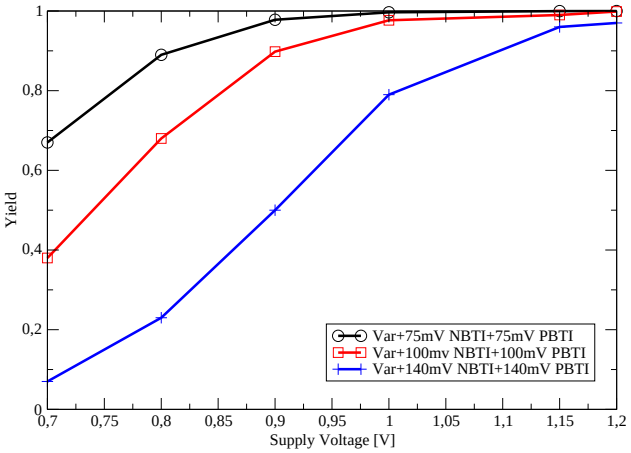

Fig. 10. Yield including global and local variations after long hold of one data with NBTI and PBTI degradation for a single Bit cell.

memory cells working in a 256 kBit array". If at least one cell in this complete array does not meet the specification, the whole array is considered as failing. One can see that lowering V_{DD} generally decreases the yield, because SNM(read) is reduced. But the main information is that variations and NBTI together do not have huge impact on SRAM. The combination of variations and NBTI plus PBTI, however, is much worse: even at $V_{DD,\mathrm{nom}}$, the yield for 25 mV BTI stress each is already below 90%. And the line for each 75 mV BTI stress does not even appear in the graph, because it is always zero! The yield in a 256 kBit array for Variations+NBTI+PBTI is so low that in Fig. 10, it is drawn for a single cell. Then the term "yield" is not the probability of all cells working in the array anymore, but the probability that this single cell fails. This can then be used to design appropriate cell circuits and redundancy schemes, so of course in realistic SRAM designs sufficient yield will still be obtained.

7 Conclusions

The impact of global and local variations and NBTI on 6T SRAM core cell are not negligible, but still do not dramatically impact the SRAM design. This is because the two pMOS pullup transistors are the only ones to be affected by NBTI. The sensitivity of the SRAM circuit to small threshold voltage drifts of these transistors is not excessive. The situation including PBTI is much worse: this effect works on the nMOS pulldown as well as the access transistors, and the sensitivity especially of the pulldown transistor is much higher: with the same threshold voltage drift, the impact on read stability is twice as high for pulldown compared to pullup devices.

Moreover, during hold state of the memory, the two effects are adding, so that the cell weakens drastically in terms of read stability. The cell loses approx. 30% for 100 mV NBTI and PBTI induced threshold voltage drift on pullup and pulldown transistor. Here is the biggest threat of undesired write during a read cycle, which is equal to data loss. BTI behavior like distribution and annealing also plays an important role, especially if a long hold is directly followed by a read cycle, because then annealing is not possible.

In future technologies including high-k materials, it is very important to consider these effects during SRAM memory design in order to be able to produce long-life memory cells.

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