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Device reliability challenges for modern semiconductor circuit design – a review

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Abstract. Product development based on highly integrated semiconductor circuits faces various challenges. To ensure the function of circuits the electrical parameters of every device must be in a specific window. This window is restricted by competing mechanisms like process variations and device degradation (Fig. 1). Degradation mechanisms like Negative Bias Temperature Instability (NBTI) or Hot Carrier Injection (HCI) lead to parameter drifts during operation adding on top of the process variations.

The safety margin between real lifetime of MOSFETs and product lifetime requirements decreases at advanced technologies. The assignment of tasks to ensure the product lifetime has to be changed for the future. Up to now technology development has the main responsibility to adjust the technology processes to achieve the required lifetime. In future, reliability can no longer be the task of technology development only. Device degradation becomes a collective challenge for semiconductor technologist, reliability experts and circuit designers. Reliability issues have to be considered in design as well to achieve reliable and competitive products. For this work, designers require support by smart software tools with built-in reliability know how. Design for reliability will be one of the key requirements for modern product designs.

An overview will be given of the physical device damage mechanisms, the operation conditions within circuits leading to stress and the impact of the corresponding device parameter degradation on the function of the circuit. Based on this understanding various approaches for Design for Reliability (DfR) will be described. The function of aging simulators will be explained and the flow of circuit-simulation will be described. Furthermore, the difference between full custom and semi custom design and therefore, the different required approaches will be discussed.

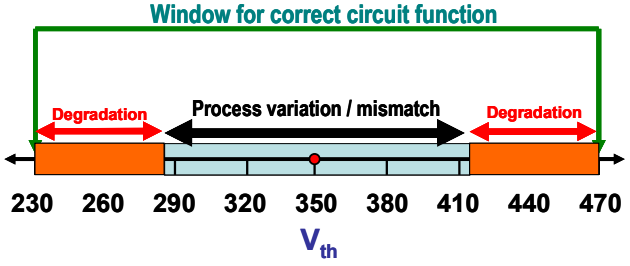

Fig. 1. Specific window for correct circuit function. In worst case process variations and parameter degradation add up.

1 Device degradation

Negative Bias Temperature Instability (NBTI) and Hot Carrier Injection (HCI, also called “hot carrier stress” → HCS) are nowadays the most critical device degradation mechanisms and became a limiting factor in scaling of modern CMOS technologies (Schlünder, 2005, 2007; Martin, 2009).

Figure 2 shows the chain of causation of circuit IC failures based on device degradation. The circuit function determines the operation points of every involved device. The operation of the transistors leading to device stress depending on the operation point and other factor like operation temperature, device geometry etc. Damage mechanisms occur leading to changes mainly of the gate oxide and adjoining parts of the transistors. These damages lead in turn to a change of the electrical behavior of the devices, which is described by electrical parameters. If this electrical parameter degradation

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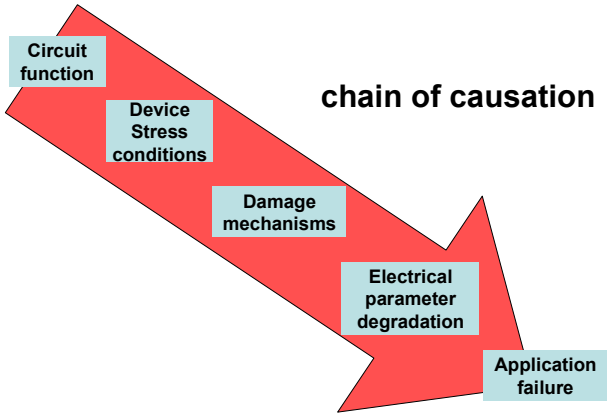

Fig. 2. Chain of causation of IC-failures.

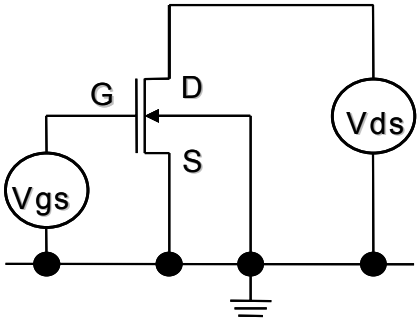

Fig. 3. Schematic Hot carrier stress condition.

leaves a circuit specific window, the circuit fails and finally the application malfunctions.

Beside the two most important degradation mechanisms NBTI and HCI, which cause transistor parameter shifts during IC operation, plasma induced damage (PID) can also contribute to MOS transistor parameter drifts. PID is a degradation of MOS devices, which occurs during processing and in fact, it can accelerate the NBTI and HCI degradation during circuit operation. PID is not discussed in this review, details can be found elsewhere (Martin, 2009). Generally, in a semiconductor manufacturing environment variations in processing conditions influence not only the parameter mismatch but also vary reliability degradation. In order to keep track of the reliability variations, very fast reliability measurements are performed on a continuous basis on productive wafers (Martin and Vollertsen, 2004).

2 Hot Carrier Stress

Hot Carrier Stress describes a degradation of the electrical parameters of MOSFETs under a dynamic stress mode (Hu et al., 1985; LaRosa et al., 1997; Thewes et al., 1999; Chen et al., 1999; Lu et al., 2004; Bravaix et al., 2009). The lateral electrical field between source and drain of a current driving transistor can lead to high energetic carriers. A part of these "hot" carriers cause impact ionization (electron hole pair generation). One carrier of the pair drains in the substrate, the other one can damage the gate oxide and adjacent spacer oxides. The schematic in Fig. 3 illustrates the stress condition for HCS. A gate-source potential drives the transistor into strong inversion, and the drain-source-voltage forms the lateral field. In a classic model lucky electrons can collect enough energy within the drift zone beyond the pinch off point to create impact ionization. The injected carriers can damage gate- and spacer-oxide at the drain side of the transistor. Therefore the device is damaged inhomogenously, the device is no longer symmetrical. Beside the drain-source voltage also the gate-source voltage has an effect on the degradation. V_{GS} affects the amount of carriers within the channel and also the energy which carriers can collect. These effects lead to a specific V_{GS} for maximal damage.

At lower V_{GS} the amount of carriers within the inversion layer is decreased. For higher gate-voltage the drift zone will be reduced and correspondingly the carriers can collect less energy. The worst case gate-source voltage for a given drain-source voltage can be determined by set of a measurements. The gate current of p-MOS devices is a measure for the amount highlights only the quantity electron hole pair generation under hot carrier stress conditions. For n-channel device the injected gate current is hard to measure (especially for thicker oxides) since the injected electrons slow down in the electric field between gate and drain node. The substrate current is measured alternatively. While the measured current highlights only the quantity of potentially injected carrier and not their energy, the worst case condition for HCS damages is at slightly lower gate voltages. Since the maximum of the substrate current curve is reasonably flat, the error is negligible.

Furthermore, HCS shows temperature dependence. At lower temperature the mean free path for the carrier is longer. They can collect higher energies. Accordingly, the worst case for HCS is at the lowest (product-) temperature. The injected carriers impact the electrical parameters of stressed devices, especially the threshold voltage and the carrier mobility (g_m). For n-MOSFETs the HCS degradation leads to an increase of the threshold voltage of and to a reduction of the carrier mobility. The drive current capability of n-MOSFETs degrades.

For the degradation of pMOSFETs we have to consider the technology node, especially the gate length and the work function formed by the material for the gate electrode. A classic buried channel p-MOS device degrades in the opposite direction to n-MOS devices. Electron trapping leads to lower threshold voltages, increased drain current and higher off-currents. For modern technologies with boron doped polysilicon gates for surface channel pMOSFETs (dual workfunction) the p-channel devices show a contrary behavior. In this case the damage is dominated by hole trapping. In general the degradation is comparable to

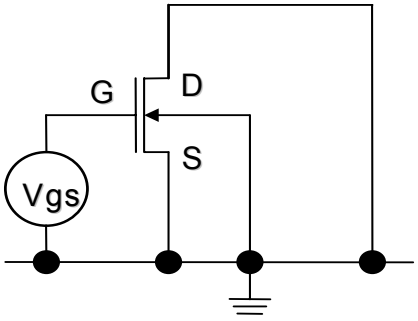

Fig. 4. Schematic NBTI stress condition.

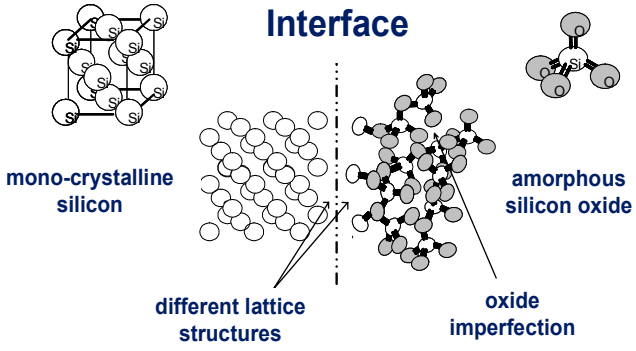

Fig. 5. Schematic of the interface region of MOSFETs. Slightly different lattice structures leads to dangling bonds satured by hydrogen. Under NBTI stress the bonds break and the dangling bonds act as interface states.

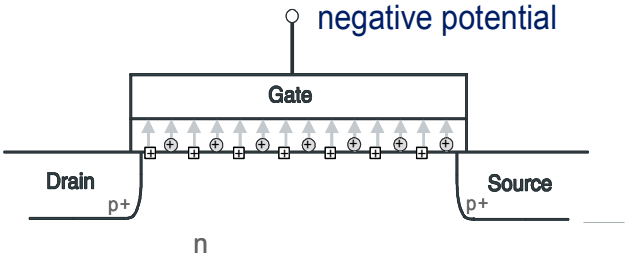

Fig. 6. Simplified cross-section of a NBTI stressed p-MOS device. Positive oxide charges and filled donor type interface states are symbolized with circles and rectangles. Trapped holes impact the electrical behavior of the device.

n-channel transistors. The threshold voltage increases and the drain current decreases. At modern dual work function technologies HCS leads to a reduction of drive current capability of the transistor independently of channel type.

Also the worst case condition for HCS differs with different technology nodes. In modern technologies (below quarter micron) the mean free path plays no longer the dominant part for the p-MOS degradation. The energy of the hot carriers and therefore, the degradation has its maximum at higher temperatures. The worst case operation point shifts to $V_{DS}=V_{GS}$. For the latest technology nodes (below 65 nm node), the worst case condition is at $V_{DS}=V_{GS}$ and higher temperature even for n-channel devices. For a lifetime assessment it has to be considered that the operation point $V_{DS}=V_{GS}=V_{DD}$ is very untypical within circuit function. Only the charge/discharge of very large capacitances can lead to operation points close to $V_{DS}=V_{GS}=V_{DD}$.

3 Negative bias temperature instability

NBTI for pMOSFETs describes the parameter degradation under a static stress mode at elevated temperature (Jeppson and Svensson, 1977; Schlünder et al., 1999; Krishnan et al., 2003; LaRosa et al., 1997). A high gate-source voltage drives the device in inversion. The carrier channel is formed, but since the drain-source voltage equals zero, no current flows in the channel region. Figure 4 illustrates the schematic for the NBTI stress condition. Due to the missing lateral field in contrast to HCS, a homogenous damage of the whole active region can be obtained. Therefore, NBTI shows only weak dependence on the geometry, based on oxide edge effects.

The high electrical field across the gate oxide in combination with an elevated temperature leads to an electrochemical reaction in the region of the interface between silicon and gate oxide. Figure 5 shows a schematic of this interface. Due to slightly different lattice structures of monocrystaline silicion and the amorphous oxide, an interface region is formed during and after gate oxide processing, which consists of only a few atomic layers and many dangling blonds. The open dangling bonds act as interface states. They can catch (channel-) carriers, trap them for a certain time and emit them back into channel. Filled interface states shift the threshold voltage and can reduce the channel carrier mobility.

During high temperature steps after gate oxide process these dangling bonds were passivated typically by hydrogen. Additional anneals under hydrogen atmosphere support this process. Such saturated bonds are no longer electrical active and do not disturb the transistor function. During negative bias temperature stress these passivated bonds break open within an electrochemical reaction.

The bonds “dangle” again and act as interface states. Filled donor type interface states counteract the charge on the gate electrode. For each trapped hole in an interface state one electron of the charge on the gate electrode is missing for controlling the channel. In other words one carrier is missing in the channel. As a result the absolute value of the threshold value increases. Additionally holes can be trapped within the oxide bulk with the same effect.

Furthermore the charged interface can reduce the carrier mobility. Figure 6 illustrates a simplified cross-section of a NBTI stressed p-MOS device. Positive oxide charges and filled donor-type interfaces are symbolized with circles and

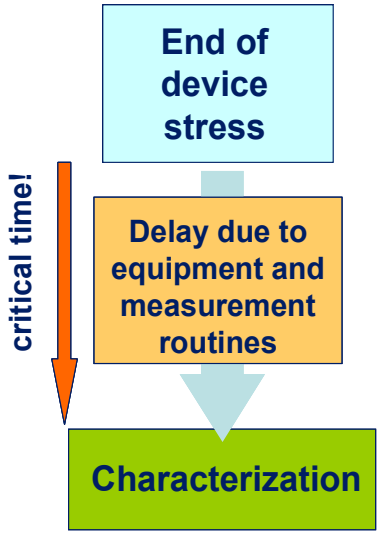

Fig. 7. Flow-chart illustrating the critical time delay between end of stress and characterization of the test-device. The NBTI degradation recovers very fast.

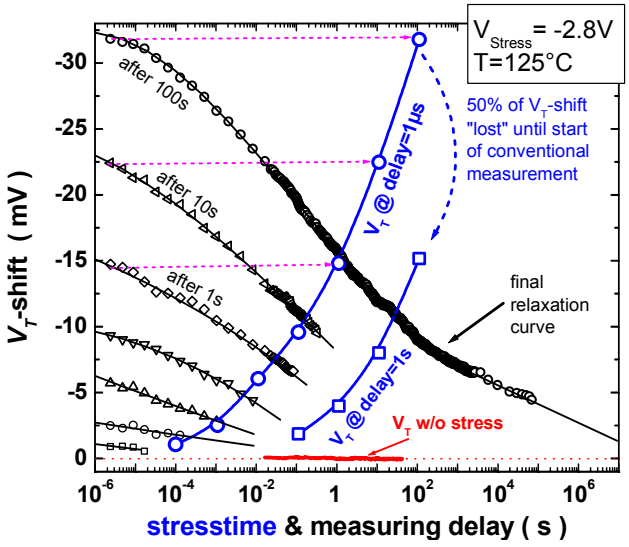

Fig. 8. Ultra fast V_{th} measurement as a function of stress- and recovery time. After 100 s stress the degraded threshold voltage recovers by 50% in the timeframe between 1 μs and 1 s after end of stress.

rectangles. NBTI has a pronounced process impact up to the passivation layer. The process for gate oxide growing and the hydrogen inventory of the entire process influence the NBTI behavior. SiON gate oxides show enhanced NBTI, but the nitrogen fraction is necessary as a diffusion barrier in the gate oxide of surface channel p-MOSFETs. The barrier prevents boron penetration from the p^+ doped poly-silicon into the channel.

The n-channel transistor of standard CMOS-technologies with SiO_2 or SiON gate oxide is almost not affected by bias temperature stress. There is no comparable electrochemical reaction between the interface and electron channel. For future CMOS technologies offering transistors with an High-K gate stack also "Positive Bias Temperature Instability" (PBTI) becomes a severe device reliability concern.

4 NBTI recovery

Beside the strong parameter degradation another phenomenon of NBTI challenges reliability assessments. The stress induced parameter degradation recovers very fast after end of stress (Rangan et al., 2003; Reisinger et al., 2006; Campbell et al., 2006; Reisinger et al., 2007a; Grasser et al., 2007; Reisinger et al., 2007b; Schlünder et al., 2007; Grasser et al., 2008). The parameter values drift back to the values before the stress. This effect has to be considered for correct parameter extraction during stress experiments. The flow-chart in Fig. 7 describes the problem: due to delays of the used measurement equipment and time demands of V_{th} extraction routines, the device is already recovered at the point-of-time of the characterization. The threshold voltage is already recovered.

In contrast to experimental measurement conditions, transistors within product circuits do not have long recovery times between stress and next operation (determined by clock frequency).

Vth extraction methods have to consider this effect. Several different methods have been introduced in the literature, each with different advantages and draw-backs (Reisinger et al., 2007b; Schlünder et al., 2007). A very fast method is introduced in Reisinger et al. (2006) and Reisinger et al. (2007a). The threshold voltage can be extracted directly within 0.5 μs after end of stress. It has to be mentioned that this cannot be achieved with today's available parameter analyzers. We recorded the data with a self-developed measurement card. Figure 8 shows recovery curves at different stress time. The threshold is measured continuously after end of stress for 11 decades of time (black symbols). A Vth measurement sequence without stress was done for verification (red line). After end of stress the electrical parameter moves backwards very fast to the values before NBTI stress.

After 100 s stress the degraded threshold voltage recovers by 50% in the timeframe between 1 μs and 1 s after end of stress (blue symbols). Neglecting the NBTI recovery phenomenon leads to falsified measurement value and inaccurate lifetime estimations. Nowadays NBTI is the most serious device degradation mechanism and a limiting factor for technology development. It is not completely understood and measures like metal gates will lead to higher electric field even at fixed gate oxide thicknesses. With PBTI an additional severe device degradation of n-MOSFETs with Hi-K gate stacks grows up.

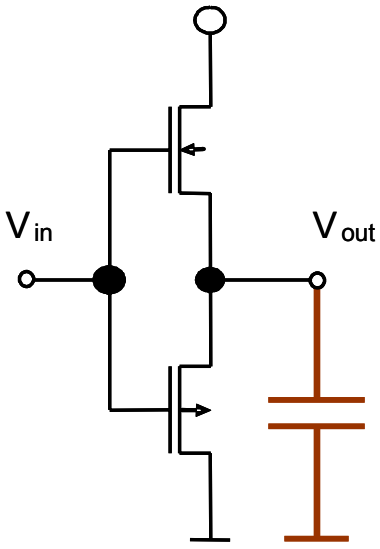

Fig. 9. CMOS inverter as a simple example for the degradation impact on circuit function. The capacitance at the output symbolizes a following stage. The inverter has to charge or discharge the gate capacitance of the next stage.

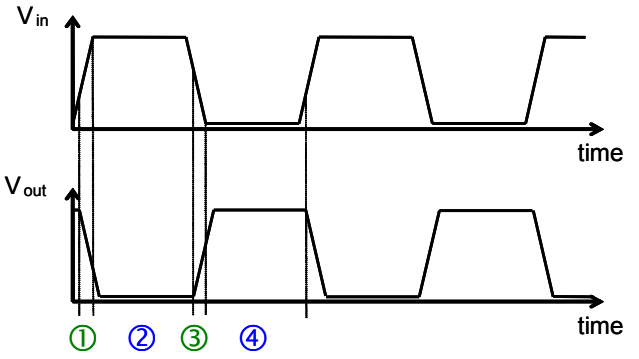

Fig. 10. Example for a chronological sequence of an input- and corresponding output-signal of an CMOS inverter (Fig. 9). Four different regions are marked with numbers describing different static and dynamic stress conditions.

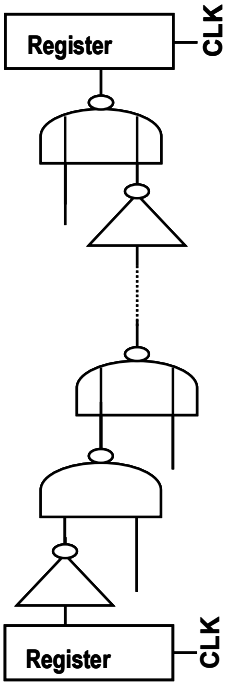

Fig. 11. Example for a logic circuit path. Due to device degradation the set up and hold time of flip-flops can change. IC-failures can occur, especially in low power application with supply voltages less than nominal.

5 Impact on circuit function

Device degradation after HCS or NBTI has an impact on circuit function. If the electrical parameter of one device leaves a specific window, a correct circuit function can not be guaranteed any more. The transistors are not necessarily destroyed (e.g. gate oxide breakdown), the degradation of the electrical behavior can lead to IC failures. In the following examples for typical analogue and digital application will be given. Furthermore a possible impact of "Low power techniques" will be introduced.

The impact of degraded electrical device parameters on digital circuits can be easily explained at an inverter as a simple basic block of digital applications.

Figure 9 shows a schematic diagram of a CMOS inverter. The capacitance at the output symbolizes a following stage. The inverter has to charge or discharge the gate capacitance of the next stage. Figure 10 plots an exemplary chronological sequence of an input- and corresponding output-signal of the CMOS inverter. Four different regions are marked with numbers describing different static and dynamic stress conditions. In region (1) the inverter has to discharge the next stage, the output signal has to be driven down to zero (better: low level). For that mainly the n-MOS device has to drive the necessary current to discharge the (gate-) capacitance of the next stage.

In this region mainly Hot Carrier Stress for this n-MOS device occurs. After finishing this job the circuit is in a static mode (region 2).

In this region no current but leakage current flows within the inverter. The n-channel device is under PBTI condition. The input signal and therefore the gate of the n-MOS is on high level, the drain-, source- and substrate contact is on low level. n-MOSFETs with SiO2 or SiON gate oxides are almost not affected, a high-K n-channel device would degrade under these PBTI conditions. Entering regions (3) the capacitance of the next stage has to be charged up to high level. For this task mainly the p-MOSFETs is required. The device has to conduct the current from V_{DD} to the capacitance. In this region mainly HCS for this p-MOS transistor occurs.

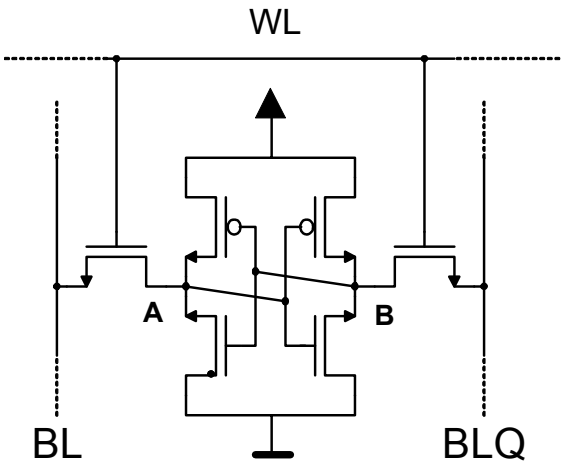

Fig. 12. Schematic diagram of a typical 6 transistor SRAM cell. The stress conditions and the impact of degradation can be transferred from a single inverter.

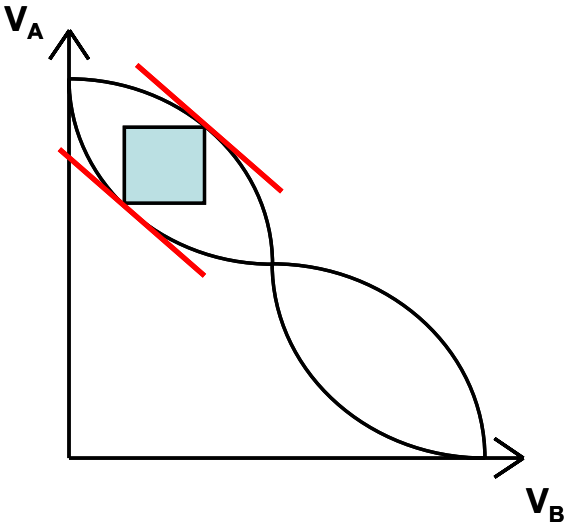

Fig. 13. Buttefly-diagram of a SRAM cell. The two inverter curves determine the form. The area of the turquoise square is a measure fo the cell stability.

Region (4) defines again a static stress mode. In this case the p-MOSFET of the inverter is loaded by NBTI stress. The gate electrode is on low level, all other terminals are on high level (V_{DD}). An elevated temperature accelerating NBTI can originate from the environment or from the circuits itself.

The induced degradations of the electrical device parameter impact the function of the inverter. First of all a reduction of the current drive capability of this stage occurs. Furthermore the switching thresholds of the inverter shifts and the duty cycle (high level to low level ratio) changes (Reddy et al., 2002). This changed behavior of one circuit block influences the entire circuit.

In Fig. 11, a part of a logic path is pictured. The degradation of the different elements leads to longer signal rise times. As a result the time delay for loading the next stage (propagation delay) is increased. The set-up and hold time of flip-flops changes. Furthermore the degradation impacts the speed and noise immunity. This is critical especially at supply voltages less than nominal (low power applications).

A SRAM cell is another typical basic block of digital circuits and can be used as another good example for circuit degradation. Figure 12 shows the schematic diagram for a typical 6 transistor SRAM cell.

Since the function is based on two cross-coupled inverters, both the stress conditions of the device and the impact of degradation on the circuit can be transferred from a single inverter. Read and write operations are dynamic modes and lead accordingly to HCS. All the remaining period the SRAM cell is in static mode, corresponding in NBTI (and PBTI).

Dependent of the data the cell has to store (1 or 0), the p-MOS transistor of the left or of the right inverter is under NBTI stress. Since this static mode typically occurs for biggest part of the lifetime, it becomes clear that degradation in static mode and accordingly NBTI is the most severe reliability concern. The NBTI degradation of the p-channel devices within SRAM cells leads mainly to a decrease of the stability of the cell (LaRosa et al., 2006).

Figure 13 shows a "Butterfly-diagram" of a 6T-SRAM cell. The two inverter curves determine its shape. These diagrams are used to describe the stability of the cell. The area of the turquoise square is a measure for this parameter. A degradation of the two inverters has an impact on β- and n-/p-MOS ratio of the SRAM-cell. The static noise margin and dynamic read stability decrease. The cell shows an increased sensitivity against Soft Error Rate (SER), supply voltage drops, noise, etc. Furthermore an increase of access time is possible.

6 Transistor reliability under analogue operation

Reliability evaluation of MOS transistors under analog operation requires a specifically adapted approach. The operating points and thus the stress conditions significantly differ. Different device parameters must be considered in the circuit design process (Chung et al., 1990; Thewes et al., 1999, 2001; Schlünder et al., 2003; Chaparala et al., 2003; Schlünder et al., 2005).

Figure 14 illustrates the background for the different impact of device degradation on analogue and mixed signal applications. The diagram plots the relative degradation of the input characteristic of a MOSFET as a function of operation gate voltage and stress time. Typical NBTI degradation behavior can be obtained with strongest drift close to the threshold voltage and weaker drift with increasing gate voltages.

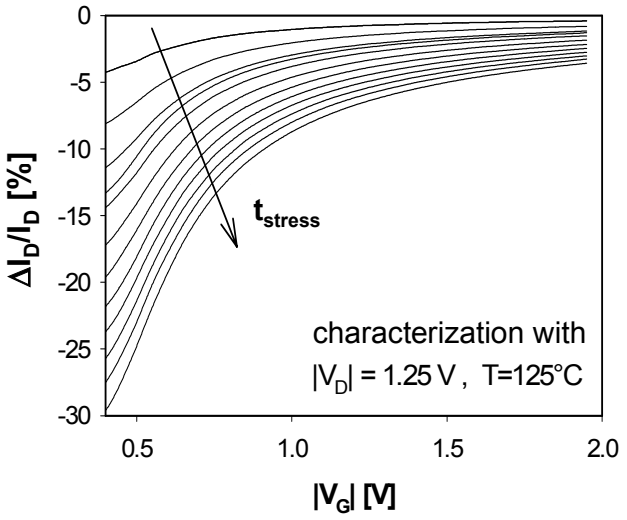

Fig. 14. Relative degradation of the input characteristic of a MOSFET as a function of operation gate voltage and stress time. Strong degradation for operation points with small gate voltages and a weaker impact on operation with high gate voltages can be obtained.

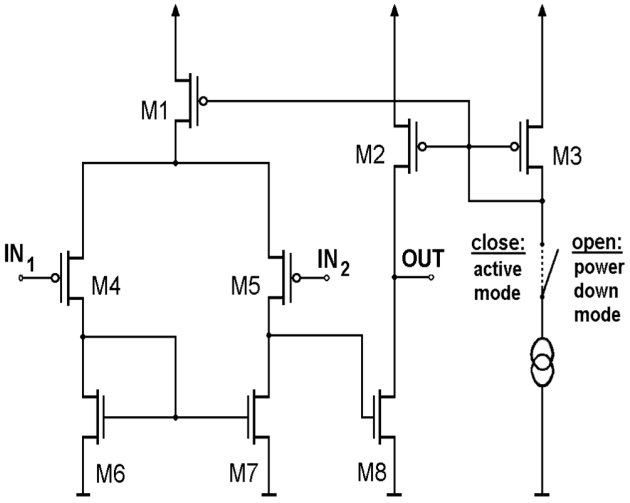

Fig. 15. Two stage operational amplifier/comparator. The switch drives the circuit in active or power down mode. During active mode HCS and inhomogenous NBTI can occur. However the worst case is the power down mode, where the input devices are exposed to NBTI with full V_{DD}.

Since for many analog applications the effective gate-to-source voltage is in the order of a few 100 mV, the impact of device degradation is much stronger for circuits of analogue or mixed signal applications. In those circuits the operation point relies on the accurate matching of paired transistors.

Figure 15 shows the schematic diagram for a two stage operational amplifier/comparator. Here the correct circuit function relies on the accurate matching of the input devices (M4 and M5). In the power-down mode, the bias current is switched off to avoid power consumption of the inactive circuit, but the supply voltages are not driven down in order to allow fast reactivation of the circuit without switching of the supply lines. The potentials of the internal nodes of the circuit are then determined by the subthreshold characteristics of the devices, leakage paths, and by the signals applied to the inputs. In our example, the connection between drain and gate of M3 and between drain and gate of M6 leads to low gate-to-bulk/well voltages of the transistors connected to the gates of M3 and M6 (M1, M2, M3, M6, and M7), so that these devices are not prone to high oxide fields.

However, high values of gate-to-channel or gate-to-bulk/well voltage can occur in the case of M4, M5, and M8 according to the values of the subthreshold currents of M1, M6, and M7 and possible further leakage paths. If in addition high temperature is applied to the circuit (e.g. provided by the environment) NBTI conditions can occur. To evaluate the effect of NBTI applied to the input devices M4 and M5 under active mode operation conditions, we must consider that a defined (fixed) current is forced through these transistors by current source transistor M1.

Therefore, M4 and M5 are operated with approximately the same drain current before and after stress. Thus the device degradation must be compensated by an increase of the absolute value of the gate-to-source voltage. Asymmetric operation of the input branches of the circuit in Fig. 15 or asymmetric degradation of the input devices under symmetrical stress conditions thus leads to a stress-induced offset voltage of the circuit which equals the difference of the stress-induced threshold voltage degradations of the input devices.

7 Low Power Techniques

In the following Low Power Techniques and their possible impact on device reliability is discussed. LP techniques are used in circuits for modern portable applications like PDAs, mobile phones, etc. to increase the standby time with accumulators. Furthermore Low Power is also used in high performance application to reduce power dissipation and accordlingly the demand for cooling (CPUs/GPUs)

Low power systems/circuit designs can affect the reliability of the integrated circuits. One typical example for these techniques are systems with “Sleep Transistors”. Figure 16 helps to understand this approach. The schematic shows a block diagram of a test chip with several Low Power Techniques assembled together to evaluate the behavior of the different techniques. We focus here on the “Sleep Transistor” approach which is based on leakage power control.

A p-MOS connects the external VCC to supply rails (Virtual VCC), or an nMOS connects the external ground VSS to the ground rail (Virtual VSS). These sleep transistors are distributed throughout the layout. The area overhead is about

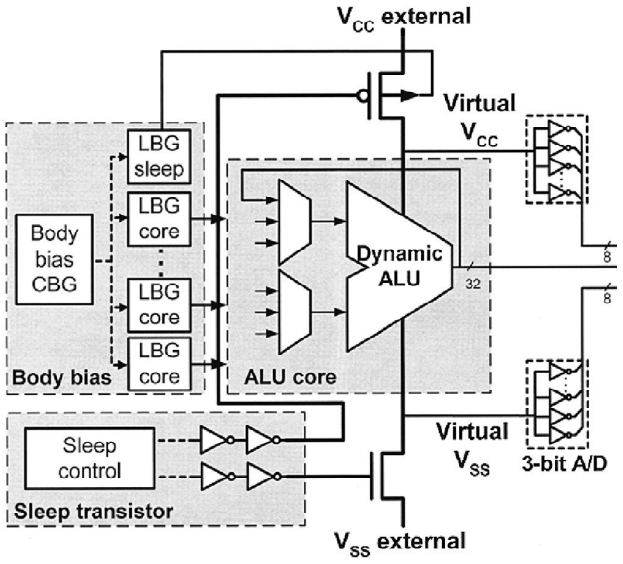

Fig. 16. Block diagram of a test chip for different Low Power Techniques. We focus the sleep transistor approach, which reduces power consumption by switching off complete circuit blocks from power supply. But Low Power techniques can also impact the circuit reliability.

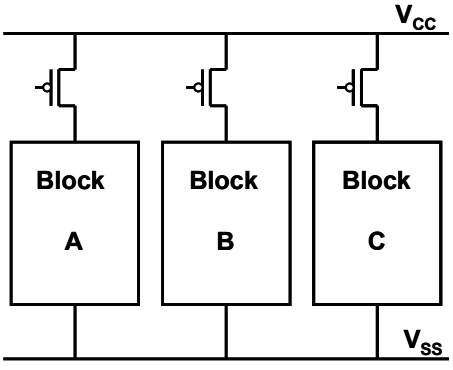

Fig. 17. Sketched block diagram of the Sleep Transistor Low Power Technique. When idle mode is entered the sleep transistors turned off and VCC are no longer connected to external VCC. Whereas idle blocks dissipate no power other circuit blocks are still working without restrictions.

3%–6%. A control block switches the sleep transistors and watches clock.

When idle mode is entered the sleep transistors turned off and VCC are no longer connected to external VCC. Whereas idle blocks dissipate no power other circuit blocks are still working without restrictions. This can impact the circuit reliability of whole system. The operation times of different blocks varies, this leads to various stages of parameter degradation. The propagation delay within the different can vary, due to different operation (stress) time. This can have an impact on timing between the different circuit blocks. On the other hand degraded circuit blocks get the opportunity for parameter recovery as already discussed in the NBTI recovery chapter.

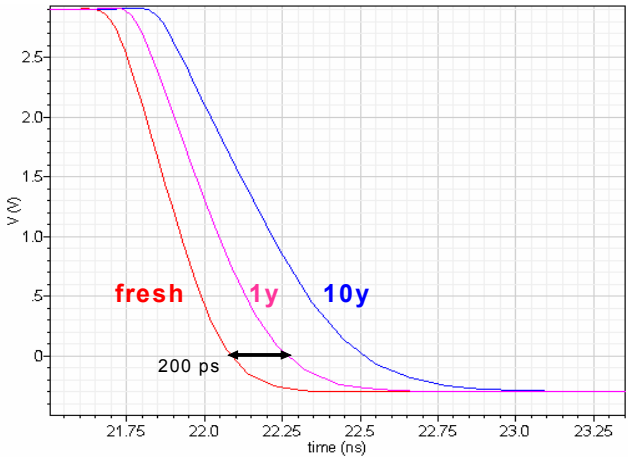

Fig. 18. Example for a output signal of a example circuit by an aging simulator. The output signal can be plotted and compared before and after given operation times.

8 Approaches for design for reliability

In the following the function of Aging Simulators will be briefly introduced. The typical flow of circuit simulation will be discussed and a simple example for circuit design optimization will be given. Furthermore constraints for semi-custom design will be evaluated.

Since process evolution will lead to higher device stress and reliability safety margins decrease in modern technologies, circuit reliability is not longer a task only for technology development but also for circuit designers.

For this work the designers have to be supported by smart software tools with built-in reliability know how. Already available are aging simulators for full-custom design. These tools are reasonable for relatively low numbers of transistors (analog/RF circuits). The circuit simulators with built-in reliability can simulate entire circuit blocks. The parameter degradation can be calculated individually for each device. The circuit designer can adjust the characteristic of each device (e.g. geometry, type).

Afterwards the circuit can be simulated again and in iteration reliable solutions can be found. Figure 18 shows an example for a circuit simulation with an aging circuit software tool. The output signal can be plotted after a given operation time. The designer can check whether the results achieve the requirements.

The goal of circuit aging simulators is to describe the change of the transistor model (e.g. BSIM) due to device degradation as a function of age. The information of the deviation of a parameter as function of age is required [ΔBSIM-Par=f(age)]. Different degradation effects have to

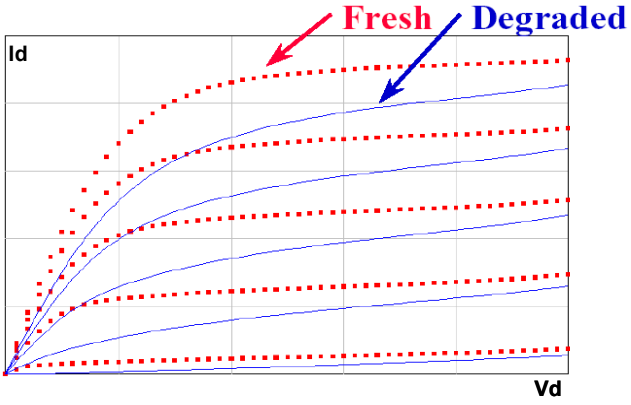

Fig. 19. Output characteristic of a MOS transistor before and after stress. An aging simulator simulate this degradation for every device in a circuit.

be taken into account (typically HCS and NBTI). In Fig. 19 an output characteristic of a virgin device is compared with simulated degraded device.

Figure 20 shows the sketched simulation flow. The reliability simulation has to be integrated in the design flow. Based on a large number of stress experiments with various stress- and characterization operation points degradation models can be fitted to the real degradation behavior of the device of the used technology.

The virgin circuit can be simulated based on standard device parameters (e.g. BSIM). Besides the simulation of the circuit function without stress, the tool extracts the duty cycle for each device within the circuit. A suitable input pattern stimulates the circuit function and all different operation points during operation are integrated by the simulator. In this manner the tool collects the aging of each device. Based on the fitted degradation model the aging simulator creates a new model card for each device. After this step a new flat netlist with individual degraded model cards or subcircuit substituions is available.

This netlist describes the circuit after stress. A new simulation of this aged circuit can be done and can be compared with the first simulation of the fresh circuits. The designer can check if the result achieve the requirement and can improve the circuit if necessary.

Figure 21 shows an example for Design for Reliability (Thewes et al., 2001). The gates of the critical input devices M4/M5 of the already discussed operational amplifier (chapter 6) are connected to V_{DD} via additional transistors M14/M15. The gate and all other terminals are pulled to the same potential. Thus high electrical gate oxide fields during power down mode are avoided. No NBTI stress occurs, the device parameters do not degrade. The necessary enable signal is already available to select the power down mode. Since the additional devices have to balance only leakage currents, the inserted devices lead to an only small additional area demand.

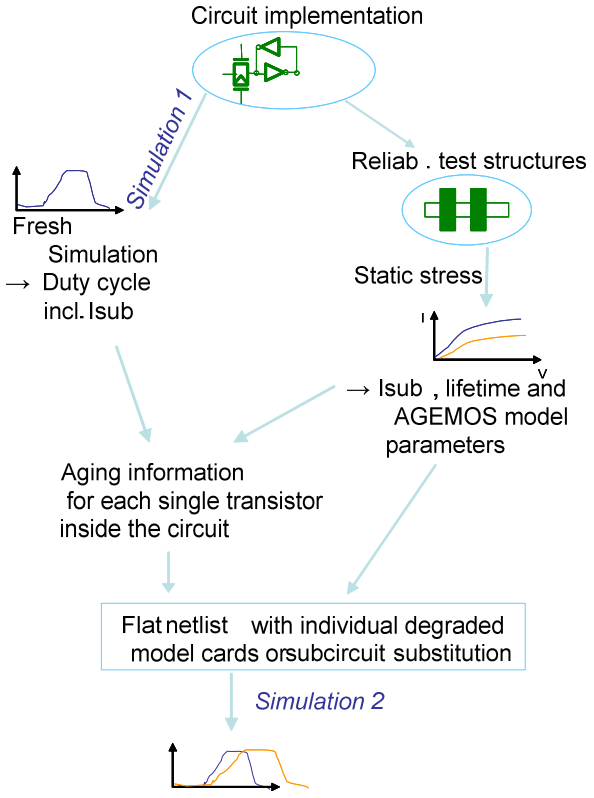

Fig. 20. Circuit simulation flow. The reliability simulation has to be integrated in the design flow.

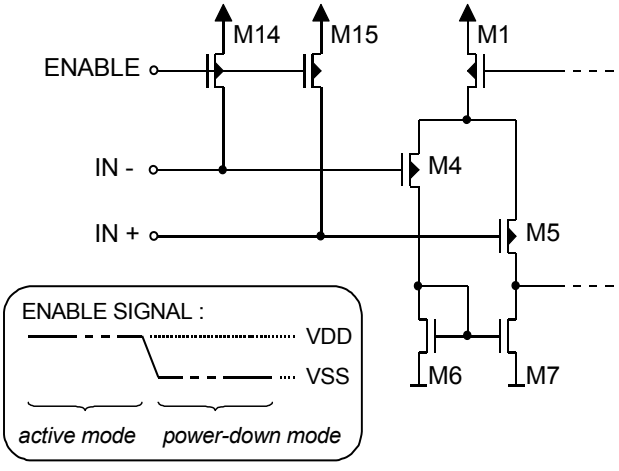

Fig. 21. Example for Design for Reliability: the critical input transistors M4 and M5 are protected against NBTI stress during the "Power Down Mode".

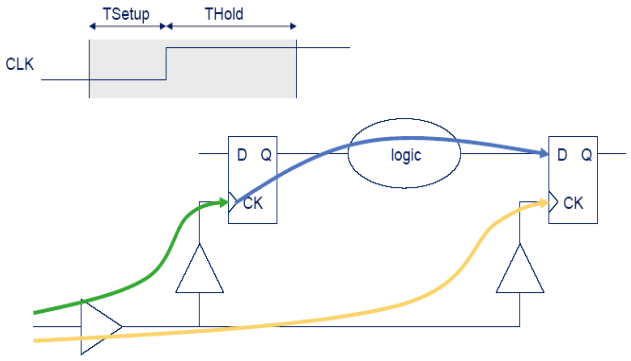

Fig. 22. Critical time path of a semi-custom design (e.g. base band chip). Since the designers do not have a direct access to single devices within the design tool, a smart approach is necessary to implement reliability checks into the design flow.

9 Constraints for semi-custom design

For digital application a more automated design approach is used. The library elements are placed automatically by the design tool. The designers do not know in advance where a single element is placed. They have no direct access to the single devices. Therefore automated design environments make it difficult to manually determine reasonable operation conditions for single library elements.

A single library element is used in many different subcircuits, and within, exposed to a lot of different applications/operation conditions. For all of these combinations a delay-calculation would be necessary, since digital design is delay driven. Therefore, in semi-custom design a completely different approach is necessary. A possible consideration of reliability in semi-custom designs is the calculation of parameter degradation as a part of on-chip-variations. Stress induced parameter variation can be transformed in propagation-delays (Pompl et al., 2006).

Smart software tools can check time paths within the product. In the case of time conflicts, gates can be replaced by faster ones. On the other hand the tools have to take area demand and power consumption into account.

The tool can select one of several different versions of gates with the same function (e.g. XOR). The tool decision for substitution is based on

- performance requirements
- stability against process variations
- stability against degradation
- area demand
- power consumption

The different demands have to be weighted. This is very difficult for the tool and therefore a key factor of the software tool. After replacement of gates the simulator checks the critical time paths again. If necessary further gate will be replaced until every degradation induced time conflict is solved.

10 Summary

This paper gives an overview of device degradation challenges of semiconductor circuit design. The most critical device degradation mechanisms NBTI and HCS were described. Furthermore critical device stress conditions in circuits of digital/mixed signal applications and low power techniques were highlighted.

Since process evolution will lead to higher device stress and reliability safety margins decrease in modern technologies, circuit reliability is not longer a task only for technology development but also for circuit designers. It is a common challenge. Aging/reliability simulators can help to optimize the circuits and save costs. The designer can consider reliability aspects early in the design phase and can develop reliable and competitive products.

The different requirements and constraints of “Design for Reliability” for full custom and semi-custom design were pointed out. For full-custom design capable aging simulators are already available. The function and integration into the design were briefly discussed. For semi-custom design a different approach is required. By transferring device degradation into a shift of the propagation delay of basic gate elements “Design for Reliability” can be integrated into semi-custom design flows. Smart software tools can check time critical paths after simulated aging and ensures the circuit function for the entire required lifetime.

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