Adv. Radio Sci., 7, 219–223, 2009
www.adv-radio-sci.net/7/219/2009/
© Author(s) 2009. This work is distributed under
the Creative Commons Attribution 3.0 License.

Advances in Radio Science

A novel technique for CAD-optimization of analog circuits with bipolar transistors

B. Dimov, V. Boos, T. Reich, Ch. Lang, E. Hennig, and R. Sommer

Institut für Mikroelektronik- und Mechatronik-Systeme gGmbH, Ilmenau, Germany

Abstract. In this paper, a novel approach for robust automatic optimization of analog circuits with bipolar transistors is presented. It includes additional formal parameters into the device model cards, which sweep the model parameters smoothly between the different device types. In this way, not only the sizing, but also the choice of the device type is committed to the optimization tool, thus improving the efficiency of the design process significantly.

1 Introduction

Very important step in the design of analog integrated circuits is the choice of the device types. The latter is a typical problem especially by the design of BiCMOS circuits. There, the bipolar transistors should be selected among several device types offered by the fabrication foundry, which have only few (or even no) adjustable parameters (X-FAB AG, 2008). In this way, the circuit performance depends strongly on the initial choice of the device types, which is done by the designer and is based mainly on his experience and basic engineering considerations. Once this choice has been made, a subsequent CAD-based circuit optimization is strongly restricted by the insufficient number of remaining adjustable device parameters.

Up to now, few approaches for optimization of the device types exist and are mostly based on discrete optimization methods (e.g. Cadence Design Systems, 2008). Here, we present a novel approach for automatic selection of device types using a gradient-based optimizer. Its general idea is described in Sect. 2 of this paper, with some important remarks about its applicability pointed out in Sect. 3. In Sect. 4, the optimization process of an integrated BiCMOS buffer amplifier with moderate complexity is described, thus demonstrating the efficiency of the proposed approach. Section 5 concludes the paper.

Correspondence to: B. Dimov
(boyko.dimov@imms.de)

2 General description of the new approach

A typical analog circuit optimization tool can be represented with the 3-level structure shown in Fig. 1. The optimization goal is to find the global minimum of the objective function OBJ($\boldsymbol{Q}$), with $\boldsymbol{Q}$=(q_1, …, q_n) – the vector of the circuit performances under optimization. At each iteration step, a set of design parameters $\boldsymbol{P}$=(p_1, …, p_m) is generated by the optimizer. The corresponding equivalent electrical circuit is composed and simulated with a SPICE-like electrical simulator, and the resulting performance vector $\boldsymbol{Q}$ is obtained. For this, electrical device models are used with model parameters $\boldsymbol{R}$=(r_1, …, r_k) specified by the fabrication foundry, i.e. $\boldsymbol{Q}$=$\boldsymbol{Q}$($\boldsymbol{P}$,$\boldsymbol{R}$).

The efficiency of the design process can be improved significantly, if not only the sizing, but also the choice of the type of the devices is performed automatically by the optimization tool. For this, additional design parameters $\boldsymbol{S}$=(s_1, …, s_l) should be incorporated, which switch between the different device model cards. The latter is schematically shown in Fig. 2. A drawback of this approach is the abrupt change of the corresponding circuit performances $\boldsymbol{Q}$, which results from the discrete change of the device type. The latter is hardly compatible with any gradient-based optimization techniques, thus prohibiting the utilization of their great fastness.

In order to facilitate the application of gradient-based algorithms, a smooth transition of the circuit performances $\boldsymbol{Q}$ across the whole range of available device types should be ensured. We do this by incorporating the additional design parameters $\boldsymbol{S}$ directly into the device model cards. They are used to map the model cards of the available device

Published by Copernicus Publications on behalf of the URSI Landesausschuss in der Bundesrepublik Deutschland e.V.

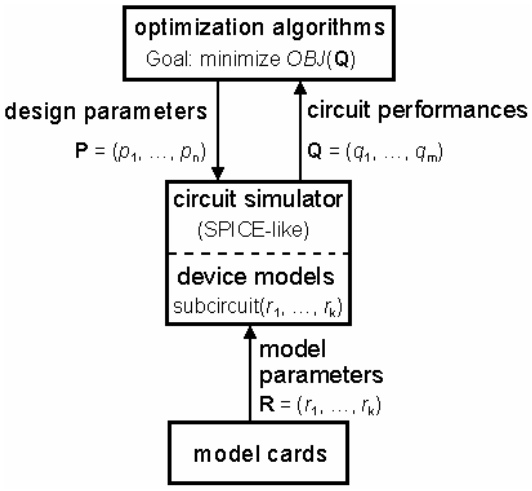

Fig. 1. Typical structure of analog circuit optimization tool.

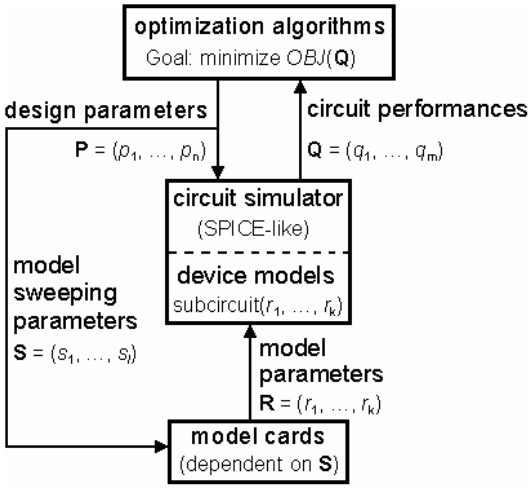

Fig. 2. Modified structure of analog circuit optimization tool permitting automatic selection of the device types.

types into a single model card with redefined model parameters $\boldsymbol{R}$:$\boldsymbol{R}(\boldsymbol{S})$=($r_1(\boldsymbol{S})$, …, $r_k(\boldsymbol{S})$). This is schematically shown in Fig. 3, where the model cards of two PNP bipolar transistor types *pnp1* and *pnp2* are mapped into the single model card *pnp12*. In this example, the devices are modeled within the *S*PICE *G*ummel-*P*oon (SGP) model (Gummel and Poon, 1970; Berkner, 2002). Only k=3 model card parameters are considered: $\boldsymbol{R}$:={BF, VAF, IS}, with BF, VAF, and IS being the forward current gain, the forward Early voltage, and the saturation current model parameters. One additional parameters s is used to map the *pnp1* and *pnp2* model cards: $\boldsymbol{S}$:={s}. As also shown in Fig. 3, this mapping is assumed to be: $pnp12|_{s=0} \leftrightarrow pnp1$; $pnp12|_{s=1} \leftrightarrow pnp2$, i.e. $r_1(0)$=`bf1`, $r_2(0)$=`vaf1`, $r_3(0)$=`is1`, $r_1(1)$=`bf2`, $r_2(1)$=`vaf2`, $r_3(1)$=`is2`.

```
model  pnp1  bjt type=pnp struct=lateral
+ BF=bf1     VAF=vaf1     IS=is1

model  pnp2  bjt type=pnp struct=lateral
+ BF=bf2     VAF=vaf2     IS=is2

model  pnp12 bjt type=pnp struct=lateral
+ BF=r1(s)   VAF=r2(s)    IS=r3(s)
```

Fig. 3. Bipolar transistor types `pnp1` and `pnp2` merged into the single model card `pnp12`.

If the functions $r_1(\boldsymbol{S})$, …, $r_k(\boldsymbol{S})$ are continuous, they sweep the circuit performances also continuously through the model cards of all available device types:

$$\boldsymbol{Q} = \boldsymbol{Q}(\boldsymbol{P}, \boldsymbol{R}(\boldsymbol{S})). \quad (1)$$

In this way, the automatic choice of the device type can be supported also by deterministic optimization algorithms, thus increasing significantly the efficiency of the optimization process. However, the following requirements should also be fulfilled:

– the sequence, in which the device types are swept, should be chosen with respect to minimize the number of the local extrema of the circuit performances, i.e. $\boldsymbol{S}$ should sweep the circuit performances q_1, …, q_n as monotonic as possible.

– because the sweeping functions $r_1(\boldsymbol{S})$, …, $r_k(\boldsymbol{S})$ are continuous, nonphysical interim values of the model parameters $\boldsymbol{R}(\boldsymbol{S})$ (and thus also of the circuit performances $\boldsymbol{Q}(\boldsymbol{P},\boldsymbol{R}(\boldsymbol{S}))$) cannot be avoided, however their evaluation as optimum ones should be suppressed somehow.

– the number l of the model sweeping parameters s_1, …, s_l should be kept as low as possible, because it directly increases the total order of the optimization problem.

Below, a possible strategy to fulfill these requirements is described.

3 Implementation of the new approach

3.1 Optimal arrangement of the device types

Although there is no full equivalence between the total circuit performance and the performances of the circuit's devices alone, they are usually strongly correlated. Utilizing this correlation, the devices are sorted with respect to their figures-of-merit, which have to be swept with $\boldsymbol{S}$ as monotonic as possible. Ideally, this sorting requirement should be fulfilled about *all* device's figures-of-merit, but this is possible only in case of device models with few model parameters and figures-of-merit (e.g. resistors and capacitors). The

optimal choice of the type of such devices is usually a trivial task; the real challenge is met with the complex device models (e.g. transistors) having many and often weak correlated figures-of-merit. In this case, a simultaneous monotonic sweeping of *all* figures-of-merit is not possible, but the designer should ensure it for those figures-of-merit *dominating* the device performance within the particular application. As a typical example for this, the sorting of amplifier's transistors can be considered. The matching of the transistors in case of differential amplification is essential for the circuit functionality. Therefore, the designer should include it within the dominating sorting criteria, contrary to the case of nondifferential amplification.

This arrangement can be performed dynamically also about devices with equal models within one and the same analog circuit. Considering again amplifier's transistors, the dominant figures-of-merit for input-stage ones are usually the generated noise and the transit frequency. However, they are less important about output-stage transistors, whose high-current performance is more dominant. Therefore, the device types of the input and output transistors can be sorted (and correspondingly swept with $\boldsymbol{S}$) in different ways, although the devices have identical models and thus share one and the same set of possible device types.

It should be pointed out, that the device type arrangement described above is performed before the circuit's optimization, i.e. at an early design stage, when even the *dc* operating point may be unknown. Therefore, the devices' figures-of-merit should be calculated out of the context of the particular analog circuit. Being dynamically dependent on both the circuit functionality in general and the device's specific function within the circuit, the device types arrangement should be usually performed multiple times during the circuit's design phase. Therefore, an efficient approach for automatic evaluation of the devices' figures-of-merit should be implemented in the optimization strategy.

One very promising candidate for this is the direct analytic approach described in Dimov et al. (2008). It is based on explicit analytic formulas calculating the device's figures-of-merit directly from its model card. Such estimation requires no electrical simulations or similar numerical calculation techniques, thus being extremely robust and fast. The formulas proposed in Dimov et al. (2008) can be easily implemented in self-written hand calculators or conventional computation tools such as Wolfram Research (2008). In this way, the device's figures-of-merit are evaluated immediately, and the device type arrangement is performed with negligible computation efforts.

3.2 Choice of the sweeping functions $\boldsymbol{R}(\boldsymbol{S})$

As pointed out in Sect. 2 of the paper, the main advantage of the proposed novel approach is its compatibility with gradient-based optimization algorithms. The gradient calculations are done numerically using finite differences (Graeb, 2007). About the optimization problem considered in this paper, the latter can be expressed using Eq. (1):

$$\operatorname{grad}\left(\mathrm{OBJ}\left(\boldsymbol{Q}\left(\boldsymbol{P}^n,\boldsymbol{R}\left(\boldsymbol{S}^n\right)\right)\right)\right) \rightharpoonup \frac{\mathrm{OBJ}\left(\boldsymbol{Q}\left(\boldsymbol{P}^n+\Delta\boldsymbol{P}^n,\boldsymbol{R}\left(\boldsymbol{S}^n+\Delta\boldsymbol{S}^n\right)\right)\right)-\mathrm{OBJ}\left(\boldsymbol{Q}\left(\boldsymbol{P}^n,\boldsymbol{R}\left(\boldsymbol{S}^n\right)\right)\right)}{\left|\left(\Delta\boldsymbol{P}^n,\,\Delta\boldsymbol{S}^n\right)\right|}$$

with superscript n representing the n^{th} optimization iteration. Despite of the particular optimization strategies implemented into the gradient-based algorithm, the decision about the next design parameter set ($\boldsymbol{P}^{n+1}$, $\boldsymbol{S}^{n+1}$) as well as the next numeric step ($\Delta\boldsymbol{P}^{n+1}$,$\Delta\boldsymbol{S}^{n+1}$) is derived always from the gradient(s) of the objective function calculated at the current (and optionally: previous) design parameter set(s) (Graeb, 2007). Therefore, the sweeping functions $\boldsymbol{R}(\boldsymbol{S})$ should be not only continuous and thus numerically differentiable, but their gradients calculated at nonphysical interim values of the device model parameters should always push the optimization algorithm towards feasible model parameter values.

This requirement is successfully met, if piece-wise linear sweeping functions are used. About the simple example described with Fig. 3, the sweeping functions have to be defined as:

$$r_1(s) = (\mathtt{bf2} - \mathtt{bf1})s + \mathtt{bf1}$$
$$r_2(s) = (\mathtt{vaf2} - \mathtt{vaf1})s + \mathtt{vaf1}$$
$$r_3(s) = (\mathtt{is2} - -\mathtt{is1})s + \mathtt{is1}$$

3.3 Minimizing the number l of the sweeping parameters

Being incorporated into the device model cards, the model sweeping parameters $s_1, \ldots, s_l$ appear as additional instance parameters of the devices under optimization. Let assume, that $i \leq l$ sweeping parameters are used to sweep the model card parameters of j uncorrelated devices from one and the same type. The latter results in $i \times j$ additional uncorrelated optimization parameters, i.e. the total order of the optimization problem increases rapidly with i. Therefore, the number of the sweeping parameters should be kept as low as possible.

A powerful way for this is the multiple reusing of already existing instance parameters. This idea will be illustrated about two types of bipolar transistors – QNA and QNB, which have to be merged in a common model card QNAB without increasing the number of optimized parameters. Let QNA be a scalable transistor with instance parameter EA=1...10 corresponding to emitter areas $1 \ldots 10\,\mu\mathrm{m}^2$, respectively. Then, its model card parameters are functions of EA, which will be designated as $\boldsymbol{R}^{\mathrm{QNA}}(EA)$. Let QNB be a transistor with fixed layout and emitter area of $1\,\mu\mathrm{m}^2$, i.e. having no instance parameters. Its model card parameters will be designated as $\boldsymbol{R}^{\mathrm{QNB}}$. A possible definition of the model card parameters $\boldsymbol{R}^{\mathrm{QNAB}}(s)$ is:

$$0.5 \leq s < 1 : \boldsymbol{R}^{\mathrm{QNAB}}(s) := 2(\boldsymbol{R}^{\mathrm{QNA}}(1) - \boldsymbol{R}^{\mathrm{QNB}})s + (2\boldsymbol{R}^{\mathrm{QNB}} - \boldsymbol{R}^{\mathrm{QNA}}(1))$$
$$1 \leq s \leq 10 : \boldsymbol{R}^{\mathrm{QNAB}}(s) := \boldsymbol{R}^{\mathrm{QNA}}(EA \rightarrow s),$$

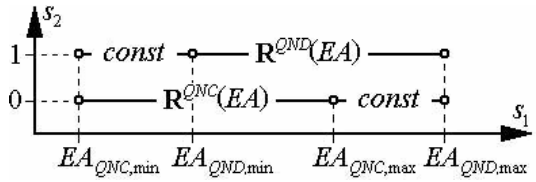

Fig. 4. Arrangement in case of different feasible ranges of the instance parameters.

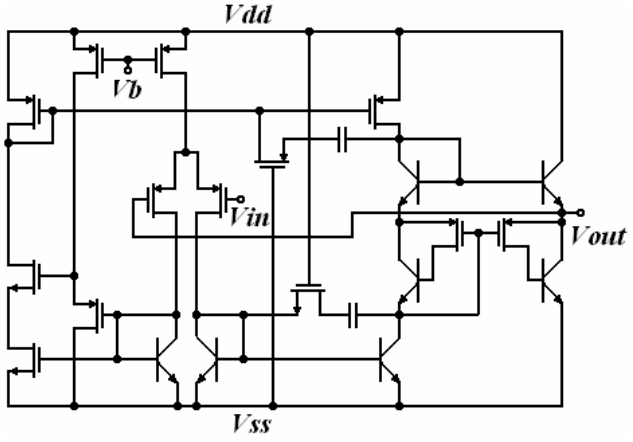

Fig. 5. BiCMOS integrated buffer amplifier under optimization (topology from Furth and Andreou, 1993).

i.e. the single sweeping parameter s incorporated into the model card of QNAB is used both to sweep linearly between QNB and QNA and to model the emitter area of QNA, thus replacing the instance parameter *EA*.

Note, that the proposed arrangement and the resulting sweeping functions $\boldsymbol{R}^{\mathrm{QNAB}}(s)$ should fulfill all sorting preconditions described in Sects. 3.1 and 3.2. Otherwise, local minima of the objective function OBJ($\boldsymbol{Q}$) can appear for interim values of s between 0.5 and 1 pointing to nonexistent type of the QNAB device.

Another typical problem is the arrangement of devices with identical instance parameters, but different feasible ranges of the latter. Considering again two bipolar transistor types QNC and QND, let both have variable emitter area *EA*, i.e. model card parameters being functions of *EA*: $\boldsymbol{R}^{\mathrm{QNC}}(EA)$ and $\boldsymbol{R}^{\mathrm{QND}}(EA)$, respectively. Let $EA_{\mathrm{QNC,min}} \leq EA \leq EA_{\mathrm{QNC,max}}$ and $EA_{\mathrm{QND,min}} \leq EA \leq EA_{\mathrm{QND,max}}$ are the feasible ranges of the emitter area of QNC and QND, respectively. Without loss of generality, let us assume: $EA_{\mathrm{QNC,min}} \leq EA_{\mathrm{QND,min}} < EA_{\mathrm{QNC,max}} \leq EA_{\mathrm{QND,max}}$. The aim is again to merge the both device types in a common model card QNCD with minimum number of additional sweeping parameters.

Table 1. Performances of the buffer amplifier: specification, before, and after the optimization.

Performance	Specification	Initial	Optimized
Bandwidth, MHz	maximized	110.1	150.1
Phase margin, degree	>60	70.6	60.0
Supply current, mA	<2	1.896	1.900
SlewRateUp, MV/s	>500	609.8	519.3
SlewRateDown, MV/s	>500	787.2	691.6
Offset, mV	<1	0.6136	0.043
PSRR, dB	<−70	−74.15	−73.88
output rmsNoise, μV	<300	277.5	192.7

For this, the sweeping parameter s_1 is introduced and the model cards of QNC and QND are extended as:

$$EA_{\mathrm{QNC,min}} \leq s_1 \leq EA_{\mathrm{QNC,max}} : \boldsymbol{R}^{\mathrm{QNC1}}(s_1) := \boldsymbol{R}^{\mathrm{QNC}}(EA \rightarrow s_1)$$
$$EA_{\mathrm{QNC,max}} < s_1 \leq EA_{\mathrm{QND,max}} : \boldsymbol{R}^{\mathrm{QNC1}}(s_1) := \boldsymbol{R}^{\mathrm{QNC}}(EA_{\mathrm{QNC,max}})$$
$$EA_{\mathrm{QNC,min}} \leq s_1 < EA_{\mathrm{QND,min}} : \boldsymbol{R}^{\mathrm{QND1}}(s_1) := \boldsymbol{R}^{\mathrm{QND}}(EA_{\mathrm{QND,min}})$$
$$EA_{\mathrm{QND,min}} \leq s_1 \leq EA_{\mathrm{QND,max}} : \boldsymbol{R}^{\mathrm{QND1}}(s_1) := \boldsymbol{R}^{\mathrm{QND}}(EA \rightarrow s_1)$$

Note, that the feasible ranges of s_1 are identical about the new model cards QNC1 and QND1. The QNCD model card is obtained by linear sweeping with a second parameter s_2, assuming e.g. QNCD$|_{s2=0} \leftrightarrow$QNC1 and QNCD$|_{s2=1} \leftrightarrow$QND1:

$$\boldsymbol{R}^{\mathrm{QNCD}}(s_1, s_2) = (\boldsymbol{R}^{\mathrm{QND1}}(s_1) - \boldsymbol{R}^{\mathrm{QNC1}}(s_1))s_2 + \boldsymbol{R}^{\mathrm{QNC1}}(s_1).$$

The latter is schematically shown in Fig. 4. It should be pointed out, that again one of the sweeping parameters (i.e. s_1) is used also to replace the instance parameter *EA*, thus reducing the order of the optimization problem. Note, that with such device type arrangement, nonphysical parameter values (e.g. s_2=0, $EA_{\mathrm{QNC,max}} < s_1 \leq EA_{\mathrm{QND,max}}$) may be evaluated as final optimum, but they can be rounded to the closest feasible parameter set (e.g. s_2=0, $s_1 = EA_{\mathrm{QNC,max}}$) without loosing the optimum circuit performance $\boldsymbol{Q}$.

4 Application of the new approach

The described novel approach for automatic optimization of the device types has been tested optimizing the BiCMOS integrated buffer amplifier with moderate complexity proposed in Furth and Andreou (1993). Its electrical scheme is shown in Fig. 5. The circuit contains seven bipolar transistors and has to be realized with a 0.6 μm BiCMOS fabrication technology providing 13 different types of bipolar transistors with fixed as well as continuously and discrete scalable emitter lengths.

The goal of the optimization has been the increasing of the bandwidth of the amplifier, keeping the rest of its performances within the specification constraints (see Table 1). Therefore, the transit frequency has been chosen to be the dominant figure-of-merit for the arrangement of the whole variety of bipolar transistors. The arrangement has been done with two sweeping parameters, one of which has replaced the emitter length instance parameters, as described in Sect. 3.3. The smooth sweeping between the different transistor types has been done using piece-wise linear functions. The amplifier has been optimized with the commercial analog circuit optimization tool WiCkeD (MunEDA GmbH, 2008). By this, only gradient-based optimization strategies have been used. During this test, only the bipolar transistors' parameters (type and sizing) have been optimized; all other circuit devices have been kept unchanged.

The results are given in Table 1: the bandwidth has been improved significantly at the cost of reasonable phase margin degradation, keeping all other performances nearly unchanged. This optimum has been achieved with only 5 optimization steps, thus demonstrating not only the efficiency of the proposed novel approach, but also its excellent compatibility with the modern CAD-tools for analog circuit design.

5 Conclusions

A novel approach for analog circuit optimization involving automatic selection of the device types has been presented. Including additional formal parameters to the model cards of the devices, it permits a smooth transition of the model parameters across the range of available device types. In this way, the optimal device type can be evaluated using gradient-based optimization strategies. At the same time, the proposed approach is fully compatible with stochastic optimization algorithms. Thus, the universality of the latter can be utilized together with the efficiency of the deterministic optimization techniques.

Acknowledgements. This work was supported by the BMBF research project HONEY under grant No. 01 M 3184.

References

Berkner, J.: Kompaktmodelle fuer Bipolartransistoren, expert verlag, 2002.

Cadence Design Systems: Virtuoso NeoCircuit Circuit Sizing and Optimization, http://www.cadence.com/products/custom_ic/neocircuit/index.aspx, 2008.

Dimov, B., Hennig, E., Lang, Ch., and Sommer, R.: Direct Performance Evaluation of Bipolar Transistor Devices for Analog Circuit Design, Proc. Xth Int. Workshop on Symbolic and Numeric Methods, Modeling and Applications to Circuit Design SMACD'08, 49–55, 2008.

Furth, P. M. and Andreou, A. G.: A High-Drive Low-Power BiCMOS Buffer Using Compound PMOS / NPN Transistors, Proc. 36th Midwest Symposium on Circuits and Systems, 2, 1369–1372, 1993.

Graeb, H.: Analog Design Centering and Sizing, Springer, 2007.

Gummel, H. K. and Poon H. C.: An Integral Charge Control Model of Bipolar Transistors, AT&T Tech. J., 49, 827–852, 1970.

MunEDA GmbH: WiCkeD Tool Suite, http://www.muneda.com, 2008.

Wolfram Research: Mathematica 6, http://www.wolfram.com/products/mathematica/index.html, 2008.

X-FAB Semiconductor Foundries AG: Design Kit Documentation, http://www.xfab.com/fileadmin/X-FAB/Download_Center/Technology/BiCMOS/XB06_Data_sheet.pdf, 2008.