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Influence of gate tunneling currents on switched capacitor integrators

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Abstract. In order to achieve a higher level of integration in modern VLSI systems, not only the lateral geometrical dimensions have to be scaled. Lowering the supply voltage also requires scaling down the oxide thickness of the transistors. While the oxide thickness is scaled down proportionally with the supply voltage, the gate tunneling currents grow exponentially, which results in special issues concerning deviations in charge based analog and mixed signal circuitry. The influence of gate tunneling currents on this kind of circuits will be demonstrated at a fully differential switched capacitor integrator. The used process data is derived from the International Technology Roadmap for Semiconductors (ITRS Roadmap, 2006). The Parameter sets for the simulations are based on the Predictive Technology Model of the Arizona State University Modelling Group for the 65 nm Technology node (Predictive Technology Model, 2008).

1 Introduction

Physical constraints are the burden of modern VLSI circuits. One of the emerging problems is the gate tunneling current. The ITRS (ITRS Roadmap, 2006) forecasts a straight increase in the next few years, like it can be seen in Fig. 1. In comparison to the source drain leakage like gate induced drain leakage or subthreshold currents, not only the source and drain nodes are incorporated. The tunneling currents also run over the gate node. Figure 2 shows the different parts of the gate tunneling currents. For the operating points of our circuit the gate to bulk current I_{GB} can be neglected. The gate to channel current can be divided in one part to the source node I_{GCS} and one to the drain node I_{GCD}. These two are only relevant for an existing channel. The currents I_{GS} and I_{GD} in the gate to drain and gate to source overlap regions have always to be considered. Figure 3 shows the simulation of the different gate tunneling currents for the source node at V_{SS} and the drain node at V_{DD}. The voltages from gate to source and gate to drain have different signs. The corresponding gate tunneling currents therefore result in a zero crossing of the overlap component $I_{GS}+I_{GD}$ for $V_{GS}=V_{DD}/2$. For gate voltages above the threshold voltage the additional gate to channel currents have to be added to the overlap parts and result in a curve with a zero crossing near but not exactly at $V_{GS}=V_{DD}/2$. The incorporation of the additional node to the leakage path requires a more complex analysis of the circuit. The following considerations will start at simple building blocks and will transfer this knowledge to the fully differential integrator.

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2 The transfer gate

The used transfer gate consists of one p-MOSFET and one n-MOSFET of the same size. This is necessary for conduction over the full voltage range and to eliminate the channel charge injection due to switching it on or off.

There are two different states of a transfer gate that have to be discussed. The conducting state allows the gate tunneling currents to flow across the channel. Both endpoints of the transfer gate will be influenced in the same way by the tunneling currents flowing from the gate to each endpoint. When the transfer gate blocks, both endpoints are separated and do not influence each other anymore. First we have a look at the blocking state. Figure 4a shows a transfer gate with a potential V_1 at the top node above $V_{DD}/2$. This causes a high voltage drop at the overlap region of the n-MOSFET and a low voltage drop at the overlap region of the p-MOSFET. Considering the exponential dependency of the gate tunneling currents to the voltage drop it is clear that the influence of the n-MOSFET is dominant in this case. When the voltage

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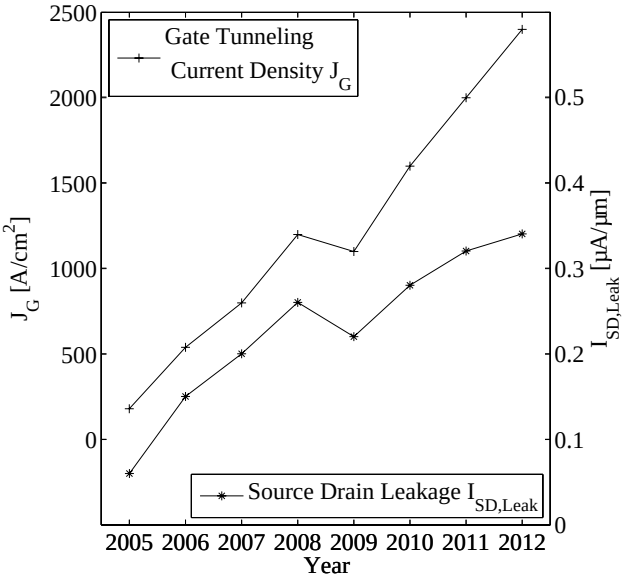

Fig. 1. The evolution of gate tunneling current density as predicted by the ITRS (ITRS Roadmap, 2006).

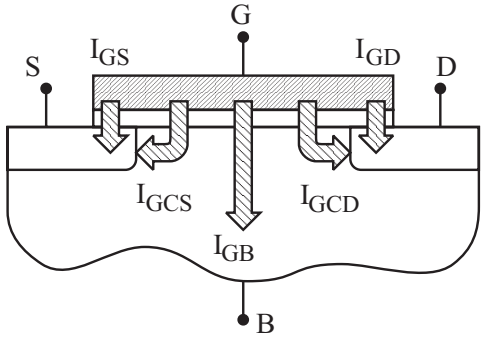

Fig. 2. The different parts of the gate tunneling currents in a MOSFET.

V_1 reaches a value near $V_{DD}/2$ the gate tunneling currents to the p- and the n-MOSFET are of the same size but of the opposite direction. In this case the gate tunneling currents eliminate each other. Due to the different tunneling characteristics of p- and n-MOSFETs this zero crossing will not be exactly at $V_{DD}/2$ (see Fig. 5).

In the conducting state both transistors establish a channel and add their gate to channel tunneling currents to the overlap part. But not only the absolute values of the gate tunneling currents change, also the zero crossing changes. The different threshold voltages of the n- and the p-MOSFET cause different tunneling characteristics, which lead to a shifted zero crossing. Figure 5 shows the comparison of both states depending on the input voltage V_1.

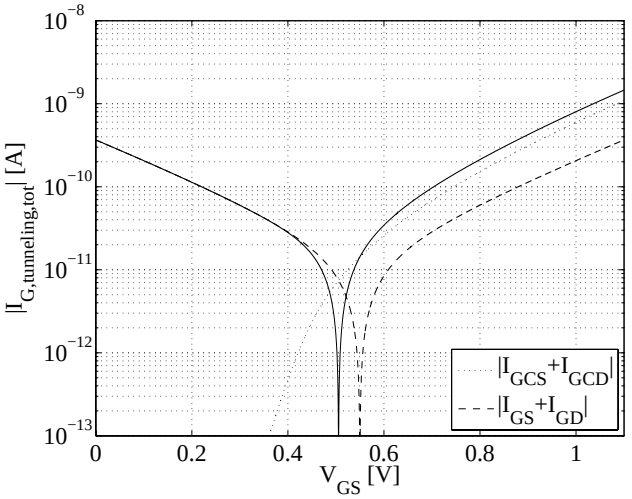

Fig. 3. Simulation results of the gate tunneling currents of a single n-MOSFET with minimal dimensions.

3 The switched capacitor integrator

3.1 Single ended integrator

Switched capacitor circuits handle and process signals by manipulating the charge stored on the involved capacitors. To see the influence of gate tunneling currents on this signals, it has to be shown in which part of the circuit and in which switching state this influence is really relevant.

At the switched capacitor integrator there are two phases, the charging phase and the integration phase. Figure 6 shows the charging phase. The coupling capacitor C_R is charged to the input voltage V_{in}. Both nodes of C_R are connected to a definite potential with a low resistance. Therefore the gate tunneling currents flow to these sinks and do not affect the amount of charges stored on C_R. One node of the integration capacitor C_I is connected to the low resistance output of the operational amplifier. The other is connected to the high resistance input of the operational amplifier and a blocking transfer gate, see Fig. 6. This node is affected by the gate tunneling currents of the transfer gate and of the operational amplifier. The influence of the operational amplifier will be discussed later. The high resistance node of C_I, which is directly connected to this transfer gate has an input voltage of $V_{DD}/2$ and will cause a very low drift of the stored charge due to a very low gate tunneling current (compare to Fig. 5).

In the integration phase the charge from C_R will be transferred to C_I. When the circuit has settled, the high resistance node at the input of the operational amplifier will have the potential of $V_{DD}/2$. Then again gate tunneling currents do not influence this node. But during the charge transfer the voltage at this node can be significantly different from $V_{DD}/2$. Figure 5 shows that the gate tunneling current can thus be about two to three decades higher than in the settled state. By integrating the gate current over this short time the

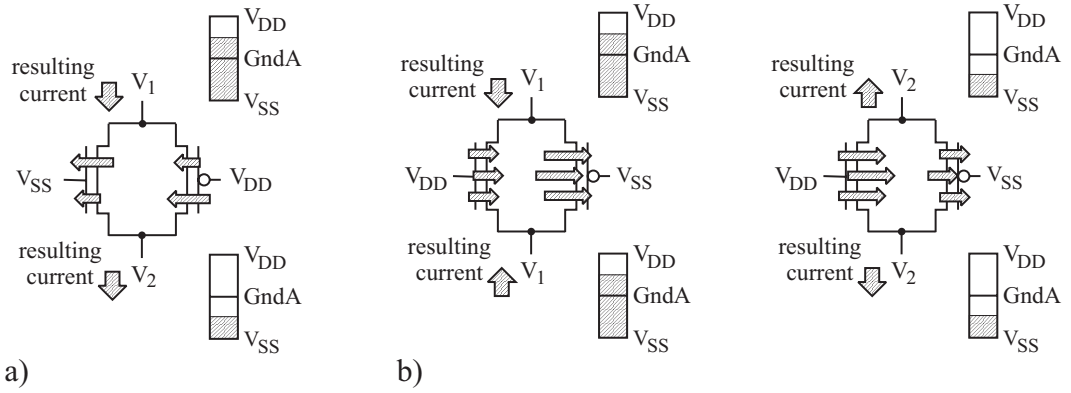

Fig. 4. Gate tunneling currents of a transfer gate in **(a)** the blocking and **(b)** the conducting state.

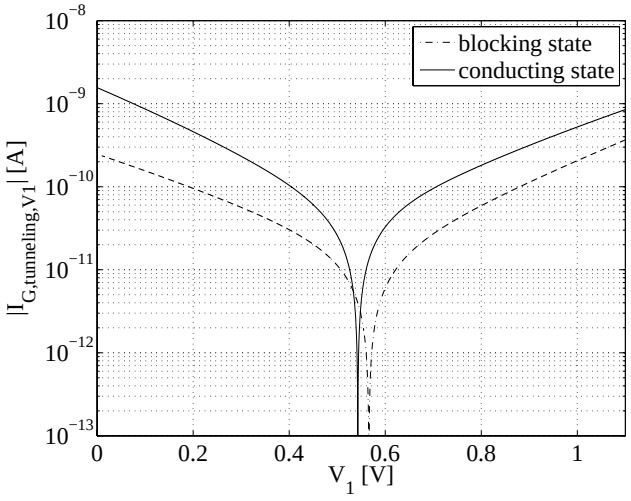

Fig. 5. Simulation results of the gate tunneling currents for the blocking and the conducting state of a transfer gate.

charge deviation can be calculated. It is proportional to the signal deviation caused by the gate tunneling currents.

3.2 Fully differential integrator

Extending the circuit with an inverted path results in the fully differential architecture. Common mode effects can be eliminated by using this technology. During the charging phase the high resistance nodes are again at $V_{DD}/2$ and the gate tunneling current in both paths is of the same value and direction. It results in a common mode effect which can be eliminated by the fully differential architecture. Local mismatch of the relevant transistors causes a residual error, but this is small in the regarded technology. This can be neglected. The same applies for the settled state of the integration phase.

During the settling phase the high resistance nodes at the input transistors of the operational amplifier have inverted potentials referenced to $V_{DD}/2$ (see Fig. 7). The resulting high gate tunneling currents are also opposite in sign and result in a differential mode signal. This can not be eliminated with the fully differential architecture.

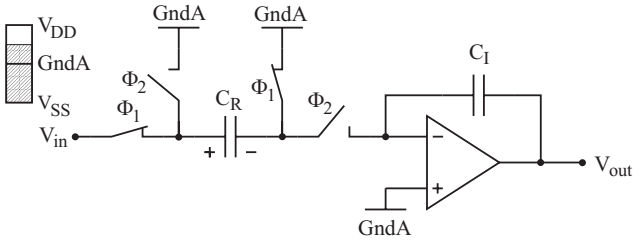

Fig. 6. Gate tunneling currents in the charging phase of a single ended switched capacitor integrator.

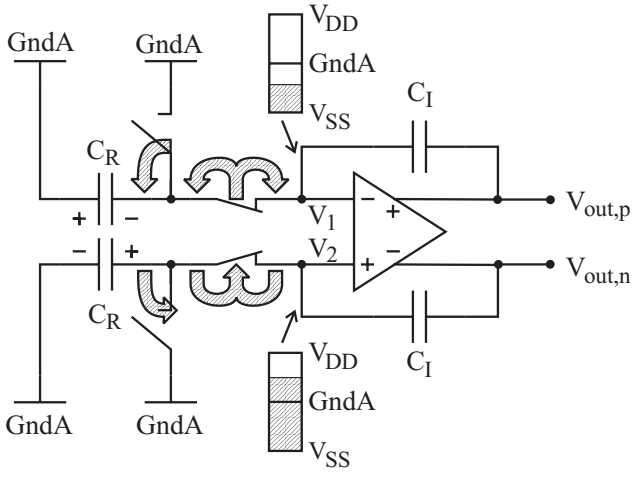

Fig. 7. Gate tunneling currents in the integration phase of a fully differential switched capacitor integrator.

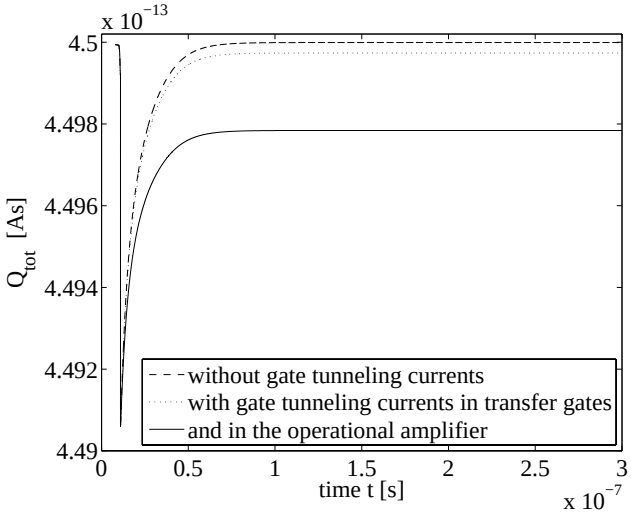

Fig. 8. Time dependency of the stored charges for the three simulations without tunneling currents, with gate tunneling currents in all transistors but the input transistors of the operational amplifier and in all transistors. At the beginning of this simulation C_R had been charged to the highest input value.

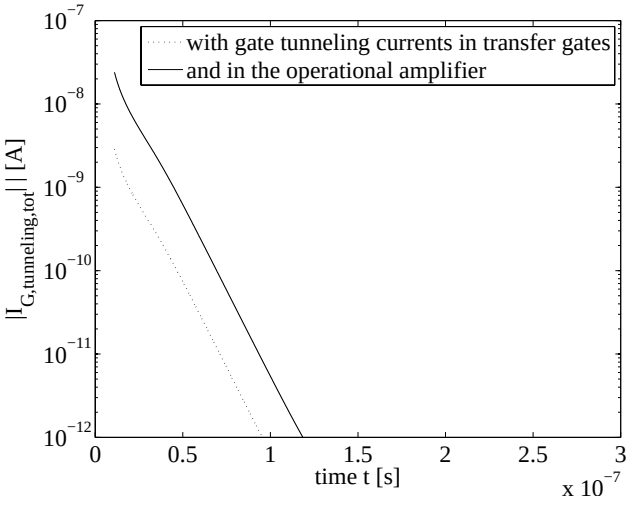

Fig. 9. Time dependency of the gate tunneling currents for the simulation with gate tunneling currents in all transistors but the input transistors of the operational amplifier and in all transistors.

3.3 Gate tunneling currents in the input transistors of the operational amplifier

An operational amplifier has a symmetrical input stage. Both input transistors show the same gate tunneling current for equal potentials at both nodes. Also the direction of the gate currents is the same. When local mismatch is negligible, gate tunneling currents can be eliminated by the fully differential architecture in this operation mode. That's why the operational amplifier does not affect the stored signal during the charging phase or in the settled state of the integration phase.

During the settling phase the potentials at both input nodes are significantly different from each other. This results in gate tunneling currents in the same way as in the transfer gates, but the currents are much higher. Because of matching constraints and speed requirements, the input transistors have to be designed with a larger area compared to the transfer gates. The gate tunneling currents are proportional to this area. During the settling state of the integration phase the influence of the input transistors of the operational amplifier can not be eliminated by the fully differential architecture.

4 Simulation results

The considerations in the last sections showed that the influence of the gate tunneling currents is relevant just in the settling state of the integration phase. Right in this moment, when the transfer gates are also switched, some other effects overlay the gate tunneling currents. In the two transistors of the transfer gates the gate voltage switches from V_{DD} to V_{SS} and vice versa. This voltage ramp at both transistors does not switch them on or off at the same time, because the threshold voltages of the n- and the p-MOSFET are different. So the charge flowing from the transistor channels to source and drain will be stored temporarily on the integration capacitor C_I. During this settling mechanism the currents do overlay each other and cannot be separated properly.

The simulation tools offer us the possibility to switch the gate tunneling currents on or off for selected transistors by changing the transistor parameters. Three simulations have been made. The first was completely without gate tunneling currents. The second simulation took the gate tunneling currents of all but the input transistors of the operational amplifier into account. With the third simulation the input transistors of the operational amplifier were also added.

To observe the influence of the gate tunneling currents, the charge was calculated, which is stored in the complete integrator. After the charging phase has finished, the stored charges only will be transferred from one to the other capacitor. During the settling state there will be a slight deviation of the summed charges, but when it is settled, the temporary charge injection has vanished again. Figure 8 shows this behavior for the simulation without gate tunneling currents.

Taking the tunneling currents of the transfer gates into account, a small amount of the stored charge will be removed by these currents. Figure 8 also shows the reduced charge stored in the capacitors. The difference of the stored charge with and without gate tunneling currents at any time gives the deviation of charge up to this moment. By differentiation of this charge deviation the gate tunneling current at this time can be calculated and is shown in Fig. 9.

The input transistors of the operational amplifier have to be designed wider than the ones used in the transfer gates because of matching and speed constraints. The larger area

causes larger gate tunneling currents. In addition to that the operation mode of these input transistors normally is in inversion, which always causes tunneling currents to the channel. Figure 9 shows about one decade larger gate tunneling currents compared to the transfer gates only.

A closer look at the time dependency in Fig. 9 shows a nearly exponential behavior. This can be explained considering the settling process in the integration phase for a high input signal. The charge from Capacitor C_R will be transferred to C_I driven by the output current of the operational amplifier, which is in the overdrive mode. In this mode the current is constant and therefore the voltage at the high resistance node will change linearily. Gate tunneling currents depend on the voltage in an exponential way, which results in the exponential time dependency.

The absolute values of the simulation with all gate tunneling currents show a deviation of the stored charges of $2.2{\cdot}10^{-16}$As, which is equivalent to about 0.05% of the signal. Taking into consideration that the integrator was designed for 10 bit resolution, the dissipated charge is equivalent to a half bit. But the gate tunneling currents depend exponentially on the voltage. So it is clear that this deviation only can be seen at high input levels.

5 Conclusions

Gate tunneling currents make the leakage problem more complex. But not every transistor contributing gate tunneling currents affects the signal path. Only the high resistance nodes at the signal storing capacitors are sensitive to them. In comparison of all relevant transistors, the input transistors of the operational amplifier had the biggest influence. They caused about one decade higher deviations of the stored signal than the rest of the relevant transistors.

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