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Circuit design with Independent Double Gate Transistors

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Abstract. Circuits with transistors using independently controlled gates have been proposed to reduce the number of transistors and to increase the logic density per area. This paper introduces a novel Vertical Slit Field Effect Transistor with unique independent double gate properties to demonstrate the possible advantages for independent double gate circuits. A new adder circuit is proposed, where the power could be reduced by one fifth and the area by on third compared to a tied gate configuration.

1 Introduction

Transistors with two gates have been investigated from the early days of semiconductor devices – namely the "Unipolar 'Field Effect' Transistor" proposed by Shockley in 1952 (Shockley, 1952). However for the last decades the single gate MOSFET in planar integrated CMOS technology dominated the semiconductor industry. Enormous progress has been made to scale transistors to ever smaller dimensions to obtain faster transistors, as well as to lower the effective costs per transistor in terms of transistors per area. With scaling device dimensions and increasing short channel effects, multiple gate transistors have been investigated to obtain an improved gate control. However multiple gate transistors can do more than just overcome the problems of increased short channel effects. If the multiple gates can be controlled independently, the logic functionality per transistor and logic density per area can be increased too. The basic concept of independent double gate transistors for logic circuits is discussed in Sect. 2. A novel transistor with excellent independent double gate properties is introduced in Sect. 3. The impact on circuit design using independent double gate transistors is outlined in Sect. 4. Basic NAND and NOR circuits are shown in Sect. 5 and adder circuits in Sect. 6.

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2 Independent Double Gate Transistors

Standard CMOS transistors within logic circuits can be seen as a switch where the gate turns the transistor "ON" and "OFF". Using more than one gate, the behaviour of the switch depends on the number of controlling gates and additional logic can be implemented into one transistor. Transistors using independently controlled gates are not limited to two gates, but for reasons of the transistor geometry and the connectivity of the terminals it is convenient to use only two gates. Independent double gate transistors can be used to implement a logic "OR" or "AND" functionality within one transistor. For the "OR" type transistor this means that if gate 1 is "low" and gate 2 is "high" the transistor is turned "ON" and vice versa for gate 1 is "high" and gate 2 is "low" (where "low" and "high" are the logic voltage levels). Similar as for the "AND" type transistor and the gates biased in the same way as just described the transistor is turned "OFF". For the rest of the paper this is referred to the "independent gate configuration" (IGC). For the case that both gates are "high", the transistor is turned "ON" for a n-type transistor and "OFF" for a p-type transistor and vice versa for both gates are "low". For the rest of the paper this is referred to the "tied gate configuration" (TGC), where the transistor can be treated as standard transistor with one gate only using the standard transistor symbols.

For CMOS multigate (or FinFET) transistors the "OR" can easily be implemented, as for the double gate transistor there are two parallel inversion channels. However implementing the "AND" functionality is rather difficult for the IGC, as the transistor must turn "OFF" though one gate is still "low" or "high", which leads in general to a significant leakage current. Circuits proposed in Chiang et al. (2006)

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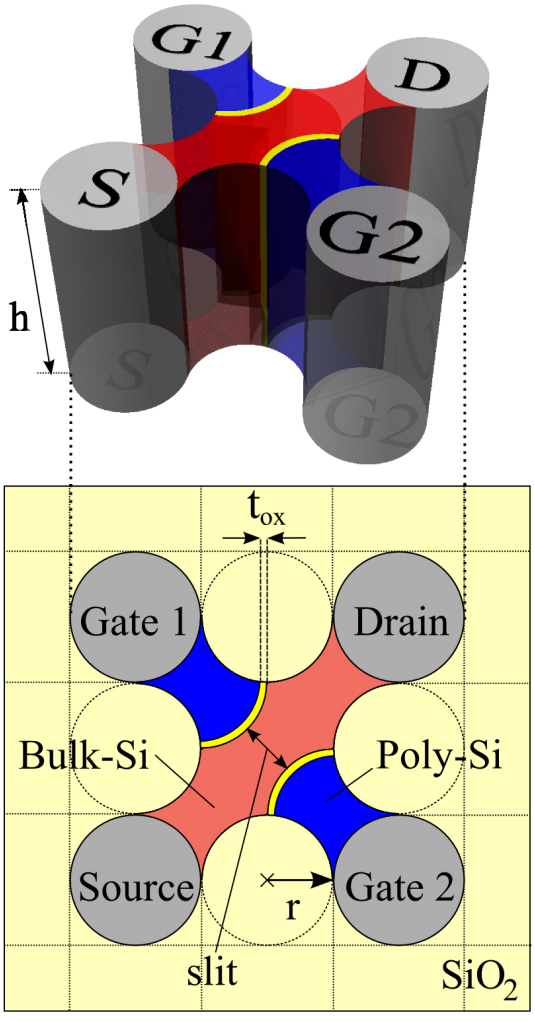

Fig. 1. Vertial Slit Field Effect Transistor.

and Mukhopadhyay et al. (2005) using transistors with the "AND" functionality suffer from these high leakage currents. Recently published Vertical Slit Field Effect Transistors (VeSFET) can offer "OR" and "AND" functionality without suffering high leakage for the "AND" type device for the IGC (Maly and Pfitzner, 2008; Weis et al., 2008; Lin et al., 2008).

3 Vertical Slit Field Effect Transistor

The VeSFET was developed in order to achieve an extreme regularity in layout of integrated circuits (Maly, 2007; Maly and Pfitzner, 2008). The implementation shown in Fig. 1 provides a square shaped unit device built on a silicon on insulator (SOI) substrate and all transistors are isolated from each other. The geometry in Fig. 1 is based on a standard feature size represented by the radius r. The four terminals are implemented using vertical metal pillars. The channel volume is defined by the distance between the source and drain terminal as well as the height h and the width of the vertical "slit" between the two gates.

3.1 Working principle of VeSFET

The VeSFET is a pn-junction-less transistor with a gate controlled bulk current using either a p- or n-type substrate for the complementary transistor types. It can be regarded as a hybrid of a Junction Field Effect Transistor (JFET) and a MOSFET. The operation is JFET-like because it is based on transport of majority carriers in a bulk channel, whose effective width is controlled by depleted regions induced by two gates on both sides of this channel. The gates, however, are separated from the channel by an insulating layer, like in a MOSFET. The difference to the MOSFET is that the current is not bound to an inversion channel but flows through the whole bulk volume between source and drain terminal. In the off-state the depletion regions induced by the two gates fill the whole channel and the device is non-conducting. For a normally "OFF" transistor the gate material has to be chosen such that for a n-type transistor and the gates biased "low", the depletion widths are close to their maximum expansion, and vice versa for a p-type transistor and the gates biased "high". Applying appropriate voltages to the gates the depletion regions withdraw and a conducting path from drain to source is established.

3.2 Independent Double Gate Operation of VeSFET

Modulation of the depleted regions induced by the two independently controlled gates can implement "AND" and "OR" functionality. This can be achieved via low and high substrate doping, as the depletion region is a function of the substrate doping for a given set of geometry and applied voltages at the terminals. The independent double gate feature of the VeSFET is illustrated in Fig. 2.

For the OR-type the depletion regions from gate 1 and gate 2 are overlapping in the middle of the channel for the case that both gates are "low" and the transistor is turned "OFF", as shown in Fig. 2a. The overlap region must be at least in the range of the debye length to ensure the transistor is "OFF". If an appropriate voltage is applied to gate 1 the corresponding depletion width will withdraw. A conducting path between source and drain will be established as shown in Fig. 2b and the transistor is "ON". The complementary case for gate 2 is shown in Fig. 2c. Applying a voltage to both of the gates both depletion widths will withdraw and the maximum opening of the channel is established, see Fig. 2d.

For the AND-type the depletion width of the gates reaches to the opposite gate, see Fig. 2e. Hence the overlap region extends over the whole channel and the transistor is "OFF". If now a voltage is applied to gate 1 the corresponding depletion region will withdraw. However the depletion with resulting

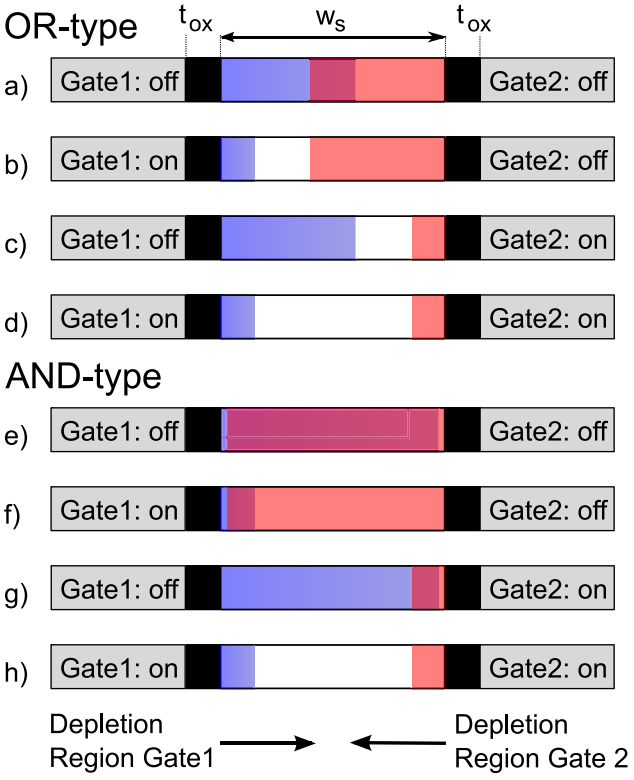

Fig. 2. Independent Double Gate for VeSFET OR- and AND-type.

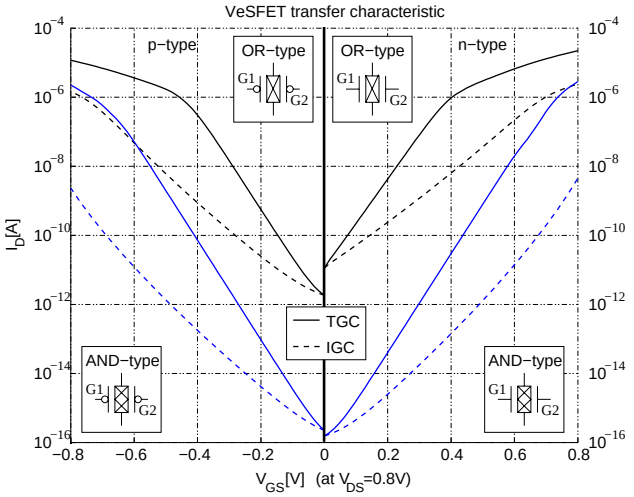

Fig. 3. Independent Double Gate VeSFET transfer characteristics.

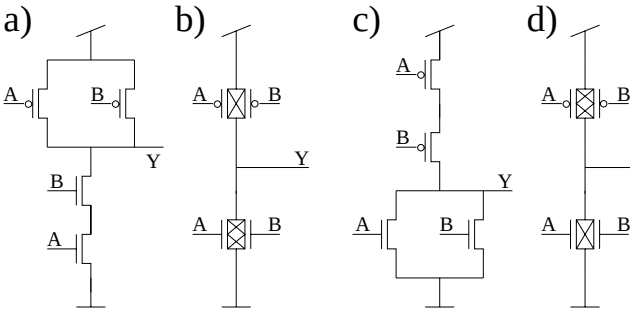

Fig. 4. 2-input NAND and NOR with TGC **(a)**, **(c)** and IGC **(b)**, **(d)**.

from gate 2 prevents establishment of a low-ohmic connecting path between source and drain as shown in Fig. 2f. Consequently the transistor is "OFF". The complementary case for gate 2 is shown in Fig. 2g. Only if an appropriate voltage is applied to both gates a low-ohmic connecting path between source and drain can be established as shown in Fig. 2h.

From device simulation low power optimized transistors were derived, where Fig. 3 shows the transfer characteristic for p- and n-type for IGC and TGC and introduces the transistor symbols (Weis et al., 2008). The transistor dimensions used for the circuits in this paper are t_{ox}=4 nm, r=50 nm and h=320 nm with substrate dopings of 1.5×10^{17} cm^{-3} for the AND-type and 5×10^{17} cm^{-3} for OR-type using polysilicon as gate material. For the AND-type IGC good turn-off is achieved with "OFF" currents around 4 nA and 2 nA for n- and p-type. TGC "ON" currents are 2.2 μA and 2.8 μA, respectively. For the OR-type TGC the "ON" currents are 22 μA and 12 μA for n- and p-type and for the IGC the "ON" currents are 2 μA and 3 μA respectively.

4 Impact on circuit design

From circuit design perspective the use of independently controlled transistors can reduce the number of transistors, as two transistors connected in parallel or series can be merged into one transistor, which is exemplary shown in Figs. 4 and 5. This technique reduces area, transistor stack height and power consumption. However all independent double gate transistors have in common that for the IGC the transistors "ON" and "OFF" currents are degraded compared to the TGC. For "OR" type devices this leads to higher gate delay and for the "AND" type devices this leads to higher leakage for the IGC. For this reason during times when the circuit is inactive input patterns should be applied in a way that both gates are at the same potential to reduce the leakage to a minimum. Multiple devices can be used in critical paths to compensate for the lower drive current in IGC. However there are cases where the TGC is a better choice instead of using multiple IGC. For this reason a trade-off between area reduction, gate delay and leakage has to be chosen when using transistors with independently controlled gates. The use of IGC is best for gates with small fan out and short capacitive wire loads.

In the following circuits using VeSFET with independently controlled gates are investigated by simulation. The proposed circuits are not limited to VeSFET and could be implemented with any type of transistor with independently controlled gates offering the "AND" and "OR" functionality.

Table 1. 2-input NAND and NOR for VeSFET and CMOS PTM.

configuration	power [nW]	leakage current min/max [nA]	rise/fall time [ps]	rise/fall delay [ps]
4a VeS	7.12	0.17/3.50	32.6/83.8	37.1/24.5
4b VeS	6.23	0.09/29.5	34.3/58.7	36.4/23.9
4a PTM	11.75	1.88/5.14	38.9/74.5	16.9/21.6
4c VeS	10.12	0.06/1.74	143/53.6	72.7/26.7
4d VeS	3.75	0.01 / 2.31	177/96.4	89.5/59.4
4c PTM	13.74	0.07/5.25	140/27.2	70.8/9.6

5 2-input NAND and NOR

Two input NAND and NOR gates in static CMOS are built in general with four transistors. Using independent double gate transistors the number of transistors can be reduced from four to two, merging transistors in parallel and in series as shown in Fig. 4. As mentioned in the previous section this will impact the power, delay and leakage currents. This structure was shown for the first time in Chiang et al. (2006) for double gate MOSFET, but with extremely high leakage in the independent gate configuration. A two transistor NAND, NOR using independent double gate VeSFET is compared to a four transistor NAND, NOR using OR-type VeSFET and to 65 nm CMOS based on the predictive technology model (PTM) (NIMO, 2008). The input is a piecewise linear voltage source with 50 ps rise and fall time. Each gate under test drives four identical copies of itself as load. The power for VeSFET compared to CMOS is reduced up to 40% due to lower device capacitances of VeSFET. Comparing IGC to TGC VeSFET the power can be further reduced by more than 10%. The leakage current for the IGC VeSFET gate is strongly dependent on the input pattern. For the case that both gates are on the same potential the leakage can be significantly reduced. However if the gates are on different potential the leakage can be increased by a factor of 8. Therefore clever input patterns should be applied during times when the circuit in inactive. The delay and the fall and rise times for all configurations for NAND and NOR are in same order of magnitude. The results are shown in Table 1 where the configuration refers to the circuits in Fig. 4. For the case that the NAND or NOR gate drives a fixed load capacitance of 1 fF the TGC VeSFET implementation is up to a factor 1.8 slower than CMOS 65 nm PTM and the VeSFET IGC is up to 3 times slower than the TGC VeSFET. However the power is reduced comparing CMOS and TGC VeSFET and can be further reduced using IGC VeSFET. Independently controlled double gate transistors can reduce the power, and the transistor count, respectively area reduction up to 50%, but it comes at the cost of an increased delay.

Table 2. One bit full adder.

configuration	average active power	minimum standby power	maximum $\overline{\text{Sum}}$ delay	maximum $\overline{\text{Cout}}$ delay
5a, OR	243.09 nW	16.091 pW	340.45 ps	198.69 ps
5a, AND	172.90 nW	2.5957 fW	2.9069 ns	1.3101 ns
5b	207.58 nW	85.89 pW	1.3998 ns	1.1076 ns
5c	203.14 nW	8.863 nW	1.2928 ns	590.84 ps
5a, PTM	220.81 nW	65.41 pW	327.58 ps	245.79 ps

6 Adder circuits

A new one bit full adder circuit using independent double gate VeSFET is proposed, which will be used to build a 16 bit ripple carry adder. Primary goal was to reduce the area and the transistor count. To find a metric for comparison all transistors are minimum sized. The area of the CMOS layout is assumed equal to that for TGC VeSFET. The independent gate VeSFET circuits are compared to the tied gate circuits using VeSFET as well as to 65 nm CMOS based on the predictive technology model (PTM) (NIMO, 2008).

6.1 One bit full adder

For the one bit full adder the standard mirror adder proposed by Weste is used (Weste and Harri, 2005). The tied gate configuration has 24 transistors without output inverters for the sum and the carry signal as shown in Fig. 5a. With independently controlled gates the transistor count can be reduced by one third to only 16 transistors. Two different circuits are shown in Fig. 5b and 5c. For the circuit shown in Fig. 5b "OR" and "AND" type transistors are used, whereas for the circuit shown in Fig. 5c only "AND" type transistors are used. The advantage for the latter circuit is that the maximum number of stacked transistors for the carry signal is reduced from two to one and the delay is decreased. For the simulation setup the inverted carry out signal is connected to another one bit full adder as capacitive load and the inverted sum signal is connected to an inverter with a fan out of two. All capacitive wire loads from the area optimized layout are included. All 56 possible transitions for the input pattern are applied using an ideal input driver with a rise and fall time of 50 ps. The results for the average power per pattern, the minimum standby power and the maximum delay for the inverted sum and carry out signals are given in Table 2.

For a supply voltage of 0.8 V one can see from Table 2 that for the circuit 3a using "OR" type TGC VeSFET the maximum inverted carry out delay ($\overline{\text{Cout}}$) is close to standard CMOS using the PTM 65nm model. Using 'AND' type TGC VeSFET leads to a dramatic increase of delay for the $\overline{\text{Cout}}$ and the $\overline{\text{Sum}}$, but also to a dramatic decrease of standby power (5a, AND). Comparing the IGC to the TGC the delay is increased by 2.4 and the leakage is higher for

Table 3. 16 bit ripple carry adder.

configuration	average active power	average standby power	maximum $\overline{\text{Cout}}$ delay	transistor count
5a, OR	0.32171 uW	11.273 nW	4.19 ns	432
5b	0.24891 uW	24.064 nW	24.49 ns	304
5c	0.25768 uW	11.676 nW	20.69 ns	304
5a, PTM	0.39701 uW	67.165 nW	2.77 ns	432

the configuration 3c. For the configuration 5b, the leakage is almost the same but the delay is five times higher. However the active power for both IGC circuits is reduced compared to the TGC (5a, OR and 5a, PTM) due to the lower capacitances and, most important, the area is reduced by one third, where the IGC area is 2.56 μm^2 compared to 3.24 μm^2 for the TGC.

6.2 16 bit ripple carry adder

The 16 bit ripple carry adder is built from the one bit full adder block discussed in the previous section. To reduce the number of transistors one can alternate stages using inverted and non-inverted signals for the input vectors. For a supply voltage of 0.8 V the results are shown in Table 3 for average active and standby power for random patterns, as well as the maximum $\overline{\text{Cout}}$ delay for the last stage and the transistor count. For the area calculation the inverters for the inverted input signals as well as the inverters for the sum signals are included, where the area for the TGC is 92.16 μm^2 and for the IGC 61.44 μm^2. For the input pattern an ideal input driver with a rise and fall time of 50 ps is used and all capacitive wire loads from the layout are included.

For TGC "OR" type VeSFET implementation (configuration 5a, OR) the delay is increased by 1.5 compared to the standard CMOS using PTM 65 nm (5a, PTM), however the active power can be reduced by 20%. As expected, due to lower drive current for the IGC VeSFET, the delay increases for the IGC implementations (5b, 5c) by factors 6 and 5 compared to the TGC VeSFET. The active power consumption for both IGC implementations is reduced to one fifth compared to CMOS. The area reduction for the IGC compared to the TGC is again one third.

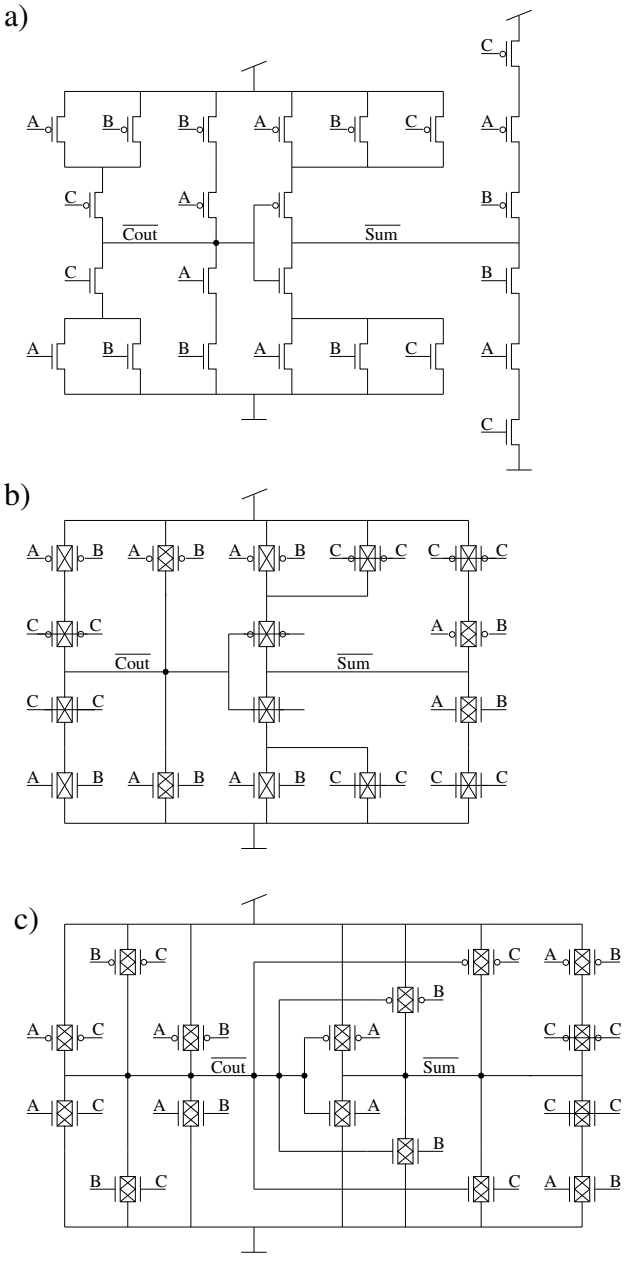

Fig. 5. One bit full adder: **(a)** Tied Gate **(b)** and **(c)** Independent Gate.

7 Conclusions

In this paper the circuit design using independently controlled gates using a novel Vertical Slit Field Effect Transistor was demonstrated and the impact on figures of merit for power consumption, delay, leakage behaviour and area was presented. It was shown that the transistor count and respectively the area can be significantly reduced for logic gates, hence the logic density per area increases. For low power circuits standby patterns are favorable where both transistor gates are on the same potential offering even less leakage current. However due to the lower drive current in the IGC mode of operation the delay will be increased. For this reason independent double gate transistors are not the first choice for high speed circuits but fit perfectly in the low power application domain.

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