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High-voltage (100 V) Chipfilm™ single-crystal silicon LDMOS transistor for integrated driver circuits in flexible displays

A. Asif[1,2], **H. Richter**[2], **and J. N. Burghartz**[1,2]

[1]Institut für Nano- und Mikroelektronische Systeme, Universität Stuttgart (INES), Elektrotechnisches Institut II, Pfaffenwaldring 47, 70569 Stuttgart, Germany
[2]Institut für Mikroelektronik Stuttgart (IMS), Allmandring 30A, 70569 Stuttgart, Germany

Abstract. System-in-Foil (SiF) is an emerging field of large-area polymer electronics that employs new materials such as conductive polymers and electrophoretic micro-capsules (E-Ink) along with ultra-thin and thus flexible chips. In flexible displays, the integration of gate and source drivers onto the flexible part increases the yield and enhances the reliability of the system.

In this work we propose a high-voltage Chipfilm™ lateral diffused MOS transistor (LDMOS) structure on ultra-thin single-crystalline silicon chips. The fabrication process is compatible with CMOS standard processing. This LDMOS structure proves to be well suited for providing adequately large switching voltages in spite of the thin ($<10\,\mu$m) substrate. A breakdown voltage of more than 100 volts with drain-to-source saturation current $I_{ds\,(sat)} \approx 85\,\mu A/\mu m$ for N-LDMOS and $I_{ds\,(sat)} \approx 20\,\mu A/\mu m$ for P-LDMOS is predicted through process and device simulations.

1 Introduction

Presently, the primary focus of electronic display industry is the large-area polymer electronics. This field employs new materials and techniques to build thin, bendable and high-resolution displays (Allen, 2005). The implementation of ultra-thin and thus flexible driver chips allows for improvements since such chips can be placed onto the flexible parts of the display, thus shortening the wiring length, and paving the way to larger flexible displays in the future.

A typical flexible display consists of a flexible substrate, an active matrix backplane, a layer with electrophoretic micro-capsules, and a transparent electrode. In the active matrix backplane an array of thin-film transistors (TFT) is used to provide the required voltage across each electrophoretic micro-capsule, according to an input address signal. In contrast to Si-bulk transistors, these TFT transistors require gate and drain voltages up to few tens of volts (Bai et al., 2007). In order to drive these thin-film transistors, source and gate driver circuits are required. These driver circuits are typically placed on the rigid part of the display near the edge, connecting to the TFT matrix through tape automated bonding (TAB). The drawback of this placement is that it increases the physical size and weight of the product. Moreover, the system also becomes unreliable especially in rugged environment. The integration of source and gate driver circuits onto the flexible part will reduce the length of the interconnects, as mentioned above.

Integration of organic, a-Si or poly-Si based transistors on flexible substrates can be achieved through large-area fabrication processes (Bock, 2005; Troccoli et al., 2006). An integrated source and gate driver chip using a-Si transistors has already been reported in Venugopal and Allee (2007). The low mobility of carriers in organic/a-Si/poly-Si based transistors, however, makes them unsuitable for high performance systems. Crystalline silicon transistors are better suited for efficient systems but the high processing temperatures required for their fabrication prevent from direct fabrication on flexible substrates. A solution comes from transferring pre-fabricated thin-film single-crystal silicon transistors onto flexible substrates (Li et al., 2006). Good resistance to fatigue and mechanical flexibility of pre-fabricated single-crystalline silicon MOSFETs on organic substrates has been reported in Li et al. (2006). But, most of the research work has focused on low-voltage single-crystal MOSFETs. The design of a thin-film high-voltage MOS (HVMOS) structure in single-crystalline silicon for flexible applications has not seen much attention yet due to unavailability of a suitable thin-chip technology.

The conventional scheme of a HVMOS is the lateral diffused MOS (LDMOS) transistor structure. This structure

Correspondence to: A. Asif
(aliasif@ims-chips.de)

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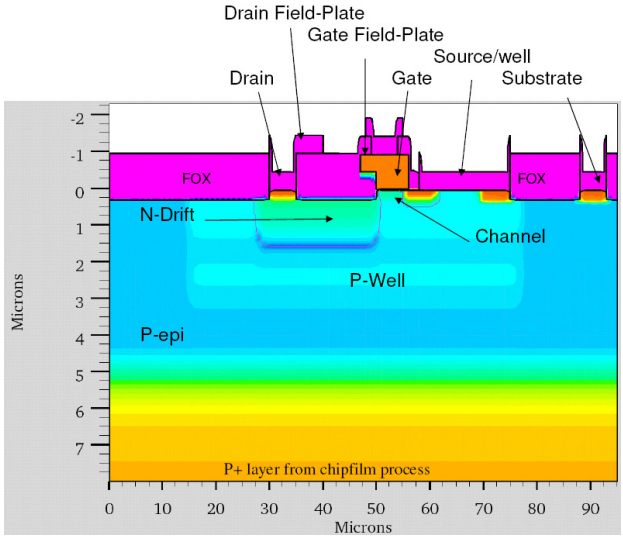
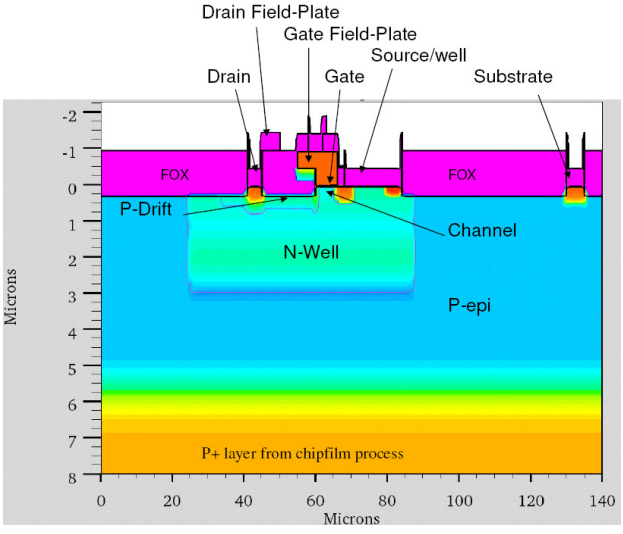


(a) The cross-section of a high-voltage N-LDMOS.



(b) The cross-section of a high-voltage P-LDMOS.

Fig. 1. Cross-sectional view of high-voltage Chipfilm™ LDMOS transistors.

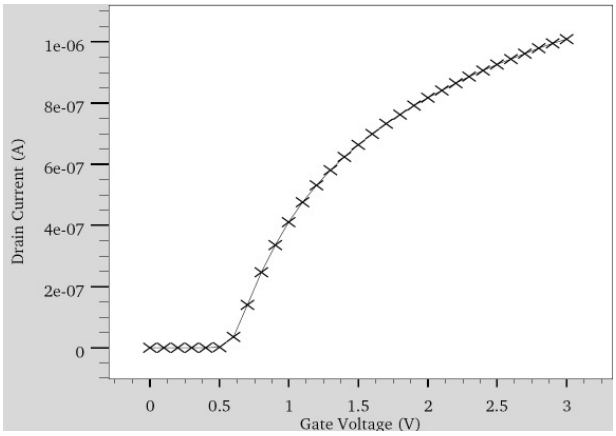
makes use of a drift region and a deep well to withstand high voltages (Sigg et al., 1972). RESURF technique (Ludikhuize, 2000) further enhances the efficiency of the device by increasing the breakdown voltage level. Other approaches could also be used for increasing the breakdown voltage and reduce the on-resistance R_{on}, such as double RESURF technique by using internal field rings, buried layers, triple well architecture and super-junction LDMOS transistors (Hossain et al., 2002; Nezar and Salama, 1991; Liaw et al., 2007; Puchner et al., 2007; Park and Salama, 2006). In literature, one can also find thin-film single-crystal silicon LDMOS structures but they use either Silicon on Insulator (SOI) (Akarvardar et al., 2007; Luo et al., 2003; Bawedin et al., 2004) or Silicon on Sapphire (SOS) (Roig et al., 2004) technologies.

In this paper, we propose a single-crystalline silicon based LDMOS transistor structure for flexible displays, built on a thin silicon chip with a breakdown voltage limit of more than 100 volts. The process steps are compatible with a CMOS standard process flow. We use the device in a high-voltage switch circuit for integrated source/data drivers and discuss the issue of efficiency enhancement.

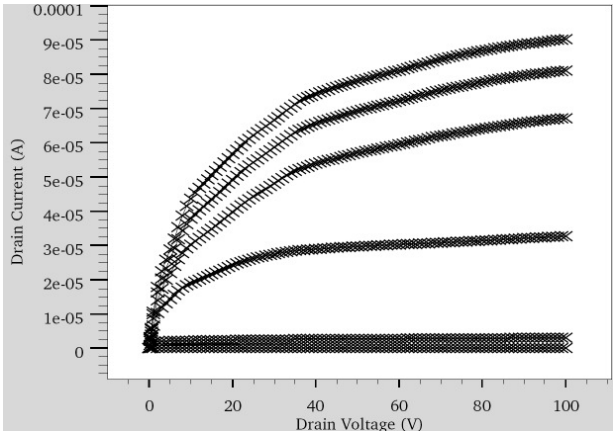
2 Device structure and fabrication

A SiF requires ultra-thin chips. A chip thinner than 20 μm has excellent flexibility and stability. The minimum bending radius, which is limited by the maximum strain of silicon, reduces toward smaller chip thickness. Thin chips result from post-process back-grinding of conventional CMOS wafers to the desired thickness. At thickness levels of a few tens of microns, post-process grinding is known to produce defects that propagate to the active regions at the chip surface. Also, the mechanical stability of back-grinded thin chips may be degraded by defect. The recently introduced Chipfilm™ technology circumvents these issues by pre-processing a wafer with buried cavities, which a piori define the chip thickness, prior to CMOS integration (Zimmermann et al., 2006). The Chipfilm™ process results in a p^+ backside layer having 1 μm–1.5 μm thickness, upon which the device structures can be fabricated. This is in contrast to thin-film SOI transistors where the device is fabricated on an insulator. A drawback of this p^+ layer is the out-diffusion into the epitaxial layer grown above. This out-diffusion takes place during the high temperature process steps e.g. well drive-in and field-oxide growth. The more the out-diffusion approaches the well-substrate junction the more the breakdown voltage limit is decreased. Therefore, the fabrication steps should be tailored for minimum thermal budget in order to minimize out-diffusion from p^+ layer.

The high-voltage thin-film LDMOS structure is developed and simulated by using the process simulator Athena from Silvaco. The cross-sectional views of high-voltage NMOS and PMOS transistors are shown in Fig. 1a and 1b. The conceptional structure of the device is identical to the conventional lateral diffused MOS (LDMOS) transistor having a RESURF structure and a drain field-plate. The drain field-plate helps in increasing the breakdown voltage limit and in reducing R_{on}. Both NMOS and PMOS transistors have identical effective channel length $\approx$3.5 μm and drift region length $\approx$15 μm. However, the drift region depth in PMOS is about 0.6 μm whereas in NMOS it is about 2.0 μm. The well depth is almost 3.0 μm. In this structure an optimised length of 5 μm for both drain field plate and gate field plate is used. Thickness of the gate oxide is 25 nm. The field oxide thicknesses under the gate field-plate and drain field plate are 0.8 μm and 1.5 μm, respectively.

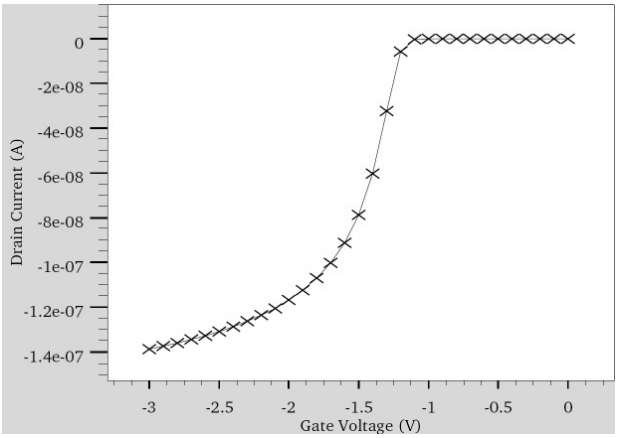


(a) Input characteristics of high-voltage Chipfilm™ N-LDMOS.

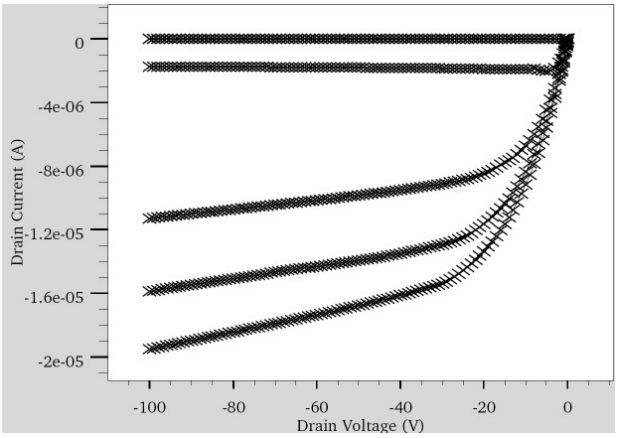


(b) Output characteristics of high-voltage Chipfilm™ N-LDMOS.

Fig. 2. Device characteristics of high-voltage Chipfilm™ N-LDMOS.



(a) Input characteristic curve of high-voltage Chipfilm™ P-LDMOS.



(b) Output characteristic curves of high-voltage Chipfilm™ P-LDMOS.

Fig. 3. Device characteristics of high-voltage Chipfilm™ N-LDMOS.

The fabrication process starts by growing a 7 μm thick p-type epitaxial layer over the p^+ layer. The epitaxial layer is grown in two steps, i.e. growth of a 5 μm thick epitaxial layer followed by a well implant and further growth of a 2 μm thick epitaxial layer, again followed by the same well implant. After well implantation, a drive-in step is done at 1150°C to attain a well depth of approximately 3 μm. Then, the drift-region implantation is performed followed by the field-oxide growth. The field-oxide growth step is done by etching trenches into silicon, growing a relatively thin field-oxide (∼100 nm) layer and then filling the trenches by depositing an oxide layer. The purpose of splitting the epitaxial growth into two parts and applying a trench formation for field-oxide is to reduce the overall thermal budget. The remaining process steps of gate-oxide growth, poly-gate deposition, source/drain region implant and metallization are very similar to the conventional CMOS process flow.

The current-voltage characteristics of the devices are obtained by using the device simulator Atlas from Silvaco. In Fig. 2a and 2b the input and output characteristics of high-voltage Chipfilm™ N-LDMOS are shown. Figure 3a and 3b show the input and output characteristic of a high-voltage Chipfilm™ P-LDMOS.

From Figs. 2a and 3a one can notice that P-LDMOS has a higher threshold voltage of about 1.2 volts compared to 0.6 volts for the N-LDMOS. This variation comes from the difference in doping density in the P-LDMOS channel ($\sim 10^{16}$ cm^{-3}) compared with that in the N-LDMOS channel ($\sim 10^{15}$ cm^{-3}). In Fig. 2b a quasi-saturation state appears between linear and saturation region. It is represented by a relatively straight line instead of a sharp edge during the transition from linear to saturation state. The quasi-saturation state appears because of velocity saturation. By changing

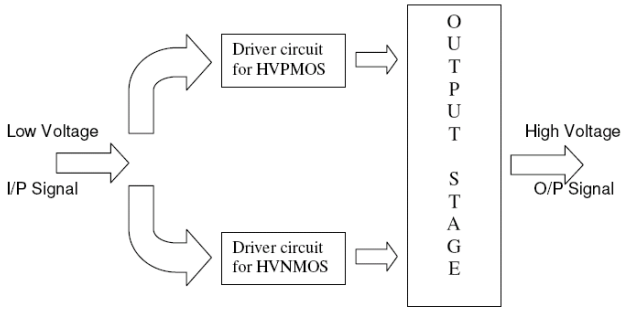


Fig. 4. Block diagram of high-voltage switch circuit topology.

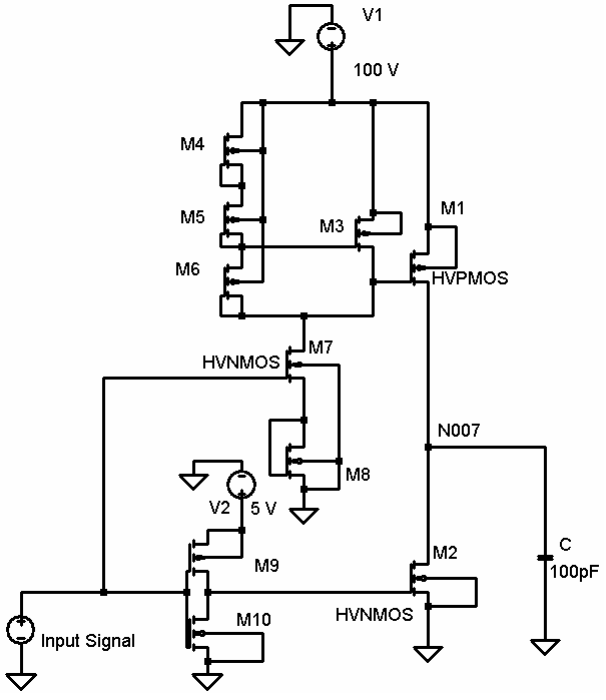


Fig. 5. Circuit diagram of the high-voltage switch. Transistors M1 and M2 constitute the output stage, transistors M3–M8 form the driver circuit for HVPMOS, transistors M9–M10 make driver circuit for HVNMOS. V_{dd} is a voltage source, input signal provides a square wave signal between 0–5 volts.

drift-region doping density and threshold adjustment implant this effect can be eliminated.

The electrical characteristics have shown that the proposed high-voltage Chipfilm™ LDMOS can provide sufficiently large switching voltages. Hence it can fairly well work as a high-voltage switch for the integrated source/data drivers of flexible displays.

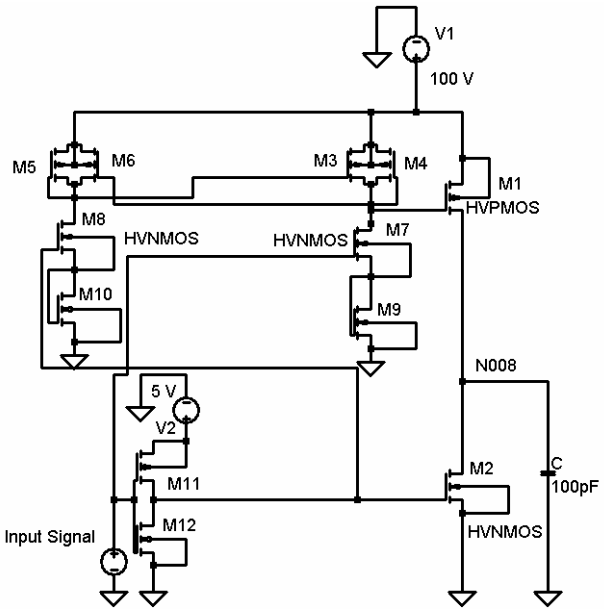


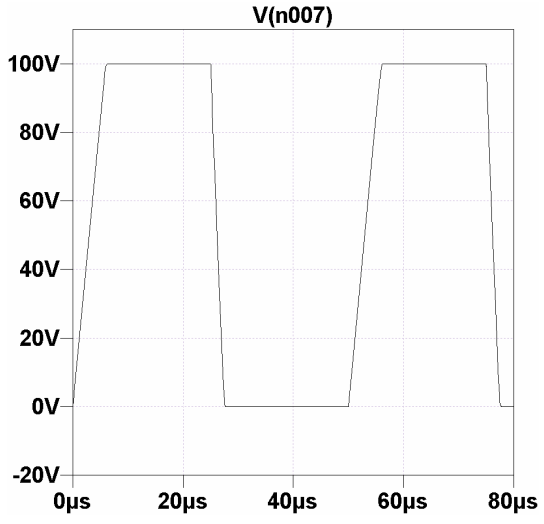
Fig. 6. Circuit diagram of high-voltage switch from literature (Declercq et al., 1993).

3 High-voltage switch for source/data drivers

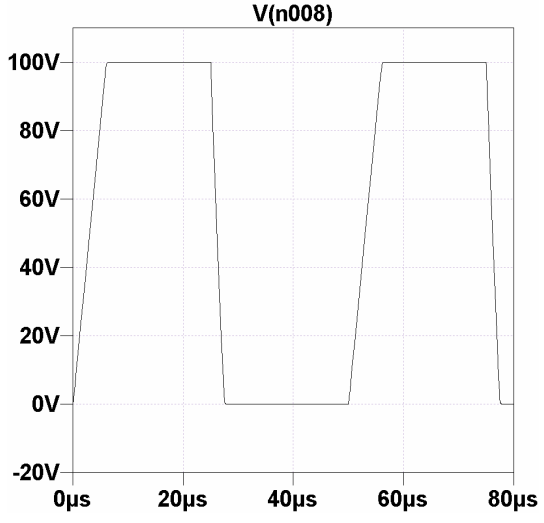
A complementary arrangement of MOS transistors is often used in the output stage of switching circuits. In high-voltage switches a level-shifter is required between the low-voltage input signal and the gate terminals of HVMOS transistors of the output stage. These level-shifters are designed with minimum static power dissipation, high-speed switching and minimum circuit-area, which directly influence the cost and yield figures of the product. In general one has to make a compromise between minimum circuit area and circuit efficiency.

A general circuit topology of a high-voltage CMOS switch is shown in Fig. 4. In this schematic a low-voltage input signal is directly and simultaneously applied to the driver circuits for the HVPMOS and HVNMOS of the output stage. These driver circuits ensure the required voltage levels according to the input signal at the gate terminals of HVPMOS and HVNMOS transistor of the output stage. The switch provides a high-voltage output signal in phase with the low-voltage input signal.

Figure 5 shows the circuit diagram of the high-voltage switch. Here, transistor M7 is used to drop most of the high-voltage across its drain-source terminals. M4 and M5 are long and narrow channel transistors, resulting in a high cannel resistance. This determines the current to primarily flow through M3, M7 and M8. Transistors M4 and M5, together with M6, are used to drive transistor M3. Transistors M3 and M8 will determine the amount of current through the driver circuit and the voltage level at the combined drain terminals of M3, M7 and M6.

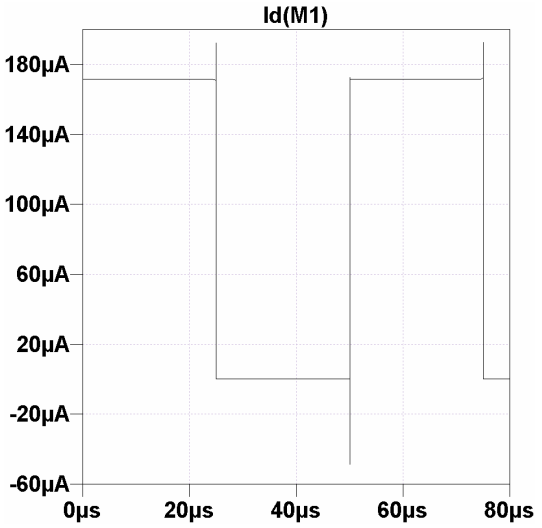


(a) Output signal of the circuit from Fig. 5.

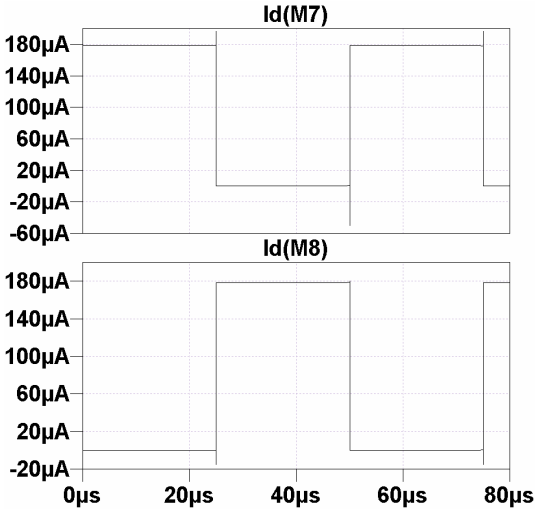


(b) Output signal of circuit taken from literature (Declercq et al., 1993).

Fig. 7. Output signal from high-voltage switches.



(a) Current through the driver circuit of HVPMOS of output stage from Fig. 5.



(b) Current through the driver circuit of HVPMOS of output stage from Declercq et al. (1993).

Fig. 8. Current through the driver circuit of HVPMOS transistors.

3.1 Performance comparison

In this section, we compare the performance of the circuit shown in Fig. 5 with that of another one reported in Declercq et al. (1993). The schematic of the circuit from literature (Declercq et al., 1993) is depicted in Fig. 6. Both use the same circuit topology illustrated in Fig. 4.

For the analysis and comparison of the performance of both circuits, we extract the parameters for high-voltage thin-film LDMOS transistor structures and fit them to a compact transistor model.

The transistor model is then used in LTSPICE simulation. The simulation is performed for an input signal frequency of 20 kHz and a load of 100 pF. The length and width of high-voltage LDMOS transistors for both P-LDMOS and N-LDMOS are set to L$\approx$3.5 μm and W$\approx$50 μm, respectively.

Figure 7a and 7b show the simulation results of the output signal of the circuit from Fig. 5 and the output signal of the circuit design from Declercq et al. (1993), respectively. It can be seen that both circuits are able to provide rail-to-rail voltage at the output terminal.

In the circuit from Fig. 5, a current of 180 μA flows during the first half cycle of the input signal whereas no current flows during the second half cycle (see Fig. 8a). That relates to an average current of 90 μA per cycle through the driver circuit of the HVPMOS.

Figure 8b illustrates the current through the driver circuit of the HVPMOS for the circuit from Declercq et al. (1993). The upper graph shows the current through driver circuit during the positive half cycle of the input signal whereas the lower graph shows the current during the negative half cycle. During both half cycles 180 μA current flows through the driver circuit. Thus, the average current over a complete cycle of input signal is also 180 μA.

Considering the transistor count, both circuits use the same number of transistors in the output stage and in the driver circuits of HVNMOS transistor. The only difference is in the driver circuit of the HVPMOS transistor, where the circuit from Declercq et al. (1993) uses two high-voltage LDMOS transistors. In contrast, the circuit from Fig. 5 has only one high-voltage LDMOS transistor (see Figs. 5 and 6). This shows that the circuit from Fig. 5 requires smaller circuit-area and dissipates less static-power compared to circuit from Declercq et al. (1993), thus making it more efficient.

4 Conclusions

We have developed a high-voltage Chipfilm™ LDMOS transistor structure on single-crystalline silicon for flexible electronic display. The process involved is compatible with CMOS standard processing. Simulation results showed that with a silicon film thickness of less than 10 μm, by using the Chipfilm™ process, the LDMOS structure has a breakdown voltage of more than 100 volts for both N-LDMOS and P-LDMOS transistor structures. This LDMOS structure proves to be well suited for use in a driver circuit chip on flexible display backplanes. It also provides adequately large switching voltages. The proposed device will significantly improve the performance of circuits on flexible substrates. Moreover, better circuit design of high-voltage switch for source/data drivers will further enhance the efficiency.

References

Allen, K. J.: Reel to Real: Prospects of flexible displays, P. IEEE, 93(8), 1394–1399, 2005.

Bai, Y., Liu, X., Chen, L., Ul-Haq, K., Khan, M. A., Zhu, W. Q., Jiang, X. Y., and Zhang, Z. L.: Organic thin-film field-effect transistors with MoO_3/Al electrode and OTS/SiO_2 bilayer gate insultaor, Microelectr. J., 38, 1185–1190, 2007.

Bock, K.: Polymer Electronics Systems – Polytronics, P. IEEE, 93(8), 1400–1406, 2005.

Troccoli, M. N., Roudbari, A. J., Chuang, T.-K., and Hatalis, M. K.: Polysilicon TFT circuits on flexible stainless steel foils, Solid State Electron., 50, 1080–1087, 2006.

Venugopal, S. M. and Allee, D. R.: Integrated a-Si:H Source Drivers for $4^{//}$ QVGA Electrophoretic Display on Flexible Stainless Steel Substrate, Journal of Display Technology, 3(1), 57–63, 2007.

Li, H. Y., Guo, L. H., Loh, W. Y., Bera, L. K., Zhang, Q. X., Hwang, N., Liao, E. B., Teoh, K. W., Chua, H. M., Shen, Z. X., Cheng, C. K., Lo, G. Q., Balasubramanian, N., and Kwong, D.-L.: Bendability of Single-Crystal Si MOSFETs Investigated on Flexible Substrate, IEEE Electr. Device L., 27(7), 538–541, 2006.

Sigg, H. J., Vendelin, G. D., Cauge, T. P., and Kocsis, J.: D-MOS Transistor for Microwave applications, IEEE T. Electron Dev., ED-19(1), 45–53, 1972.

Ludikhuize, A. W.: A review of RESURF Technology, in: Proc. Int. ISPSD Conf. 2000, 11–18, 2000.

Hossain, Z., Imam, M., Fulton, J., and Tanaka, M.: Double-resurf 700V N-channel LDMOS with Best-in-class On-resistance, in: Proc. Int ISPSD Conf. 2002, 137–140, 2002.

Nezar A. and Salama, C. A. T.: Breakdown Voltage in LDMOS Transistors Using Internal Field Rings, IEEE T. Electron. Dev., 38(7), 1676–1680, 1991.

Liaw, C.-W., Chang, C.-H., Lin, M.-J., King, Y.-C., Hsu, C. C.-H., and Lin, C. J.: P-Channel Lateral Double-Diffused Metal-Oxide-Semiconductor Field-Effect Transistor with Split N-Type Buried Layer for High Breakdown Voltage and Low Specific On-Resistance, Jpn. J. Appl. Phys., 46(7A), 4046–4049, 2007.

Puchner, H., Lee, S., Hinh, L., and Jang, J.: High Voltage LDMOS Transistors utilizing a Triple Well Architecture, Proc. of the 19th International Symposium on Power Semiconductor Devices and Ics, May 27–30, 2007, Jeju, Korea, 2007.

Park, I.-Y. and Salama, C. A. T.: Super Junction LDMOS Transistors, IEEE Circuit. Devic., 22(6), 10–15, 2006.

Akarvardar, K., Cristoloveanu, S., Bawedin, M., Gentil, P., Blalock, B. J., and Flandre, D.: Thin film fully-depleted SOI four-gate transistors, Solid State Electron., 51, 278–284, 2007.

Luo, J., Cao, G., Ekkanath Madathil, S. N., and De Souza, M. M.: A high performance RF LDMOSFET in thin film SOI technology with step drift profile, Solid State Electron., 47, 1937–1941, 2003.

Bawedin, M., Renaux, C., and Flandre, D.: LDMOS in SOI technology with very-thin silicon film, Solid State Electron., 48, 2263–2270, 2004.

Roig, J., Flores, D., Hidalgo, S., Rebollo, J., and Millan, J.: Thin-film silicon-on-sapphire LDMOS structures for RF power amplifier applications, Microelectr. J., 35, 291–297, 2004.

Zimmermann, M., Burghartz, J. N., Appel, W., Remmers, N., and Burwick, C.: A seamless Ultra-Thin Chip Fabrication and Assembly Process, IEEE International Electron device meeting 2006, 1–3, 2006.

Declercq, M. J., Schubert, M., and Clement, F.: 5V-to-75V CMOS Output Interface Circuits, IEEE International Solid State Conference 1993, 162–163, 1993.