Non-linear behaviour of charge-pump phase-locked loops

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Abstract. The analysis of the mixed analogue and digital structure of charge-pump phase-locked loops (CP-PLL) is a challenge in modelling and simulation. In most cases the system is designed and characterized using its continuous linear model or its discrete linear model neglecting its non-linear switching behaviour. I.e., the time-varying model is approximated by a time-invariant representation using its average dynamics. Depending on what kind of phase detector is used, the scopes of validity of these approximations are different. Here, a preeminent characterization and simulation technique based on the systems event-driven feature is presented, merging the logical and analogue inherent characteristics of the system. In particular, the high-grade non-linear locking process and the dead-zone are analyzed.

1 Introduction

Phase-locked loops (PLL) are widely used and can be utilized to synchronize an oscillator in phase and frequency. If the PLL is absolutely synchronized, the phase error between the input signal and the oscillator signal is minimal. As soon as a phase error occurs, the oscillator will be readjusted until the phase error is again minimal (Gardner, 1980, 1966; Best, 1993; Shu and Sanchez-Sinencio, 2005). Depending on what kind of phase detector (PD) is used, the lock margin sensitively varies (Best, 1993; Wolaver, 1991). If the PLL is stable and the loop bandwidth is wide enough, the locked system has a dynamic, which can be described by an averaged/linearized model. By using a tri state phase and frequency detector (PFD), the PLL is locked if the absolute phase error remains smaller than 2π (Best, 1993; Wolaver, 1991; Den Dulk, 1988). Generally, there are two operating

ranges in CP-PLL systems: the linear operating range and the non-linear operating range. The linear operating range is defined by the linear model of the PLL and can be assigned as that range where the PLL is locked. Even if the PLL is locked and all non-idealities (dead-zone, non-linear characteristic of the VCO etc.) are neglected, the PLL possesses a weak non-linear behaviour caused by the logical switching of the PFD. Furthermore, while the PLL is out-of-lock, the system shows a high-grade non-linear behaviour. The non-linear operating range is also called the pull-in range. For this purpose, the PLL is characterized by considering the switching of the PFD. In addition a new lock detection circuitry delivering reliable information about the status of the output clock signal is presented. This is a direct consequence of the characterization of the switching behaviour. The proposed method monitors and detects when the phase error between the reference and the synthesized output clock leaves (out-of lock) or enters (locked) the phase and frequency detector's linear range ($\varphi_e \in [-2\pi, 2\pi]$). For this, the digital information of the PFD monitoring the closed loop is scanned along the transient progress of the system. We will focus here on the case of a tri state PFD. A methodology is presented, which allows to identify and to characterize a CP-PLL by means of its inherent non-linear switching behaviour.

Beside the switching of the PLL, another non-linearity is considered and characterized. The dead-zone due to the PFD and the charge-pump, mostly considered as a static non-linearity embedded into the linear continuous approximation, represents a dynamic non-ideality caused by the delays of the PFD's logic and the charge-pump's slew-rate (Hedayat et al., 1999). An advanced PFD model for accurate simulations of CP-PLL systems is presented.

In Sect. 2.1 the general structure of the CP-PLL is envisaged. Section 2.2 presents the continuous linear model of a second order high-gain phase-locked loop. The non-linear behaviour (without non-idealities) and the linear model are compared and characterized in Sect. 2.3. For this, special
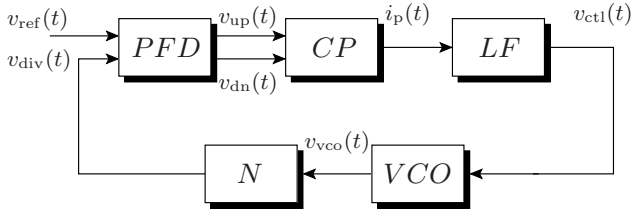
Fig. 1. Schematic representation of a charge-pump phase-locked loop.

Fig. 2. Finite state machine of the phase and frequency detector driven by the falling edges of the reference signal $v_{\mathrm{ref}}(t)$ and the VCO or the divider output signal $v_{\mathrm{vco}}(t)$ respectively $v_{\mathrm{div}}(t)$.

PFD state sequences are considered. The last subsection of Sect. 2 is dedicated to a particular non-linearity. A behavioural non-linear model of the dead-zone is introduced. In Sect. 3 a direct implication (application) of Sect. 2.3 is presented.

2 Modelling

The PLL offers various models and various non-linearities. In the following, the main focus is pointed upon the non-linear behaviour of the PFD. For this, the switching properties and the linear model are compared. Additionally, an advanced PFD model is introduced.

2.1 Architecture

For simplicity, an integer-N PLL frequency synthesizer architecture is considered (see Fig. 1). The PLL consists of five functional blocks.

- **PFD:** The phase and frequency detector is a purely digital device having two output signals ($v_{\mathrm{up}}(t)$ and $v_{\mathrm{dn}}(t)$) and is driven by the falling (or rising) edges of its input signals (reference signal $v_{\mathrm{ref}}(t)$ and VCO signal $v_{\mathrm{vco}}(t)$ [if no divider is used] respectively the divider output signal $v_{\mathrm{div}}(t)$) estimating the phase error between $v_{\mathrm{ref}}(t)$ and $v_{\mathrm{vco,div}}(t)$.

- **CP:** The charge-pump delivers a current $i_{\mathrm{p}}(t)$, driven by the PFD outputs $v_{\mathrm{up}}(t)$ and $v_{\mathrm{dn}}(t)$.

- **LF:** The loop filter is a low-pass filter, which converts the current i_{p} into a voltage $v_{\mathrm{ctl}}(t)$ filtering the alternating current component.

- **VCO:** The oscillating output $v_{\mathrm{vco}}(t)$ of the VCO is controlled by the loop filter's output voltage $v_{\mathrm{ctl}}(t)$.

- **N:** The divider is a periodic or a modulo N counter, allowing frequency multiplication $f_{\mathrm{vco}} = f_{\mathrm{div}} \cdot N$.

2.2 Linearized continuous model

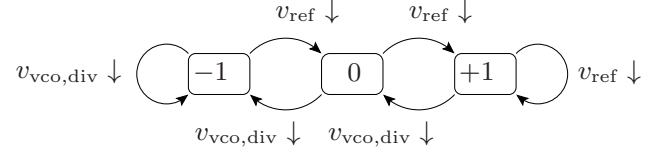It is assumed, that the system is stable. This is mainly assured when the denominator of the following phase transfer function (second order PLL) is hurwitzian and the reference frequency f_{ref} is notably higher than the loop natural frequency $f_{\mathrm{n}} = \omega_{\mathrm{n}}/(2\pi)$ (Gardner, 1980). In general, it can be said, that if a second order CP-PLL is locked (the absolute phase error $|\varphi_{\mathrm{e}}|$ remains smaller than 2π), the linear continuous approximation can be used to describe the average dynamic behaviour. It holds

$$H(s) = \frac{2\zeta\omega_{\mathrm{n}}s + \omega_{\mathrm{n}}^2}{s^2 + 2\zeta\omega_{\mathrm{n}}s + \omega_{\mathrm{n}}^2}, \tag{1}$$

where

$$\zeta = \frac{R_1 C_1}{2}\omega_{\mathrm{n}} \tag{2}$$

denotes the damping factor and $\omega_{\mathrm{n}} = \sqrt{K/C_1}$ represents the natural frequency, where $K = K_{\mathrm{v}}I_{\mathrm{p}}$ is called the loop gain. Obviously, the linear model can not describe the non-linear pull-in process.

2.3 Non-linear model and characterization

In the following, the non-linear signature of the switched differential equation system caused by the finite state machine is characterized. For this, the VCO is considered as an ideal integrator. Non-idealities like dead-zone and non-linear characteristic of the VCO are neglected. With this assumption, the only non-linearity of the loop is related to the switching behaviour of the digital PFD. The traditional PFD (tri state PFD) is a sequential circuit, driven by the falling or rising edges of its input signals (reference signal v_{ref} respectively divider signal $v_{\mathrm{vco,div}}$, where the subscripts "vco" or "div" denote a PLL without divider respectively with divider). In a more abstract view, the PFD can be represented by a finite state machine consisting of three states. Figure 2 shows the state graph of the PFD, driven by a given type of edges (falling edges or rising edges of v_{ref} and $v_{\mathrm{vco,div}}$). The states of the PFD are represented by the logical output signals v_{up} and v_{dn} and can be defined with $\{v_{\mathrm{up}} = 0; v_{\mathrm{dn}} = 1\} \hat{=} \mathcal{S}_{-1}$, $\{v_{\mathrm{up}} = 0; v_{\mathrm{dn}} = 0\} \hat{=} \mathcal{S}_0$ and $\{v_{\mathrm{up}} = 1; v_{\mathrm{dn}} = 0\} \hat{=} \mathcal{S}_{+1}$. It is obvious, that the charge-pump is controlled by these states, i.e. by the PFD output signals v_{up} and v_{dn}. The interrelation between the states of the PFD and the solution of the differential equation of the switching system is presented in Eqs. (3) and (5).

$$\boldsymbol{x}_{\mathrm{n}+1} = \boldsymbol{\Phi}(t_{\mathrm{n}} - t_{\mathrm{n}+1})\boldsymbol{x}_{\mathrm{n}} +$$
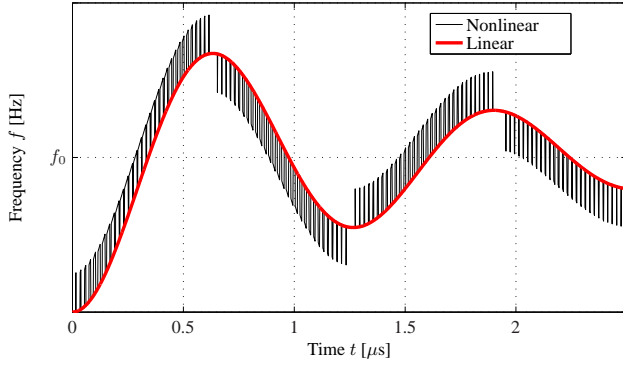
Fig. 3. While the second order PLL delivers a phase error between $-2\pi < \varphi_e < 2\pi$ the PLL is called locked and the linear approximation provides a good average conformity.

$$\int_{t_n}^{t_{n+1}} \boldsymbol{\Phi}(t_n - \tau) \boldsymbol{b} i_p(\mathcal{S}(\tau)) \mathrm{d}\tau \qquad (3)$$

$\boldsymbol{\Phi}(\cdot)$ represents the matrix exponential of the state matrix, $\boldsymbol{b}$ is the control vector, the vector $\boldsymbol{x}$ is denoted as the vector of state variables and $i_p(\mathcal{S}(\tau))$ is the charge-pump current controlled by the states $\mathcal{S}(\cdot)$ of the PFD, where $\mathcal{S}(\cdot) \in \{\mathcal{S}_{+1}, \mathcal{S}_0, \mathcal{S}_{-1}\}$ and is controlled by the reference signal $v_{\mathrm{ref}}(t)$ and the output signal $v_{\mathrm{vco,div}}$. Therefore, $\mathcal{S}(\tau)$ is a function of $v_{\mathrm{ref}}(\tau)$ and $v_{\mathrm{vco,div}}(\tau)$:

$$\mathcal{S}(\tau) = \mathcal{S}(v_{\mathrm{ref}}(\tau), v_{\mathrm{vco,div}}(\tau)) \qquad (4)$$

Obviously, there are three states modulating the charge-pump current into three constant values. It holds $i_p(\mathcal{S}(\tau)) \in \{+I_p, 0, -I_p\}$. Thus, Eq. (5) results:

$$\boldsymbol{x}_{n+1} = \boldsymbol{\Phi}(t_n - t_{n+1})\boldsymbol{x}_n + \begin{cases} +I_p \int_{t_n}^{t_{n+1}} \boldsymbol{\Phi}(t_n - \tau)\boldsymbol{b}\mathrm{d}\tau & , \mathcal{S}_{+1} \\ 0 & , \mathcal{S}_0 \\ -I_p \int_{t_n}^{t_{n+1}} \boldsymbol{\Phi}(t_n - \tau)\boldsymbol{b}\mathrm{d}\tau & , \mathcal{S}_{-1} \end{cases} \qquad (5)$$

By using a first order passive $R - C$ loop filter (Gardner, 1980; Hedayat et al., 1997; Daniels and Farrell, 2008), a second order loop results.

As it can be observed on Fig. 3, when the loop is locked (i.e. the absolute phase error $|\varphi_e|$ remains smaller than 2π) and stable with a reference frequency f_{ref} notably higher than the loop natural frequency, the linearized continuous-time model represents a good approximation of the average behaviour. In addition to the damped sinusoidal dynamics, the non-linear model possesses a comp-shaped behaviour (illustrated in Fig. 3). This comb-shaped structure indicates the state $\mathcal{S}(t)$ of the PFD. The heights of the peaks is correlated to the product of the loop filters resistor R_1 and the charge-pump current $i_p(\mathcal{S}(\tau))$. All the peaks of the comb-shaped structure directed upwards are associated to the logical state $\mathcal{S}_{+1}$. The peaks directed downwards are related to
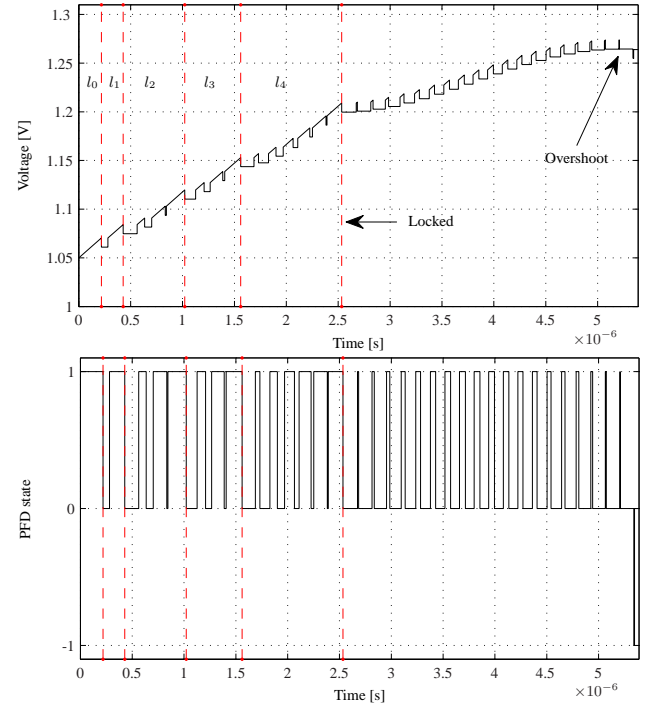

Fig. 4. The pull-in process is divided into five ranges l_i ($i \in \{0, 1, 2, 3, 4\}$) and the course of events of the PFD's states $\mathcal{S}$.

the PFD state $\mathcal{S}_{-1}$. When the linear model matches with the non-linear one, the PFD is at the state $\mathcal{S}_0$. Considering Fig. 3 two state sequences can be identified. The PFD sequence corresponding to a digital overshoot is defined as

$$\mathcal{S}_\uparrow = \{\mathcal{S}_{+1}, \mathcal{S}_0, \mathcal{S}_{-1}\}, \qquad (6)$$

where the subscripted down arrow emphasizes the direction and the state sequence of a digital undershoot is defined as

$$\mathcal{S}_\downarrow = \{\mathcal{S}_{-1}, \mathcal{S}_0, \mathcal{S}_{+1}\}. \qquad (7)$$

Generally an overshoot or an undershoot occurs if the damping ζ is less than 1.2. In the case of a third order or a high order PLL system (the second order filter consists of the first order passive loop filter with a parallel smoothing capacitor, see Shu and Sanchez-Sinencio, 2005; Hedayat et al., 1999), the state sequences $\mathcal{S}_\downarrow$ and $\mathcal{S}_\uparrow$ do not identify the real frequency f_{vco} (voltage v_{ctl}) overshoot or undershoot. Only zero crossings of the phase error φ_e are detected by these state sequences, because the phase and frequency detector operates on the phase of the reference (v_{ref}) and divider (resp. VCO) output signal ($v_{\mathrm{vco,div}}$). For this reason, the logical signature can be used for characterizing the dynamic behaviour of the PLL.

While the PLL is out-of-lock (phase error $|\varphi_e| > 2\pi$), the linear model is no more valid. Therefore the pull-in process has to be analyzed by means of the non-linear pulse width modulated (PWM) model (see Eq. 5). It is obvious, that the
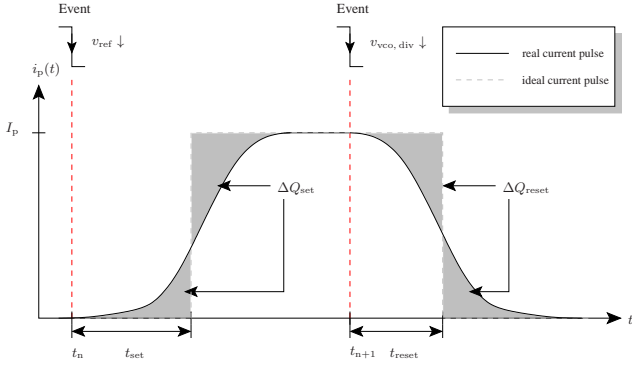
Fig. 5. Charge-pump current with slew-rate and delay propagation from the inputs of the PFD to the output of the charge-pump.

state signal $\mathcal{S}(t)$ is a PWM signal (see Fig. 4). The wider the pulse width is, the bigger is the absolute phase error $|\varphi_e|$ (detected by the PFD). The detectable phase error is limited by the PFD, even if any frequency can be theoretically reached. Thus, a phase error of $|\varphi_e| = 2\pi$ is equivalent to the occurrence of two successive falling edges of the reference signal v_{ref}, respectively the output or divider signal $v_{vco,div}$. Hence, two important state sequences can be identified, where

$$\mathcal{S}_{\not\downarrow} = \{\mathcal{S}_-, \mathcal{S}_-\} \tag{8}$$

and

$$\mathcal{S}_{\not\uparrow} = \{\mathcal{S}_+, \mathcal{S}_+\} \tag{9}$$

are denoted as cycle slips of the down branch ($\mathcal{S}_{\not\downarrow}$) respectively of the up branch ($\mathcal{S}_{\not\uparrow}$). The pull-in process is shown in Fig. 4, where five ranges are emphasized and labeled with l_i ($i \in \{0, 1, 2, 3, 4\}$). Evidently, if the last cycle slip occurs, the PLL is locked and the absolute phase error remains less than 2π. By considering the logical outputs of the PLL, the transient behaviour can be monitored, without observing the analogue outputs. Assuming that a cycle slip is identified and an overshoot (undershoot) appears subsequently, the PLL is locked. However, the occurrence of an overshoot or an undershoot does not imply, that the PLL is locked. If there is no knowledge in terms of a detected cycle slip, an overshoot and an undershoot must be identified. To ensure that the PLL is locked, one of the following state sequences must be detected:

$$\mathcal{S}_\circ = \{\mathcal{S}_\downarrow, \mathcal{S}_\uparrow\} \vee \{\mathcal{S}_\uparrow, \mathcal{S}_\downarrow\} \vee \{\mathcal{S}_{\not\downarrow}, \mathcal{S}_\downarrow\} \vee \{\mathcal{S}_{\not\uparrow}, \mathcal{S}_\uparrow\}. \tag{10}$$

2.4 Dead-zone

Ideally, the PFD can be modelled as a finite state machine (see Fig. 2), consisting of three states and operating on the triggering edges (falling or rising edges) of the input signal v_{ref} and the divider output signal v_{div} (or the VCO output signal v_{vco} when the feedback comprises no divider). Every state machine can be realized by using flip-flop circuits.
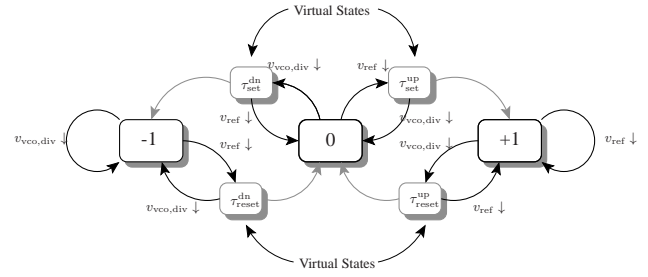

Fig. 6. Modified PFD model describing delay propagation from the inputs to the output.

Thus, the PFD operates by setting and resetting the flip-flops with the incoming signals v_{ref} and v_{div} (v_{vco}). While a triggering edge is identified, the PFD is not able to change the state (the current) instantaneously. Thus, the flip-flop is set by the triggering edge. But, when the phase error is small, the second triggering edge will reset the flip-flop before the signal has been propagated to the output. Correspondingly, the phase error between the incoming signals will not arise at the PFD output (respectively the charge-pump output). Beside the presented delay propagation from the inputs to outputs of the PFD, the waveform cannot offer edges with an infinite slope. Thus, a different charge is injected to the loop filters capacitance compared to the ideal charge injection. A schematic waveform is viewed in Fig. 5, describing the delay propagation and the charge injection. The aspect of the delay propagation can be modelled introducing virtual states within the state machine. If the charges ΔQ_{set} and ΔQ_{reset} are equal to zero, the new state machine (see Fig. 6) can be used for accurate simulations of the non-linear behaviour. If $\Delta Q_{set} \neq 0$ and $\Delta Q_{reset} \neq 0$, the discrepancy of the charge injection to the loop filter's capacitance can be interpreted as the decrease or the increase of the current pulse integration and therefore this can be modelled as a time delay.

The modified PFD model described in Fig. 6 represents a simple possibility to include the non-linear characteristic of the dead-zone into the simulation model of Eq. (3) or into the event-driven modelling techniques (see Hedayat et al., 1997, 1999; Van Paemel, 1994).

3 Application and simulation

Conventional digital lock detection techniques are based on counting methods. These methods are heuristic procedures based on the maximum lock time and the maximum settling time. Because of this, for every application a new counter has to be designed. Additionally, the locking point and settling point in time is increasing if the frequency step applied to the system is increasing. Using an identification algorithm of the presented state sequences (see Eq. 10), a simple purely digital lock and settling detection circuitry can be developed. The circuit is divided into three subcircuits, identifying the
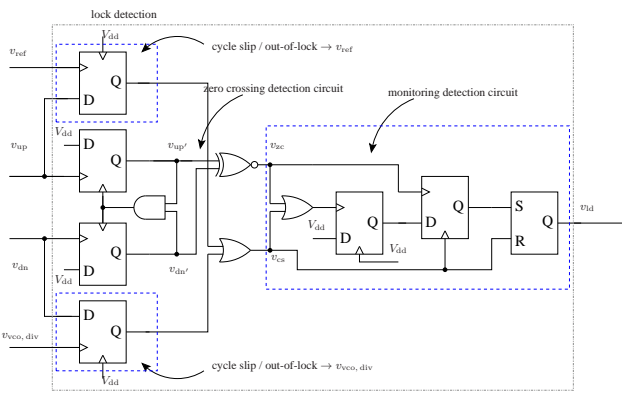
Fig. 7. Schematic representation of the monitoring circuit based on the state sequence identification.

Fig. 8. Course of events of the important lock detection signals and the VCO control voltage v_{ctl} of a third order CP-PLL.

state sequences of Eq. (3). The cycle slip (out-of-lock) detection circuit consists of two D-flip-flops and an OR gate (see Fig. 7). Assuming that the UP signal v_{up} (resp. the DN signal v_{dn}) is true, the occurence of a reference (resp. output) triggering edge makes the $v_{\mathrm{up'}}$ (resp. $v_{\mathrm{dn'}}$) to be set to one. This situation $\{v_{\mathrm{up}} = 1, v_{\mathrm{up'}} = 1\}$ (resp. $\{v_{\mathrm{dn}} = 1, v_{\mathrm{dn'}} = 1\}$) corresponds to a phase error larger than 2π and the PLL is considered as out-of-lock. The zero crossing detection circuit is depicted in Fig. 7. This circuit is like a conventional tri state PFD, where its outputs are combined through an exclusive OR gate. It appears that $v_{\mathrm{up'}}$ (resp. $v_{\mathrm{dn'}}$) can be understood as the envelope of v_{up} (resp. v_{dn}). More precisely, these envelopes are used as inputs of the exclusive OR gate and thereby make it possible to detect zero crossing of the phase error (digital overshoot or undershoot).

The lock detection monitoring circuit (see Fig. 7) is driven by the outputs of the cycle slip (out-of-lock) detection circuit and the zero crossing detection circuit. This monitoring circuit consists of two D flip-flops, an RS flip-flop and an OR gate and verifies Eq. (3). In Fig. 8 a Cadence/Spectre Simulation with 90nm technology of ST-Microelectronics of a third order CP-PLL is presented. By means of the proposed lock detection circuit, the digital information delivers a simple possibility to track the transient behaviour of the VCO control voltage v_{ctl} (resp. the output frequency f_{vco}) and the dynamics of the system. The control voltage and the important logical outputs of the detection circuitry are depicted in Fig. 8. The lock detection circuit delivers three important signals: phase zero crossing detection v_{zc}, cycle slip detection v_{cs} and lock detection v_{ld}.

4 Conclusions

In this work the non-linear behaviour of a charge-pump phase-locked loop was characterized and modelled. The focus was pointed upon the digital phase and frequency detector, i.e. the switchi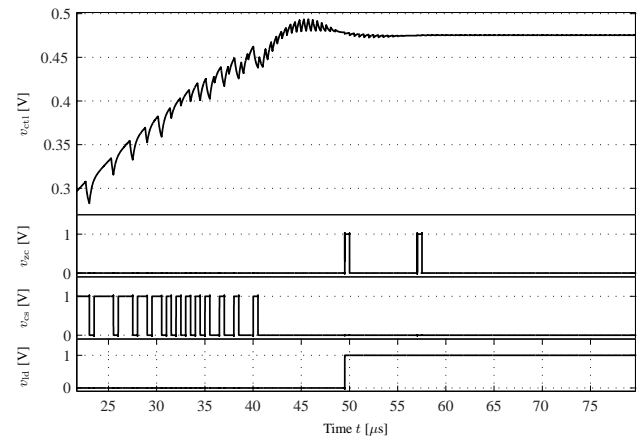ng signature, the dead-zone of the PFD and the charge-pump. An accurate model of the non-linear PFD was presented for efficient simulations of mixed signal systems within event-driven modelling techniques. In addition, a simple and robust lock detection circuit based on monitoring zero crossing (overshoot/undershoot) events and cycle slip identification was presented, by using only the digital information of the system (i.e. the input and output signals of the phase and frequency detector).

Furthermore, the detection circuit can be used to implement fast locking phase-locked loops with course and fine tuning elements. Further work will focus in the optimization and an the further developement of the event-driven and non-linear modelling and simulation techniques for accurate and efficient design methodologies.

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