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Advances in Radio Science

Network model of on-chip antennas

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Abstract. A Network model of an ultra-wide band, intra-chip wireless link is presented. Numerical data of Z-parameters, obtained from full wave simulation of the structure, are used to obtain a rational function representation via the Vector Fitting procedure. Brune's circuit synthesis is applied to generate the network model from rational functions.

1 Introduction

Today CMOS technology allows to realize monolithic integrated front-ends for wireless communication links up to millimeterwave frequencies. Due to the small dimensions of antennas on-chip integration of antennas for inter-chip and intra-chip communication becomes an interesting option. Network models of the communication links generated from electromagnetic full-wave simulation data are a valuable tool for circuit and system design.

In this work we describe the systematic generation of a lumped element network model of an intra-chip wireless communication link formed by integrated antennas. To save chip area the antenna electrodes are also used as the ground planes of the integrated circuitry operating in a frequency band below the carrier frequency of the wireless link.

In the following, we shall describe the detailed design of the antennas, and how they are decoupled from the rest of the CMOS circuitry. Then the Brune's synthesis of a lumped element equivalent circuit is described. We conclude by comparing the results generated by the circuit model and full-wave electromagnetic simulation.

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2 Structure

The structures, which have been modelled in the present work, are monolithically integrated antennas for chip-to-chip communication (Yordanov, 2008; Yordanov and Russer, 2010; Yordanov, 2010). The antenna design is based on the sharing of on-chip elements between the integrated circuit and the antenna in order to save chip area. This has been obtained by cutting the top-most metallisation layer of the chip into patches and exciting the patches in antenna mode. Inductive connections between the patches provides the DC connection, required for the CMOS circuitry.

A cross-section view of such an antenna is presented in Fig. 1. The substrate is high-resistivity silicon ($\rho > 1000\,\Omega\,\mathrm{cm}$), required to reduce the dielectric losses of the radiated filed. The thickness of the substrate is 675 µm. The rare side of the substrate is covered by a ground plane (not shown in the figure). On top of the high-resistivity substrate a 3 µm layer of low-resistivity silicone is manufactured, as required by the CMOS technology. The active elements are contained in this layer. A top follow several metallisation layers with the CMOS interconnects, embedded in SiO_2. The total thickness of the interconnection layers is 5–8 µm. The top metallisation layer contains the ground supply plane, which is cut into patches. A microwave generator is connected across the gap between the patches, thus exciting the antenna mode.

The metallisation layers, containing the CMOS interconnects, have a total thickness of about 5 µm, which is orders of magnitude smaller than the wavelength of the antenna mode (Yordanov and Russer, 2010). Therefore the interconnects, located underneath the patches, do not influence the antenna field and do not need to be included in the numerical simulation, thus reducing significantly the computational effort. This simplification can be made, as long as there are no interconnects, located in the gap between the patches, since they effectively short-circuit the gap and interfere with the antenna field. Such cases are not investigated in this work.

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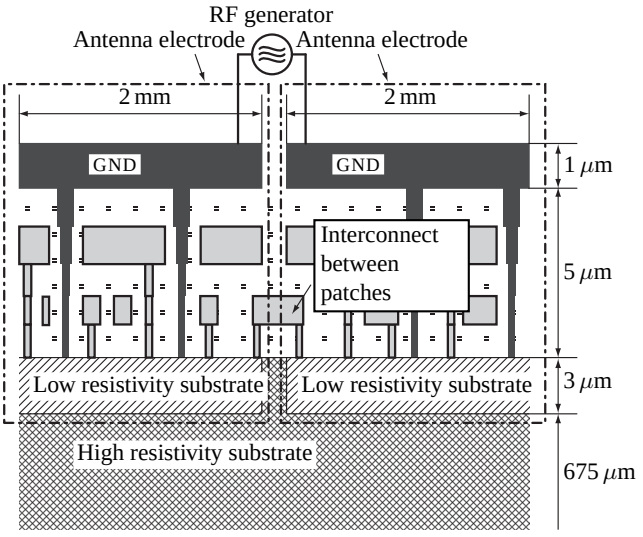

Fig. 1. Cross-section view of integrated on-chip antenna, using the ground planes as antenna electrodes. The separated areas of the ground planes have to be connected to each other using inductive connections. The RF generator is also integrated in the CMOS circuit. Figure is not to scale.

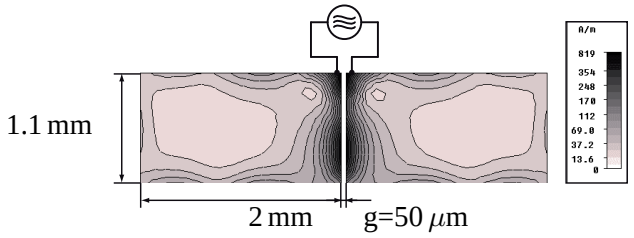

Fig. 2. Top view and current distribution of a two patch antenna, operating at 66 GHz.

Figure 2 shows the geometry and the current density distribution of a two-patch antenna, operating at 66 GHz. The current is concentrated in the vicinity the gap and is directed along the gap. This shows that the wave emerging from the generator is transmitted along the slot and reflected from the open-circuited end of the gap, thus creating a standing-wave pattern between the patches. This pattern generates the radiated field of the antenna. Figure 3 shows fabrication of two antennas on one chip with a distance of 2 mm between them.

3 Procedure

Network modelling was carried out in four steps. The first step is *Data Acquisition*. The transient solver of CST® was used to calculate S-parameters and Z-parameters. Care was taken to ensure that the data was positive real (P.R.). At each point of frequency, the real part of the Z-parameters matrix should be positive definite, for the function to be

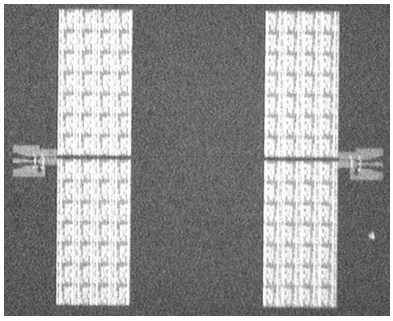

Fig. 3. Fabrication of integrated antennas with distance of 2 mm.

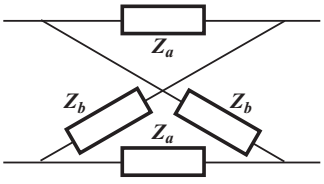

Fig. 4. Lattice structure for symmetric two port.

P.R. i.e. if $\mathbf{R} = \Re[\mathbf{Z}]$, then $R_{11} \geq 0$, $R_{22} \geq 0$ and $|\mathbf{R}| \geq 0$. For the achievement of P.R. data, finer mesh size of structure was taken and simulation was run for more time steps.

This is followed by *decomposing the two-port data* into one-port data. This is done by using a lattice structure shown in Fig. 4 and using equations

$$Z_a = Z_{11} - Z_{12}$$
$$Z_b = Z_{11} + Z_{12} \quad (1)$$

Third step is to find a proper rational function describing the data. Vector Fitting(V.F.) Method (Gustavsen, 1999, 2006; Deschrijver, 2008) is used to find poles and residues for curve fitting. It should be kept in mind that V.F. method is a mathematical tool providing the poles giving best fit. Thus the rational function obtained is valid in given range of frequency.

Last step is *network synthesis* of the rational function. This can be accomplished in number of ways. Authors have adopted Brune's circuit synthesis procedure as it is extendable to arbitrary number of ports (Tellegen, 1953).

4 Results

Figure 5 show a general schematic description of impedances Z_a and Z_b of Fig. 4. Each one-port consists of N stages which are one of the circuits depicted in Fig. 6. The number of poles for Z_a and Z_b were 17 and 21, respectively.

The circuits were simulated in SPICE and Z-parameters are compared in Figs 7 and 8.

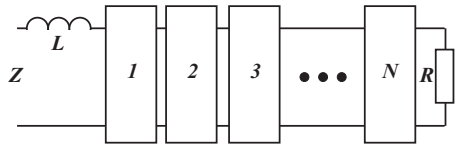

Fig. 5. Overall Circuit Representation.

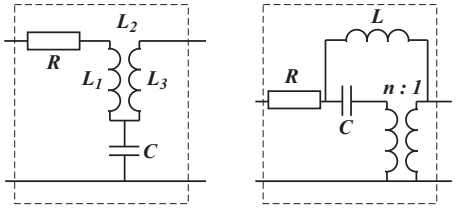

Fig. 6. Circuit within each stage of whole network.

5 Conclusions

An accurate model of intra-chip antennas is presented. The results obtained from full wave simulation of structure, simulation of network model and from measurements are compared.

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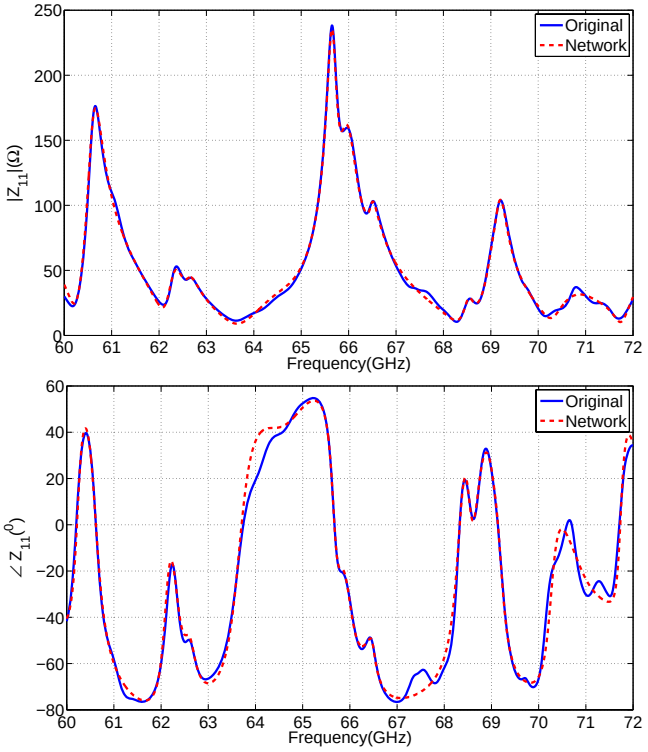

Fig. 7. Comparision of magnitude and phase of Z_{11}.

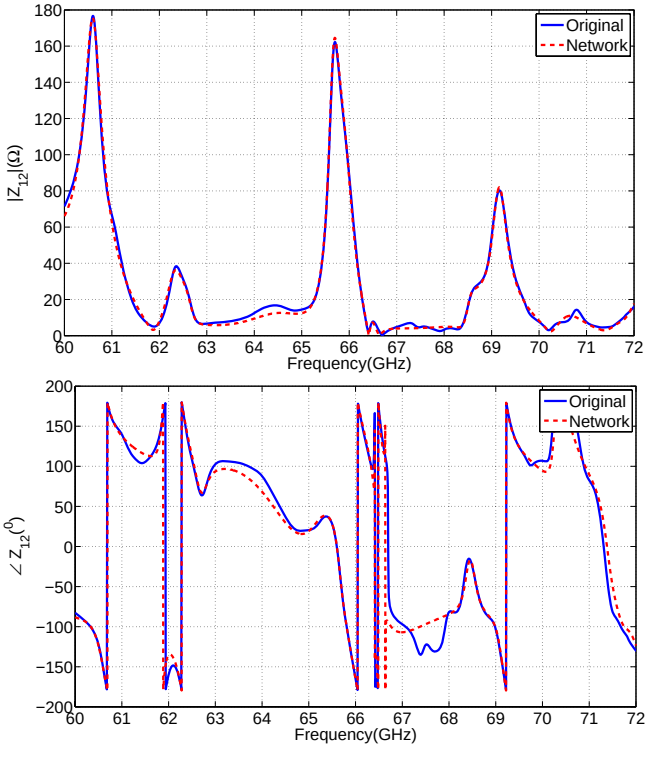

Fig. 8. Comparision of magnitude and phase of Z_{12}.