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# Fully-integrated LDO voltage regulator for digital circuits

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**Abstract.** Low-dropout (LDO) voltage regulators are widely used to supply low-voltage digital circuits. For recent ultra-low-power microcontroller systems, a fully-integrated LDO without any external capacitance is preferred in order to achieve a fast and energy-efficient wake-up.

Commonly, an LDO is specified, designed and verified for DC load currents. In contrast, a digital load creates large current spikes. As an LDO designed for low quiescent current is too slow to react on fast current spikes, a minimum on-chip capacitance is required to keep the supply voltage within a certain error window. Different fully-integrated LDO topologies are investigated regarding their suitability to supply low-voltage digital circuits. The any-load stable LDO topology is selected and implemented on a 0.13 µm test-chip. The LDO is able to provide a maximum load current of 2.5mA while consuming a quiescent current of 17 µA.

## 1 System overview: ultra-low-power microcontroller

Ultra-low-power microcontrollers (MCU) are used in many small scale battery-powered applications today. Typical examples are smart meters, alarm systems and medical monitoring devices. These applications spend most of their time in sleep mode consuming only a few microamperes and waking up periodically to perform a certain task. When activated their current consumption abruptly increases usually by more than three decades. Assuming a rather typical 1/1000 active/sleep ratio both modes consume half of the available energy and need to be optimized to maximize the battery lifetime (Zwerg, 2011).

While the external supply voltage of an ultra-low-power MCU system is determined by battery voltage over lifetime, its digital core requires a lower sub-regulated supply voltage. It is therefore supplied by an integrated LDO as depicted in Fig. 1. Keeping the LDO and consequently the digital core always powered causes digital leakage current as well as LDO quiescent current flowing even in sleep mode. To minimize LDO quiescent current in sleep mode, some ultra-low-power MCU systems use different LDOs, each optimized for a dedicated power mode, but with a complex and slow transition between them (Kristjansson, 2006).

As in modern CMOS technologies leakage current increases, the battery lifetime for typical ultra-low-power applications becomes more and more limited by leakage current in sleep mode. The most effective approach to minimize leakage current in sleep mode is to switch-off the digital core by disabling the LDO. Thereby, the pass-transistor of the LDO acts as power switch. Only some digital control and interrupt circuitry in the battery voltage domain remain active in sleep mode.

From an energy perspective, a minimum sleep time can be defined for which it is useful to switch-off the digital core. At each transition into sleep mode, the capacitance at the LDO output is discharged and consequently has to be recharged at wake-up. This results in a trade-off between saved leakage energy on the one hand and additional energy required for recharging the load capacitance on the other hand, as depicted in Fig. 2. To achieve fast and energy-efficient transitions between power modes, lowest capacitance at the LDO output is obviously preferred. Consequently, the large external capacitance at the LDO output, which is typically in the range of some 100 nF, is removed and only a much smaller on-chip capacitance remains. A welcome side-effect is a higher system integration resulting in lower system costs. However, as an LDO typically use the external capacitance for compensation, its absence greatly affects the LDO design.

In this paper, the fundamental design considerations for a fully-integrated LDO supplying the digital core of an ultra-low-power MCU are presented. In Sect. 2, the supply voltage requirements of the digital core and the interferences with the LDO are discussed. In Sect. 3, different LDO topologies are investigated regarding their suitability to supply the digital core. The any-load stable LDO topology is selected and implemented on a 0.13 µm test-chip. The measurement results are presented in Sect. 4.

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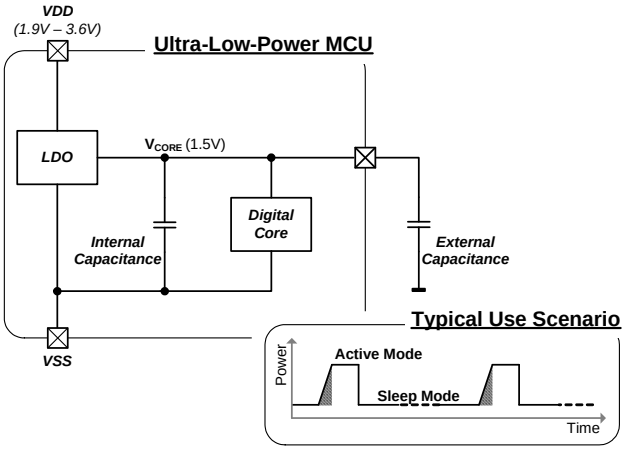


**Fig. 1.** Power supply system and typical use scenario of an ultra-low-power MCU.

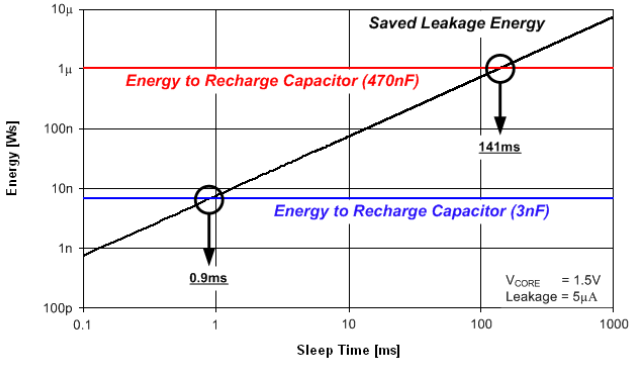


**Fig. 2.** The minimum sleep time for which it is useful to switch the digital core off is proportional to the LDO load capacitance.

## 2 LDO operating environment

To guarantee fault-free operation of the digital core, the core voltage must remain within a certain error window. This window is determined by reliability constraints of the digital core on the upper boundary side and speed requirements on the lower boundary side. To minimize current consumption of the digital core, the core voltage in an ultra-low-power MCU system is typically set to the lower boundary with some safety margin. This safety margin is determined by several tolerances within the supply system, which accumulate:

- Static inaccuracy of the reference voltage due to limited accuracy of the bandgap reference.
- Static inaccuracy due to limited LDO loop gain and LDO offset.
- Dynamic inaccuracy in response to fast line and load transient conditions due to limited LDO bandwidth.
- Supply noise within the on-chip power distribution network due to IR-drop and di/dt-drop.

The tolerances are budgeted during the system specification such that the core voltage always remains in the specified error window, which in the present case is $1.5\,\mathrm{V} \pm 0.1\,\mathrm{V}$.

The digital core operates synchronous to a system clock; it draws current by charging the various load capacitances whenever they are switched. Thereby, as depicted in Fig. 3a, the digital core creates large current spikes at each clock edge. The average current consumption of the digital core, which is equal to the LDO load current, can be expressed as:

$$I_{\mathrm{LOAD}} = \sum_{i=1}^{k} (\alpha_i C_i)\, f_{\mathrm{CLK}}\, V_{\mathrm{CORE}} \tag{1}$$

where $\alpha_i$ is the activity rate and $C_i$ is the load capacitance of a single digital logic gate, $f_{\mathrm{CLK}}$ is the system clock and $V_{\mathrm{CORE}}$ is the core voltage. The current consumption of the digital core can instantly change from zero to maximum (and back) when the system clock is gated. An LDO supplying the digital core must therefore have a large bandwidth in order to react as fast as clock speed determines.

To ensure the power integrity of the digital core, capacitance is allocated and distributed on-chip (Popovich, 2007). This capacitance acts at the same time as load capacitance for the fully-integrated LDO. As an LDO designed for low quiescent current is too slow to react on single current spikes produced by the digital core, there is a certain minimum on-chip capacitance required. Each current spike results in a voltage ripple $\Delta V_{\mathrm{CORE}}$, which is determined by charge sharing:

$$V_{\mathrm{CORE}} C_{\mathrm{LOAD}} = (V_{\mathrm{CORE}} + \Delta V_{\mathrm{CORE}}) \left( C_{\mathrm{LOAD}} + \sum_{i=1}^{k} (\alpha_i C_i) \right)$$

$$\Delta V_{\mathrm{CORE}} = - \frac{\sum_{i=1}^{k} (\alpha_i C_i)}{C_{\mathrm{LOAD}} + \sum_{i=1}^{k} (\alpha_i C_i)} V_{\mathrm{CORE}} \tag{2}$$

where $C_{\mathrm{LOAD}}$ is the on-chip capacitance. Inserting Eq. (1) into (2) and assuming that the load capacitance is sized much larger than the effective switching capacitance results in:

$$\Delta V_{\mathrm{CORE}} \approx - \frac{I_{\mathrm{LOAD}}}{f_{\mathrm{CLK}} C_{\mathrm{LOAD}}} \tag{3}$$

Thereby, the digital core is assumed to have the same effective switching capacitance at each clock edge. The resulting voltage ripple adds to the overall LDO inaccuracy. To limit this voltage ripple to a sufficient level of some 10 mV, a minimum on-chip capacitance is required, which depends on the maximum load current and is in the range of some nanofarads in case of an ultra-low-power MCU system.

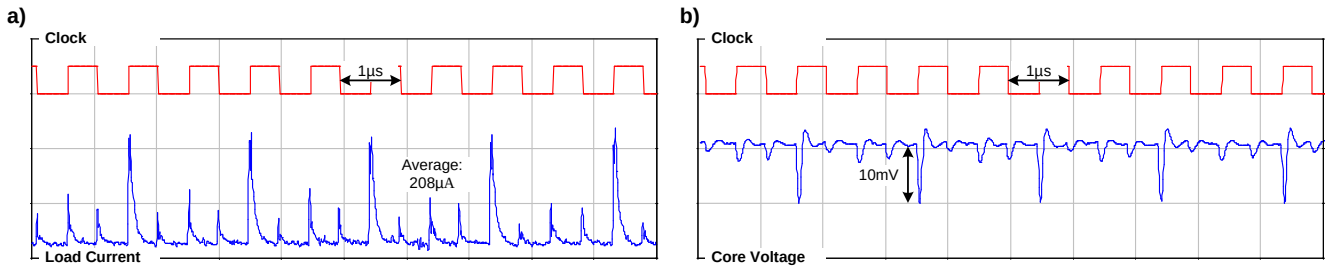


**Fig. 3.** **(a)** Simulated transient load current profile of the digital core when operating at 1 MHz, and **(b)** the resulting core voltage when the load current profile is presented to the any-load stable LDO with an on-chip capacitance of 3 nF.

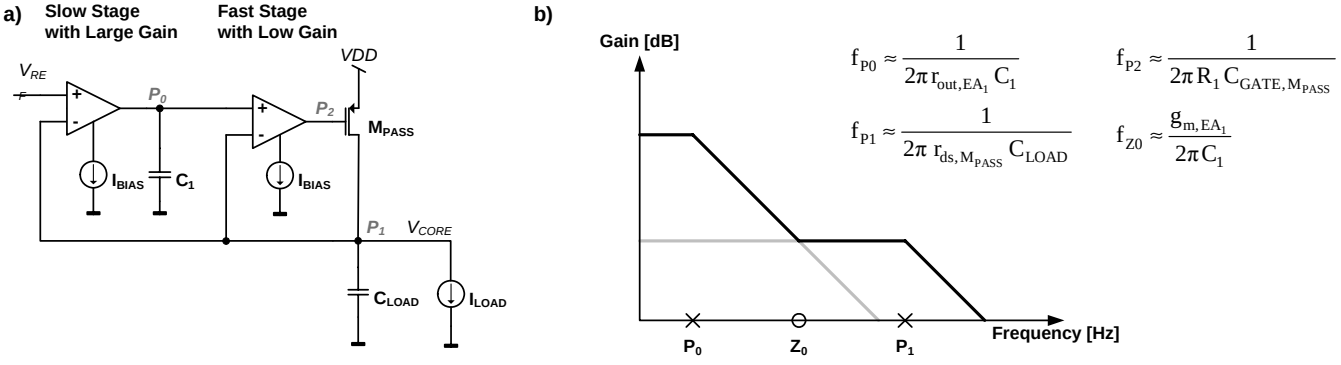


**Fig. 4.** **(a)** Block diagram of the any-load stable LDO, and **(b)** its open-loop gain over frequency: The any-load stable LDO topology is compensated by an active feed-forward compensation scheme.

Figure 3b shows the simulated core voltage when the transient load current profile of the digital core is presented to the fully-integrated any-load stable LDO with an on-chip capacitance of 3 nF.

## 3 Fully-integrated LDO

An LDO can be considered as a voltage buffer with a certain current drive capability. Ideally, the voltage buffer should have high gain for an accurate final value and large bandwidth for fast settling while loop stability is guaranteed under all operating conditions. In practice, it is not easy to combine these requirements. This is especially true for a fully-integrated LDO without a large (external) capacitance.

The design of fully-integrated LDOs has received a lot of attention in literature. While conventional LDO topologies are compensated by a large (external) capacitance with the dominant pole being at the LDO output, most of the presented, fully-integrated LDO topologies use some form of miller compensation to establish an internal, dominant pole (Guo, 2010; Leung, 2003). These LDO topologies in principle suffer from stability issues in light load conditions. Thereby, the required minimum load current increases for a larger capacitance at the LDO output. For example, the LDO topology presented in (Guo, 2010) requires a minimum load current of 3 mA while the capacitance is limited to 50 pF in order to achieve loop stability. Hence, these topologies are not best suited to supply the digital core of an ultra-low-power MCU system.

An alternative LDO topology, called any-load stable LDO, is presented in (Ivanov, 2009). This LDO topology achieves high gain and large bandwidth by combining two stages in two control loops as shown in Fig. 4a. The LDO topology is compensated by an active feed-forward compensation scheme (Thandri, 2003). As depicted in Fig. 4b, this compensation scheme uses the positive phase shift of a left-half-plane zero caused by the fast control loop to cancel the negative phase shift of the first dominant pole $P_0$. A second dominant pole $P_1$ is located at the LDO output. This pole widely moves with load current due to changing output impedance of the pass-transistor.

The transistor-level implementation of the any-load stable LDO topology is shown in Fig. 5a. While the slow stage is implemented as a folded-cascode amplifier, the fast stage is based on a cascoded flipped voltage follower (FVF) (Ramirez-Angulo, 2005). The cascoded FVF is formed by the common-gate transistors $M_{CG1}$ and $M_{CG2}$, the current

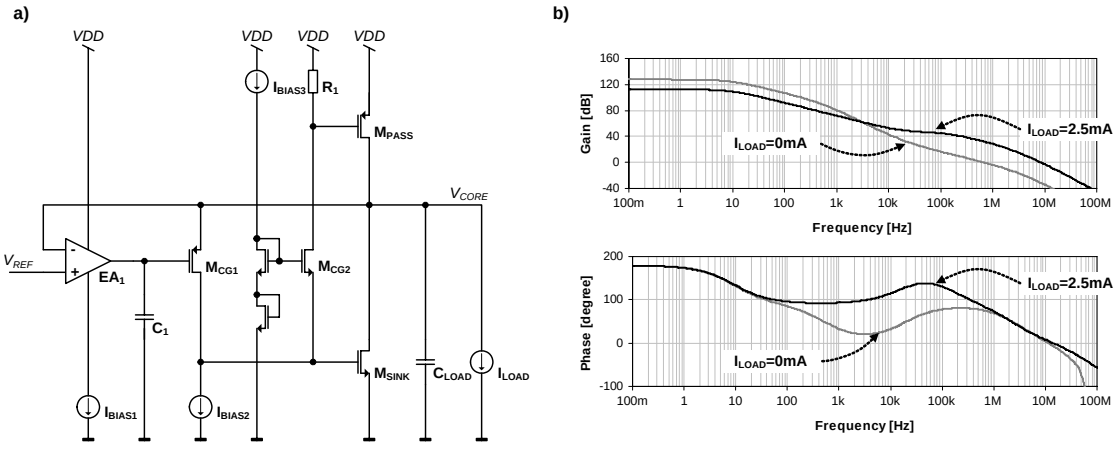


**Fig. 5.** **(a)** Basic circuit diagram of the any-load stable LDO topology, and **(b)** the simulated Bode plots for minimum and maximum load current at VDD = 3.0 V and $C_{\mathrm{LOAD}} = 3$ nF.

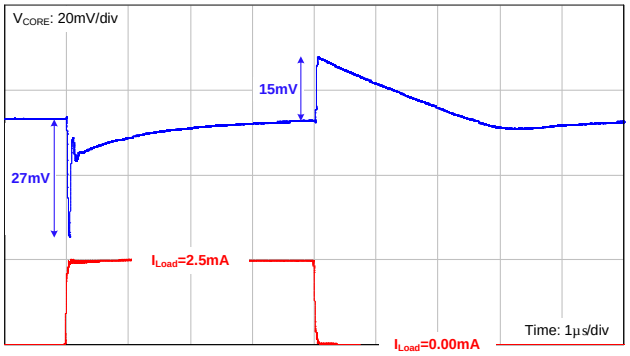


**Fig. 6.** Measured LDO transient behavior when applying a load current step from 0 mA to 2.5 mA under worst case conditions (VDD = 1.9 V, T = −40°C).

source $I_{\mathrm{BIAS2}}$, the resistor $R_1$ and the pass-transistor $M_{\mathrm{PASS}}$. The two control loops are combined at $M_{\mathrm{CG1}}$.

The first non-dominant pole $P_2$ of the cascoded FVF is defined by $R_1$ and the gate capacitance of $M_{\mathrm{PASS}}$. The cascoded FVF can be easily stabilized for any capacitance at the LDO output by adapting the resistance $R_1$. Thereby, loop stability for smaller capacitances requires an increased LDO quiescent current.

The simulated Bode plots of the any-load stable LDO topology in minimum and maximum load current condition are depicted in Fig. 5b. By employing the active feed-forward compensation scheme, loop stability is easily achieved over the full load current range without any limitations on the on-chip capacitance. The fully integrated any-load stable LDO is therefore well suited to supply the digital core of an ultra-low-power MCU system.

## 4 Measurement results

The any-load stable LDO has been implemented as part of a complete ultra-low-power MCU in a 0.13 µm digital CMOS process. The supported supply voltage range is determined by battery voltage over lifetime (1.9 V–3.6 V); the nominal output voltage is 1.5 V. Reference voltage and bias current are provided by a reference circuit not discussed here. The on-chip capacitance coming with the digital core is 3 nF. For test purposes, a DC load current profile can be generated by an on-chip circuit resulting in rise and fall times of 1 ns.

The LDO is able to provide a maximum load current of 2.5 mA while consuming a quiescent current of 17 µA. Fig. 6 shows the measured LDO transient behavior when applying a load current step from 0mA to 2.5 mA under worst case conditions (VDD = 1.9 V, T = −40°C). The resulting transient voltage errors are −27 mV and +15 mV, respectively. The effect of the multi-loop LDO topology with its slow and fast control loop is well noticeable from the transient response.

## 5 Conclusions

In this paper, the fundamental design requirements for a fully-integrated LDO supplying the digital core of an ultra-low-power MCU are summarized. Among other presented LDO topologies, the any-load stable LDO is selected and implemented on a test-chip. The LDO is able to provide a maximum load current of 2.5 mA while consuming a quiescent current of 17 µA. Its loop stability over the full load current range is proven by measurement results. The any-load stable LDO is therefore well suited to supply digital circuits.

## References

Zwerg, M., Baumann, A., Kuhn, R., Arnold, M., Nerlich, R., Herzog, M., Ledwa, R., Sichert, C., Rzehak, V., Thanigai, P., and Eversmann, B.: An 82 µA/MHz Microcontroller with Embedded FeRAM for Energy-Harvesting Applications, IEEE ISSCC 2011, 334–335, 2011.

Kristjansson, E.: ARM7 Low Power Design, White Paper www.microcontroller.com/ARM7_Low_Power_Design_-_White_Paper.htm, November 2006.

Popovich, M., Friedman, E., Secareanu, R., and Hartin, O.: Efficient placement of distributed on-chip decoupling capacitors in nanoscale ICs, IEEE ICCAD 2007, 811–816, 2007.

Guo, J. and Leung, K.: A 6 µW Chip-Area-Efficient Output-Capacitorless LDO in 90-nm CMOS Technology, IEEE JSSC, 45(9), 1896–1905, 2010.

Leung, K. and Mok, P.: A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation, IEEE JSSC, 38(10), 1691–1702, 2003.

Ivanov, V.: Design Methodology and Circuit Techniques for Any-Load Stable LDOs with Instant Load Regulation and Low Noise, Analog Circuit Design, 339–358, 2009.

Thandri B. and Silva-Martinez, J.: A robust feedforward compensation scheme for multistage operational trans-conductance amplifiers with no Miller capacitors, IEEE JSSC, 38(2), 237–243, 2003.

Ramirez-Angulo, J., Gupta, S., Padilla, I., Carvajal, R., Torralba, A., Jimenez, M., and Munoz, F.: Comparison of conventional and new flipped voltage structures with increased input/output signal swing and current sourcing/sinking capabilities, IEEE MWSCAS 2005, 2, 1151–1154, 2005.