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Coupling path influence on the conducted emission measurement results by the EMC semiconductor test board

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Abstract. The fact of reduced development time in the automotive sector requires a change in the electromagnetic compatibility (EMC) validation of electronic components. To increase the development time of automotive components, e.g. sensors or electronic control units (ECUs), it is mandatory to verify the EMC behavior of the integrated circuit (IC) itself in an early development stage simultaneous to the development process of the entire ECU into which it is embedded. The conducted IC EMC tests emission as well as immunity is realized with a specific test printed circuit board (PCB) which is built according to the guidelines of the Bosch, Infineon, Siemens VDO Specification (BISS, 2007). The measurement results of these EMC tests are affected by the test PCB itself. To deduce the application requirements of the component from the application circuit of the test PCB it is necessary to consider this influence by the printed circuit board. The text at hand gives an overview on how far the emission results are adulterated by the used test PCB. The presented method also grants a validation of the disturbance voltage directly at the IC pin considering the application circuit.

1 Introduction

To accelerate the development process of automotive components it is impossible to verify the complete new product, e.g. a sensor or ECU, at the end of the development process respecting the EMC. The tight schedule demands a systematic EMC validation of each complex sub module which is built into the component, e.g. an IC or microcontroller (µC) at an early development stage. A consistent EMC validation of each of these complex sub modules will usually decrease the number of EMC based redesigns and promises a good EMC performance of the entire component.

As usually at EMC tests, the conducted IC EMC tests are divided into emission and immunity tests, too. Both test versions are accomplished by a specific test PCB which has been particularly developed for each IC and includes the respective application circuits. In both emission and immunity case the test PCBs are usually populated with the same application circuits. Only the radio frequency (RF) coupling networks, which are used to carry the electro magnetic energy to the test receiver (emission) or the IC pin (immunity), differ. In case of the emission test the coupling network, as shown in Fig. 4, is used to connect the IC pin with the test receiver and matches the IC pin impedance to the 50 Ω measurement impedance as well as possible. At the immunity test, in contrast, the coupling network is only used to connect the RF immunity test setup with the IC pin via a DC block capacitor. The application circuit and the coupling/decoupling network influence the measurement results most. An efficient method to determine and consider the influence of the EMC semiconductor test PCB during the conducted emission test is given in this paper.

2 Conducted emission of integrated circuits

To verify an integrated circuit regarding its EMC behavior it is necessary to solder the device under test (DUT), including the application circuits, to a specific test PCB as shown in Figs. 2 and 3. By means of this test PCB it is possible to set the IC into different operating modes, like it is used in the ECU, and measure the conducted emission of any IC pin. Figure 1 illustrates the result of such a conducted emission measurement. The diagram shows the disturbance voltage of a supply pin which is measured at the RF connector of the test PCB by using an electromagnetic interference (EMI) test receiver. The frequency range of these measurements is

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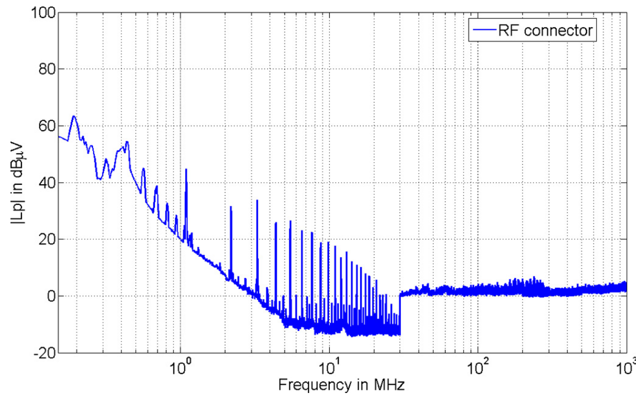

Fig. 1. Measured disturbance voltage at the RF-connector.

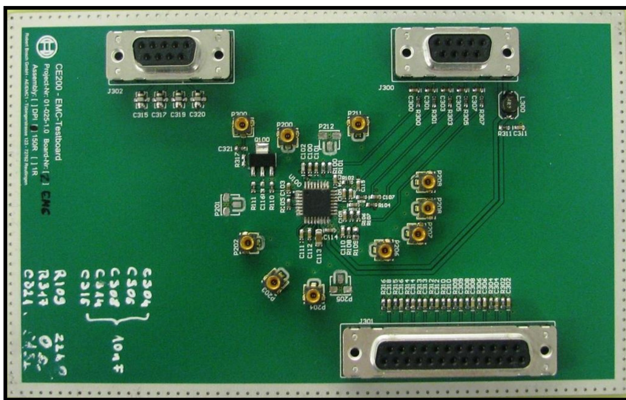

Fig. 2. EMC test PCB, top layer.

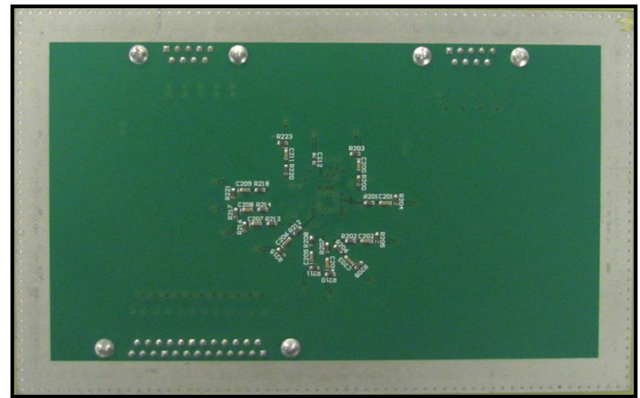

Fig. 3. EMC test PCB, bottom layer.

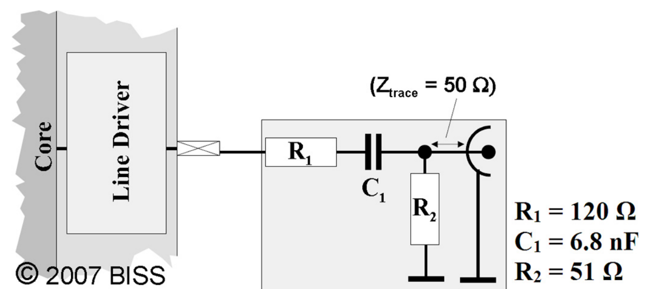

Fig. 4. Coupling network of the conducted emission measurement (BISS, 2007).

required in the BISS (2007) paper. It starts at 150 kHz an ends at 1 GHz. One significant item in this diagram is the amplitude offset at 30 MHz. This offset does not arise from the DUT itself but from the altered measurement bandwidth of the test receiver. The peaks at 1.1 MHz and integer multiples which rise up out of the noise floor derive from a charge pump which is embedded in the IC.

3 EMC test PCB

Figures 2 and 3 show the PCB which is used to determine the conducted emission of the IC. The circuit board consists of four layers with a dimension of 160 × 100 mm and is manufactured out of FR4 PCB material. The connectors are mounted onto the top layer, as shown in Fig. 2, to supply the IC and monitor the signals during the measurements. The IC and the application circuits are mounted on the top layer, too.

Regarding the bottom layer, which is shown in Fig. 3, it is only the RF coupling networks that are mounted onto the surface to match the IC pin impedance appropriate to the 50 Ω impedance of the measurement equipment. The coupling network consists of a 120 Ω series resistor on the IC side of the coupling network, followed by a 6.8 nF coupling capacitor and a 51 Ω parallel resistor to ground as shown in Fig. 4.

3.1 Characterization of the EMC test PCB

To characterize the scattering parameters of the test PCB a prober measuring station is used. The main constituent of this measuring station is a four port vector network analyzer (VNA) and a manual probe system. The VNA decreeds about a test frequency range from 9 kHz up to 8.5 GHz and a dynamic range of more than 120 dB. The manual probe system offers a front and back side microscope that enables a connection of the top and bottom layer concurrently.

Figure 5 shows the calibration substrate which is used to calibrate the entire measurement setup including the probes. By means of this substrate, a full two port calibration of the measurement setup is realized in the open, short, load and thru standard. After the measurement setup is calibrated the PCB characterization can be started. In Fig. 6 the top and bottom layer including the test points, which are used to characterize the coupling path of the supply pin, are shown.

To detect the complex scattering parameters of the test board any RF coupling path is considered as an independent two-port.

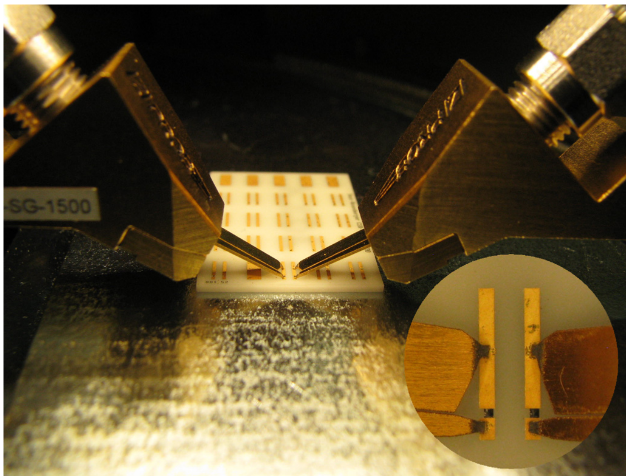

Fig. 5. Calibration measurement setup.

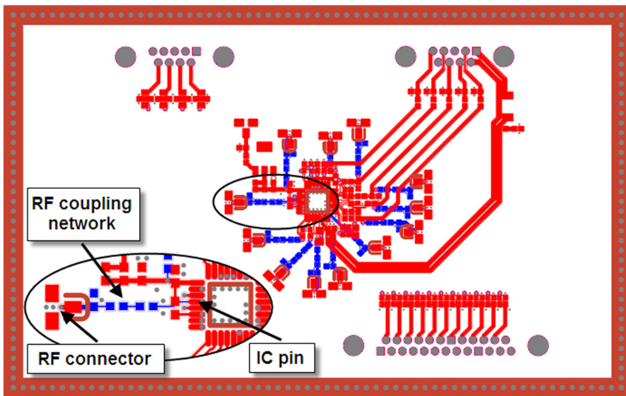

Fig. 6. Test points of the coupling path characterization.

Therefore the first port of the VNA is connected to the IC side of the coupling path and the second port is connected to the RF connector of the test PCB as it is shown in Fig. 7. During this measurements neither the RF connector nor the IC is mounted on the test PCB.

The results of this scattering parameter characterization is given in Fig. 8. The blue line illustrates the reflection coefficient S_{11} at the IC side of the coupling path. The worse progression of the curve is a result of the impedance mismatch between the 50 Ω port of the VNA and the coupling network. The cyan curve in this diagram shows the reflection coefficient S_{22} at the RF connector side of the coupling path. The progression of the curve gives a feedback for the well matching impedance of the VNA and the measured device under test (DUT). The forward transmission parameter S_{21} is congruent with the backward transmission parameter S_{12}, this confirms the reciprocity of the two-port.

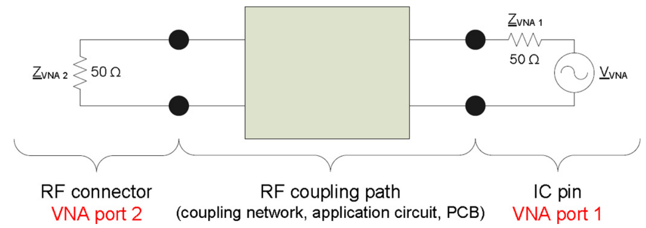

Fig. 7. Equivalent circuit of the scattering parameter measurement.

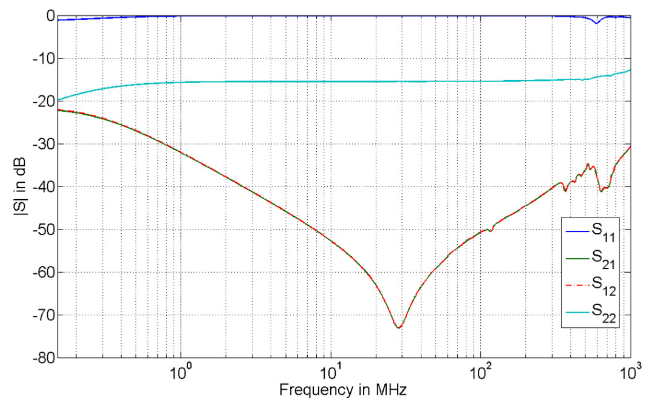

Fig. 8. Scattering parameter of the two-port.

4 Applied method

To determine the disturbance voltage directly at the IC pin, the influence of the used test PCB on the measurement results has to be considered. Therefore this particular PCB problem has to be transformed into a basic framework which could be used to describe an EMC problem in general (Paul, 2006). This framework divides all included elements of that problem into three main aspects like:

– Source (emitter)

– Transfer (coupling path)

– Receptor (receiver)

In case of the conducted emission the IC pin is considered as a source of the electromagnetic energy. After the energy is produced it will be transferred by using the RF coupling path of the EMC test PCB. Finally the transmitted RF energy will be absorbed by the EMI test receiver, as shown in Fig. 9. The IC pin, which generates the disturbance voltage, could be understood as a Thévenin equivalent circuit which is including a RF voltage source and an internal resistor.

The coupling path is represented by the influence of the coupling network, the application circuit and the printed circuit board. The third and last part of the given EMC basic decomposition is the used EMI test receiver which is interpreted as the receptor at the two-port output. In order to determine the disturbance voltage at the IC pin, the applied method is separated into the following items:

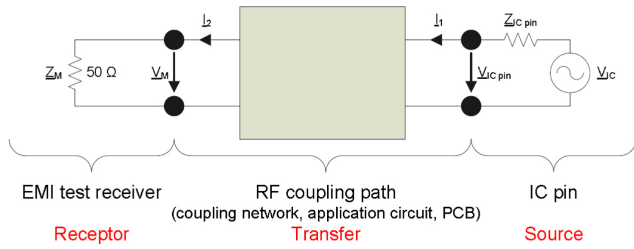

Fig. 9. Equivalent circuit of the IC pin emission measurement.

1. Measuring the disturbance voltage $\boldsymbol{V}_{\mathrm{M}}$ at the RF connector of the test PCB

2. Observing any RF coupling path as an independent two-port

3. Determining the voltage gain $\boldsymbol{A}_{\mathrm{v}}$ of any coupling path

4. Calculating the disturbance voltage $\boldsymbol{V}_{\mathrm{IC\,pin}}$ straight at the IC pin by using the voltage gain of the coupling path

After the complex scattering parameters of the EMC test PCB are measured, the voltage gain of each coupling path can be calculated by using the following formula (Michel, 1981):

$$\boldsymbol{A}_{\mathrm{v}([\mathbf{S}],\boldsymbol{\Gamma}_{\mathrm{M}})} = \frac{\hat{\boldsymbol{V}}_{\mathrm{M}}}{\hat{\boldsymbol{V}}_{\mathrm{IC\,pin}}} = \frac{-\boldsymbol{S}_{21}(\boldsymbol{\Gamma}_{\mathrm{M}}+1)}{(\boldsymbol{S}_{11}\boldsymbol{S}_{22}-\boldsymbol{S}_{12}\boldsymbol{S}_{21}+\boldsymbol{S}_{22})\boldsymbol{\Gamma}_{\mathrm{M}}-\boldsymbol{S}_{11}-1} \quad (1)$$

As it is shown in Eq. (1) the voltage gain of the coupling path is depending on the scattering parameters [**S**] of the test PCB on the one hand, and the reflection coefficient $\boldsymbol{\Gamma}_{\mathrm{M}}$ which is appearing at the RF connector of the test PCB on the other hand. Section 3.1 describes how to measure the scattering parameters. However, the reflection coefficient cannot be measured during the emission test and therefore remains unknown. For this reason the consequence of change in this parameter is investigated in the next few chapters.

4.1 Output impedance of the considered two-port

The reflection coefficient at the RF connector of the printed circuit board results from the impedance mismatch between the RF connector itself and the output impedance of the two-port, as shown in Fig. 10. For this reason the output impedance of the two-port has to be calculated first.

In addition the two-port, as shown in Fig. 11, which includes the behavior of the coupling network, the application circuit and the printed circuit board, is considered as a Thévenin equivalent circuit including the elements of the input circuit (Berroth, 2009). Now the internal resistance of the Thévenin equivalent circuit, which is identical to the output impedance of the two-port, has to be calculated.

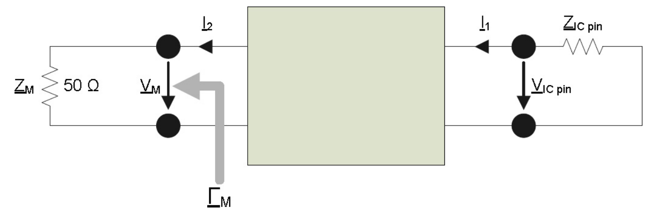

Fig. 10. Reflection coefficient at the RF connector of the test PCB.

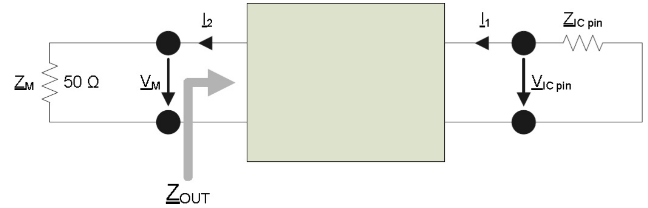

Fig. 11. Output impedance of the two-port.

Figure 12 shows this new equivalent circuit which is used to determine the two-port output impedance.

The output impedance calculation of the two-port is realized by the following equation (Berroth, 2009), in which [**A**] is the chain parameter (ABCD-parameter) matrix of the two-port and $\boldsymbol{Z}_{\mathrm{IC\,pin}}$ the impedance of the IC pin.

$$\boldsymbol{Z}_{\mathrm{eq}} = \boldsymbol{Z}_{\mathrm{OUT}} = \left.\frac{\boldsymbol{A}_{22}\boldsymbol{Z}_{\mathrm{IC\,pin}}+\boldsymbol{A}_{12}}{\boldsymbol{A}_{21}\boldsymbol{Z}_{\mathrm{IC\,pin}}+\boldsymbol{A}_{11}}\right|_{V_{\mathrm{IC}}=\mathrm{shorted}} \quad (2)$$

With Eq. (3) to Eq. (6) (Meinke and Gundlach, 1992) the chain parameters of the two-port can be calculated by the measured scattering parameters of each coupling path.

$$\boldsymbol{A}_{11} = \frac{(1+\boldsymbol{S}_{11})(1-\boldsymbol{S}_{22})+\boldsymbol{S}_{12}\boldsymbol{S}_{21}}{2\boldsymbol{S}_{21}} \quad (3)$$

$$\boldsymbol{A}_{12} = \frac{Z_0((1+\boldsymbol{S}_{11})(1+\boldsymbol{S}_{22})-\boldsymbol{S}_{12}\boldsymbol{S}_{21})}{2\boldsymbol{S}_{21}} \quad (4)$$

$$\boldsymbol{A}_{21} = \frac{(1-\boldsymbol{S}_{11})(1-\boldsymbol{S}_{22})-\boldsymbol{S}_{12}\boldsymbol{S}_{21}}{Z_0 2\boldsymbol{S}_{21}} \quad (5)$$

$$\boldsymbol{A}_{22} = \frac{(1-\boldsymbol{S}_{11})(1+\boldsymbol{S}_{22})+\boldsymbol{S}_{12}\boldsymbol{S}_{21}}{2\boldsymbol{S}_{21}} \quad (6)$$

Equation (2) in combination with Eqs. (3) to (6) demonstrates the influence of different parameters on the two-port output impedance like scattering parameters, reference impedance ($Z_0 = 50\,\Omega$) and the IC pin impedance. The scattering parameters and the reference impedance are now well known as shown above. The only missing parameter to calculate the output impedance is the unknown IC pin impedance. Since it is not possible neither to measure the pin impedance during the emission test nor to determine it with the available measurement results, both worst cases, open circuit and short circuit of the IC pin impedance, are investigated. Figure 13

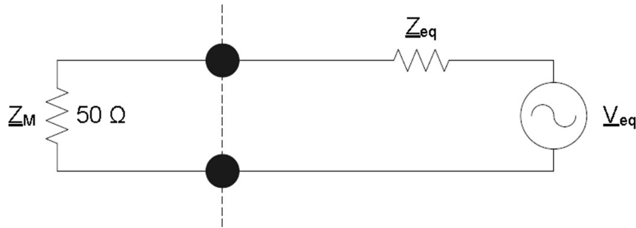

Fig. 12. Thévenin equivalent circuit of the two-port output (Berroth, 2009).

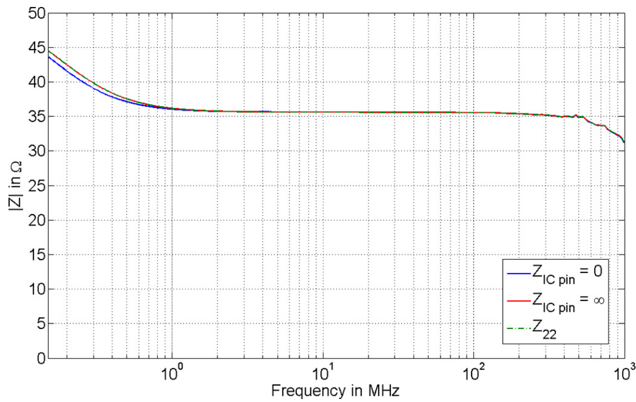

Fig. 13. Output impedance of the two-port by varying the IC pin impedance.

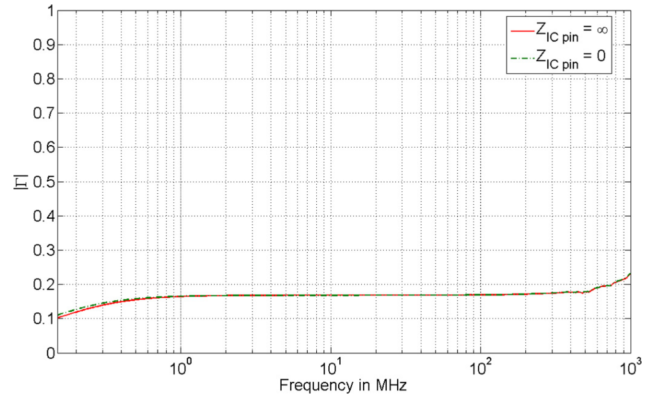

Fig. 14. Reflection coefficient at the RF connector of the test PCB by varying the IC pin impedance.

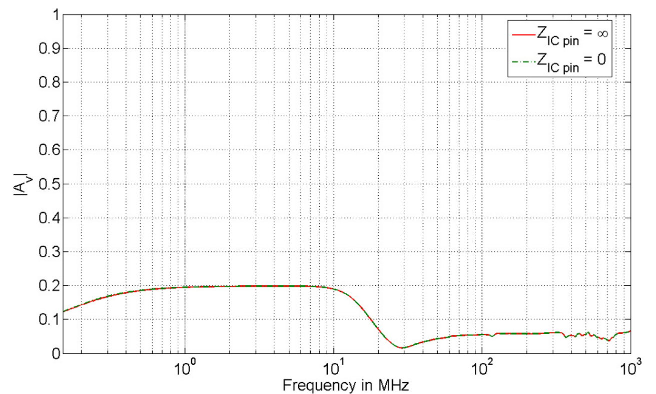

Fig. 15. Voltage gain of the coupling path by varying the IC pin impedance.

illustrates the marginal influence of a varying pin impedance between 0 and ∞ on the output impedance of the two-port. The green dash-dot line shows the progression of the secondary open loop impedance of the two-port. This graph matches completely with the output impedance in case the pin impedance is ∞.

4.2 Reflection coefficient at the RF connector

Both worst case values which have previously been determined for the open circuit and short circuit case of an IC pin will be used to calculate the reflection coefficient at the RF connector of the EMC test PCB. Equations (7) and (8) display the interrelationship between the reflection coefficient and the varying output impedance of the two-port.

$$\boldsymbol{\Gamma}_{\mathrm{M_{min}}} = \frac{\boldsymbol{Z}_{\mathrm{M}} - \boldsymbol{Z}_{\mathrm{OUT_{max}}}}{\boldsymbol{Z}_{\mathrm{M}} + \boldsymbol{Z}_{\mathrm{OUT_{max}}}} \tag{7}$$

$$\boldsymbol{\Gamma}_{\mathrm{M_{max}}} = \frac{\boldsymbol{Z}_{\mathrm{M}} - \boldsymbol{Z}_{\mathrm{OUT_{min}}}}{\boldsymbol{Z}_{\mathrm{M}} + \boldsymbol{Z}_{\mathrm{OUT_{min}}}} \tag{8}$$

As shown in Fig. 14, the variation of the IC pin impedance between the both worst cases 0 and ∞ is hardly visible. Both curves are nearly congruent over the entire frequency range.

4.3 Voltage gain of the coupling path

The reflection coefficient, whose performance range is calculated in the last chapter, is the last missing parameter of Eq. (1). Now the voltage gain of the coupling path can be determined for both worst case reflection coefficient values by using the measured scattering parameters of the EMC test PCB. Figure 15 shows the results of the voltage gain by varying the IC pin impedance.

The red line illustrates the performance for an open circuit inside the IC pin ($\boldsymbol{Z}_{\mathrm{IC\,pin}} = \infty$) which is accompanied by a minimum reflection coefficient at the RF connector. The green dash-dot line represents a short circuit inside the IC pin ($\boldsymbol{Z}_{\mathrm{IC\,pin}} = 0$) which is accompanied by a maximum reflection coefficient at the connector.

4.4 Disturbance voltage straight at the IC pin

After the voltage gain of the coupling path is determined the disturbance voltage straight at the IC pin can be calculated by the following equation (Michel, 1981):

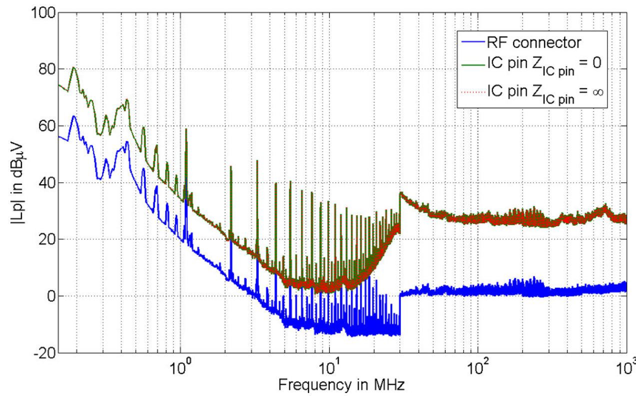

Fig. 16. Influence of the RF coupling path to the conducted emission measurement results.

$$\hat{V}_{\mathrm{IC\,pin}} = \frac{\hat{V}_{\mathrm{M}}}{A_{\mathrm{v}([\mathbf{S}],\Gamma_{\mathrm{M}})}} \quad (9)$$

The influence of the EMC semiconductor test PCB on the conducted emission EMC test is shown in Fig. 16. The blue line illustrates the disturbance voltage of a supply pin, measured at the RF connector of the test PCB which is accompanied by the output voltage at the two-port. The green respectively red dotted curve represents the determined disturbance voltage directly at the IC pin of both worst cases.

As in case of the voltage gain the deviation between a short circuit inside the IC pin ($Z_{\mathrm{IC\,pin}} = 0$) and an open circuit inside the IC pin ($Z_{\mathrm{IC\,pin}} = \infty$) is also very low and calculated to less than 0.1 dB. This robustness of the RF coupling path regarding its transmission behavior against the varying IC pin impedance is caused by the dominant external circuit devices. The difference between the blue and the green respectively red dotted line, which could be up to 36 dB in case of this investigated supply pin, is caused by the EMC test PCB.

5 Conclusions

The RF coupling path influence on the conducted emission measurements due to the EMC semiconductor test PCB is presented in this paper. By using this method a pin selective validation of the IC regarding its conducted emission, excluding the external circuit devices is possible. The robustness of the RF coupling path against the varying IC pin impedance, regarding both, its transmission behavior and the voltage gain of the investigated IC pin, has been proved. This ruggedness of the two-port is caused by the dominant external application circuit of the supply pin. A more dominant external circuit increases the robustness of the coupling path against the varying IC pin impedance. After a pin selective validation of the IC regarding its conducted emission is realized, the application requirements of the component (ECU/sensor) can be deduced from the application circuit of the EMC test PCB.

References

Berroth, M.: Vorlesungsskript, Theorie der Schaltungen III, Kapitel 4: Grundzuege der Vierpoltheorie, Institut fuer Elektrische und Optische Nachrichtentechnik, Universitaet Stuttgart, http://jfz.50g.com/files/tdslll-kapitel_4.pdf, October 2009.

BISS; Bosch, Infineon, Siemens VDO Specification: Generic IC EMC Test Specification 2004–2007.

Meinke, H. and Gundlach, F. W.: Taschenbuch der Hochfrequenztechnik, Hrsg. von Lange, K., Loecherer, K.-H., ISBN-10:3-540-54714 -2, Springer-Verlag, Fuenfte Auflage, 1992.

Michel, H.-J.: Zweitor-Analyse mit Leistungswellen, Studienbuecher Elektrotechnik, ISBN-10:3-519-06112-0, B. G. Teubner Stuttgart, 1981.

Paul, C. R.: Introduction to electromagnetic compatibility, ISBN-13: 978-0-471-75500-5, John Wiley & Sons Inc., second edition, 2006.